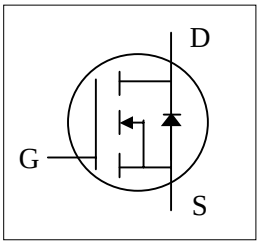
XP15NA7R4CDT

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% R_g & UIS Test**
- ▼ **Simple Drive Requirement**
- ▼ **Low On-resistance**
- ▼ **RoHS Compliant & Halogen-Free**



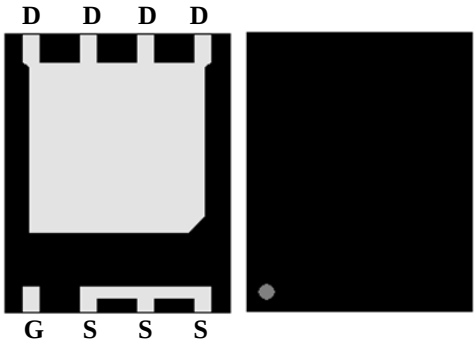
BV_{DSS}	150V
$R_{DS(ON)}$	7.4mΩ

Description

XP15NA7R4C series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PDFN5x6-FL package used advanced package and silicon combination for ultra low on-resistance and high efficiency, special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

PDFN5x6-FL



Bottom View **Top View**

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4](Silicon Limited)	120	A
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4](Package Limited)	100	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	85	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	18.6	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	15.6	A
I_{DM}	Pulsed Drain Current[1]	400	A
P_D@T_C=25℃	Total Power Dissipation	250	W
P_D@T_A=25℃	Total Power Dissipation[3]	6	W
E_{AS}	Single Pulse Avalanche Energy[6]	312.5	mJ
T_{STG}	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	0.6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	25	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	150	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=50A	-	-	7.4	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=50A	-	95	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=120V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[5]	I_D=50A	-	91	146	nC
Q_{gs}	Gate-Source Charge[5]	V_{DS}=75V	-	23	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]	V_{GS}=10V	-	31	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=75V	-	23	-	ns
t_r	Rise Time[5]	I_D=50A	-	102	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=6Ω	-	76	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	154	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	4450	7120	pF
C_{oss}	Output Capacitance[5]	V_{DS}=100V	-	350	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	30	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.8	1.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=50A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[5]	I_S=50A, V_{GS}=0V,	-	83	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	220	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.

4.Package limitation current is 100A .

5.Guaranteed by design.

6.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , V_{GS}=10V ,I_{AS}=25A

7.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

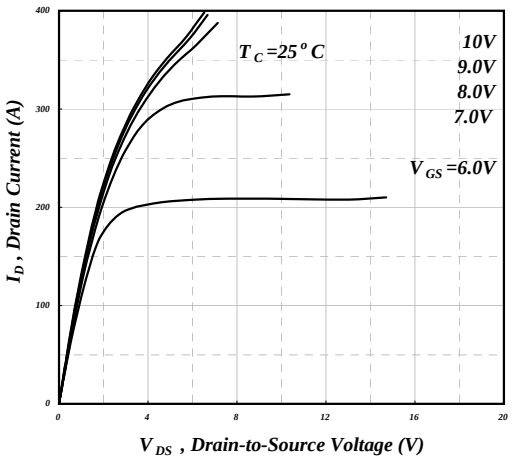


Fig 1. Typical Output Characteristics

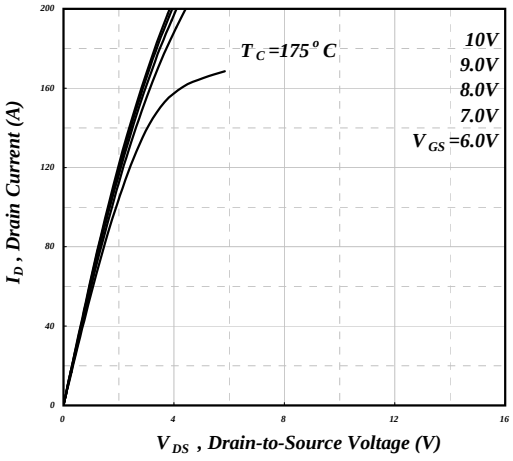


Fig 2. Typical Output Characteristics

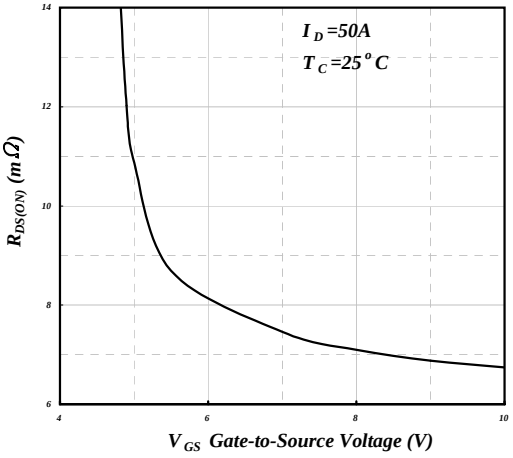


Fig 3. On-Resistance v.s. Gate Voltage

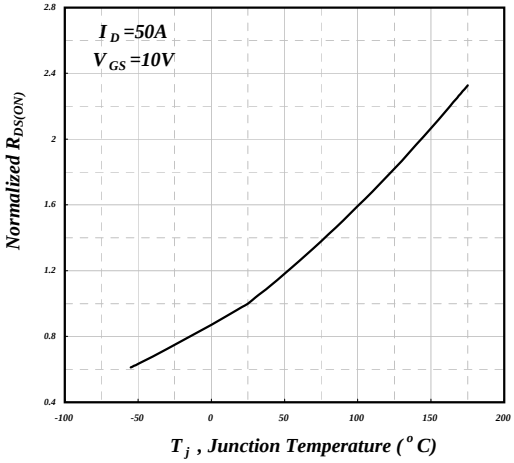


Fig 4. Normalized On-Resistance v.s. Junction Temperature

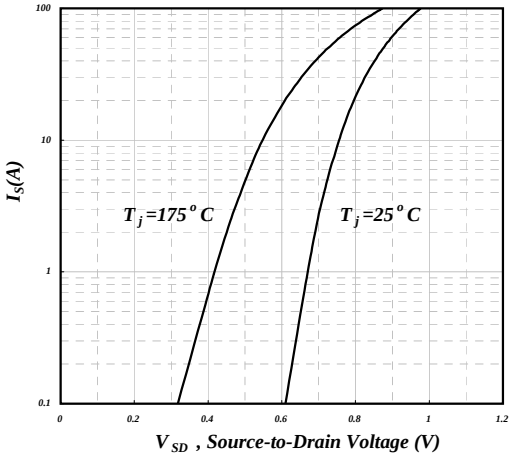


Fig 5. Forward Characteristic of Reverse Diode

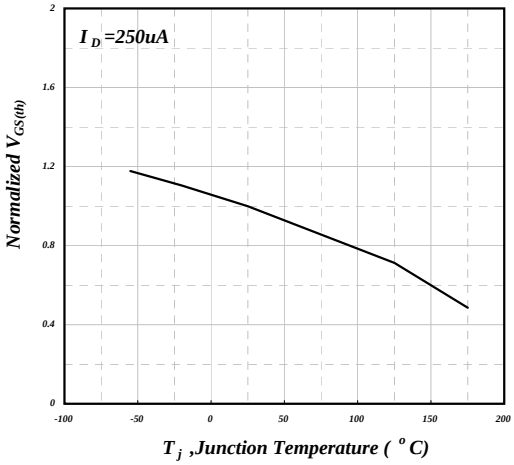


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

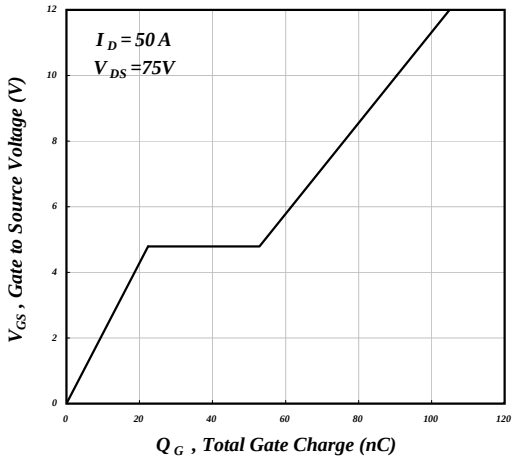


Fig 7. Gate Charge Characteristics

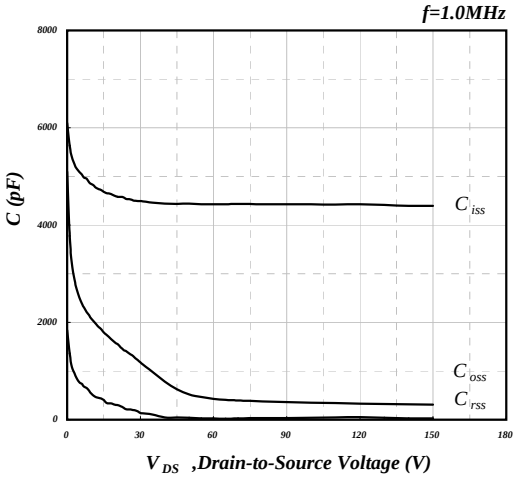


Fig 8. Typical Capacitance Characteristics

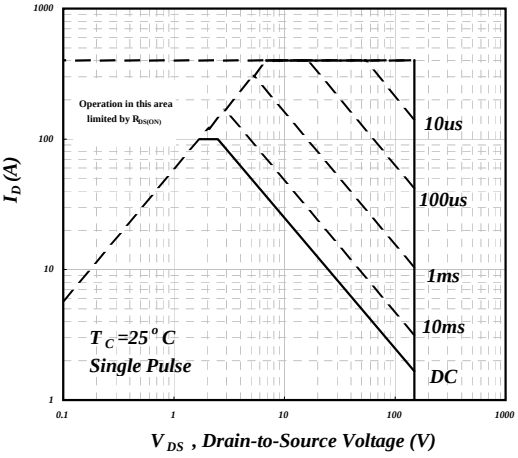


Fig 9. Maximum Safe Operating Area[7]

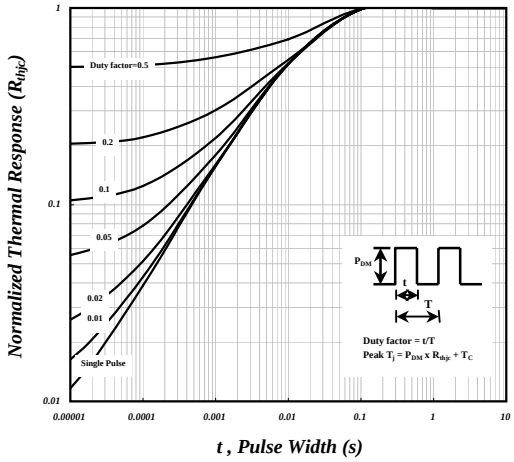


Fig 10. Effective Transient Thermal Impedance

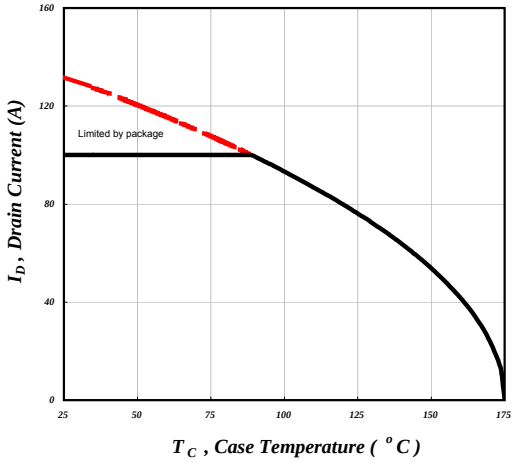


Fig 11. Drain Current v.s. Case Temperature

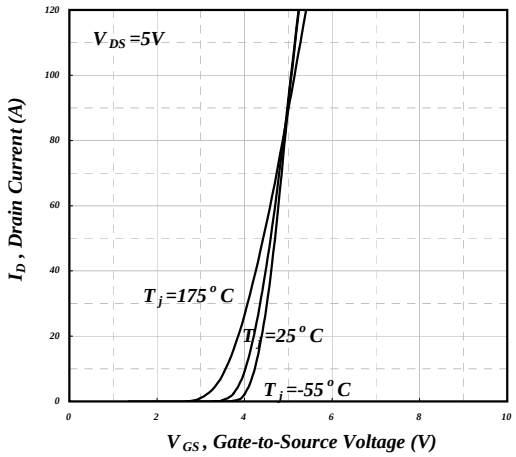


Fig 12. Transfer Characteristics

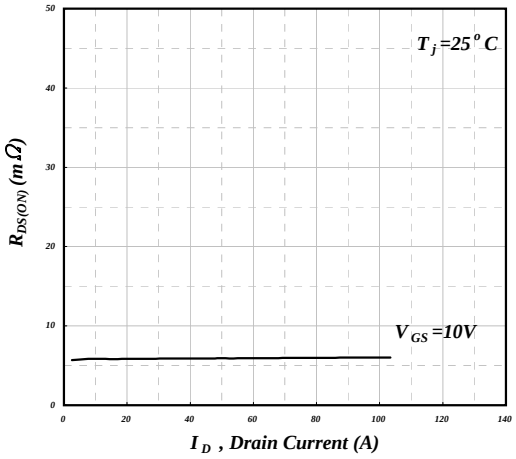


Fig 13. Typ. Drain-Source on State Resistance

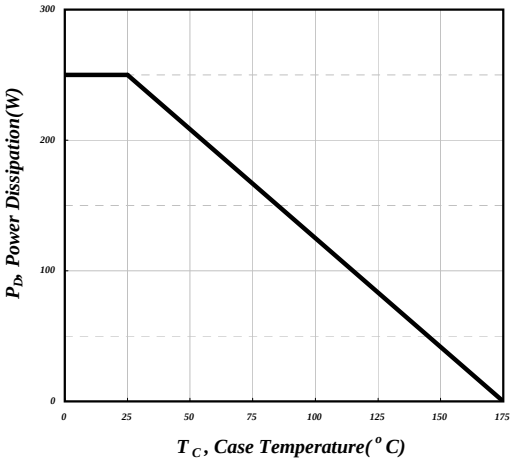


Fig 14. Total Power Dissipation

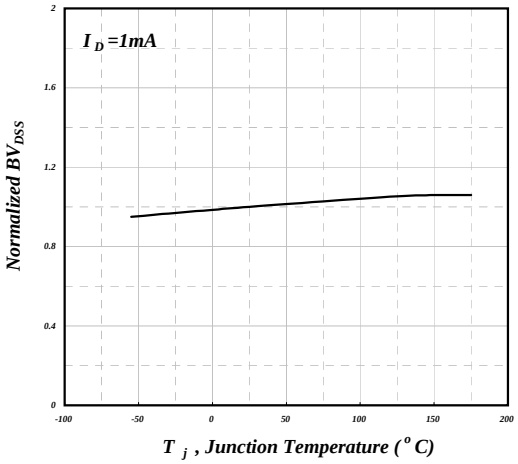
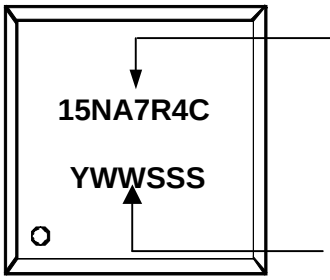


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION



Part Number

Date Code (YWWSSS)

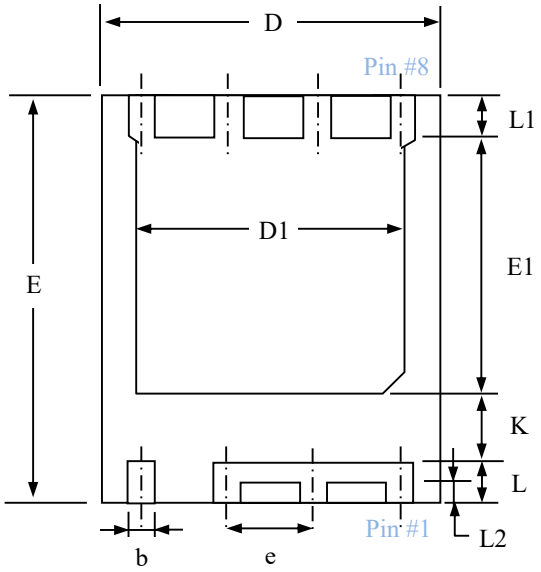
Y：Last Digit Of The Year

WW：Week

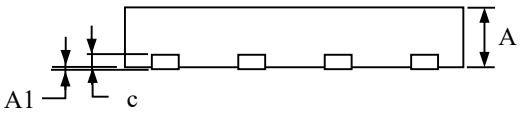
SSS：Sequence

Package Outline :PDFN 5x6-FL

BOTTOM VIEW



SIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.000	0.025	0.050
b	0.30	0.40	0.50
c	0.218 REF		
D	5.00 BSC		
D1	3.80	3.95	4.10
E	6.00 BSC		
E1	3.55	3.70	3.85
e	1.27 BSC		
L	0.50	0.60	0.70
L1	0.50	0.60	0.70
L2	0.20	0.30	0.40
K	0.95	1.10	1.25

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

Draw No. : M1-DT(FL)-8-I-G-v01

PDFN5x6-FL FOOTPRINT：