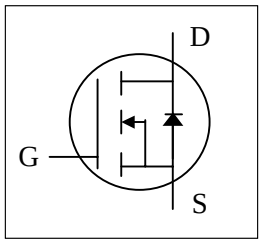
XP10NB5R5H

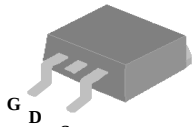
Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% R_g & UIS Test**
- ▼ **Simple Drive Requirement**
- ▼ **Lower On-resistance**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	100V
$R_{DS(ON)}$	5.5mΩ



TO-252(H)

Description

XP10NB5R5 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[6](Silicon Limited)	103.6	A
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[6](Package Limited)	75	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	73	A
I_{DM}	Pulsed Drain Current[1]	350	A
P_D@T_C=25℃	Total Power Dissipation	125	W
P_D@T_A=25℃	Total Power Dissipation[3]	2.4	W
E_{AS}	Single Pulse Avalanche Energy[4]	200	mJ
T_{STG}	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.2	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=40A	-	-	5.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=40A	-	80	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[5]	I_D=40A	-	54	87	nC
Q_{gs}	Gate-Source Charge[5]	V_{DS}=50V	-	16	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]	V_{GS}=10V	-	17	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=50V	-	16	-	ns
t_r	Rise Time[5]	I_D=40A	-	88	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=7.5Ω	-	45	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	110	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	2950	4720	pF
C_{oss}	Output Capacitance[5]	V_{DS}=80V	-	440	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.5	3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=40A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[5]	I_S=40A, V_{GS}=0V	-	64	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	93	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board

4.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , V_{GS}=10V ,I_{AS}=20A

5.Guaranteed by design.

6.Package limitation current is 75A .

7.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

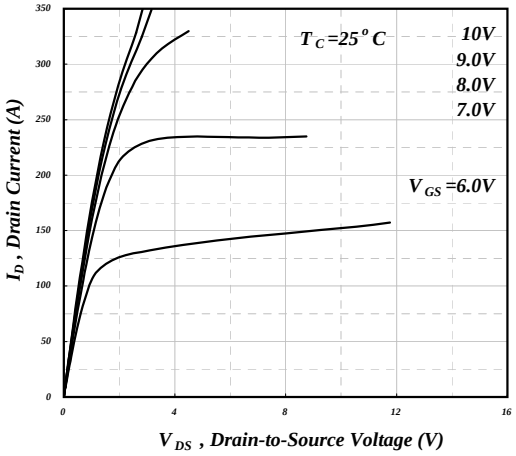


Fig 1. Typical Output Characteristics

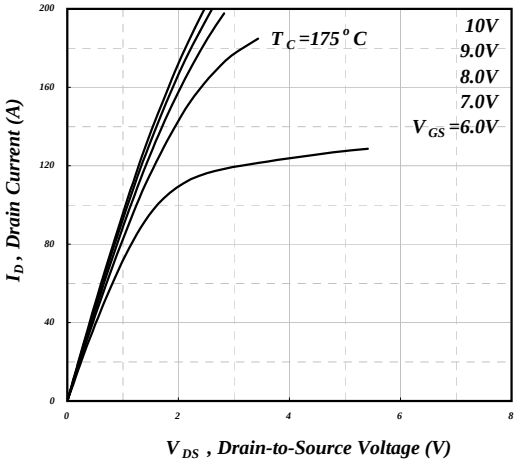


Fig 2. Typical Output Characteristics

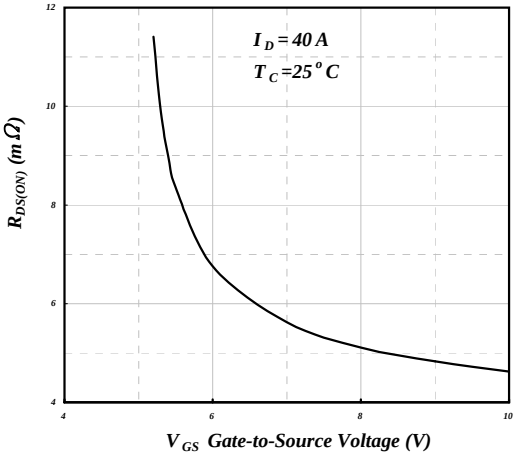


Fig 3. On-Resistance v.s. Gate Voltage

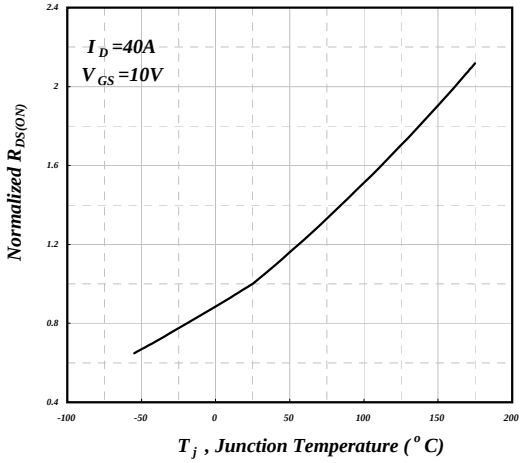


Fig 4. Normalized On-Resistance v.s. Junction Temperature

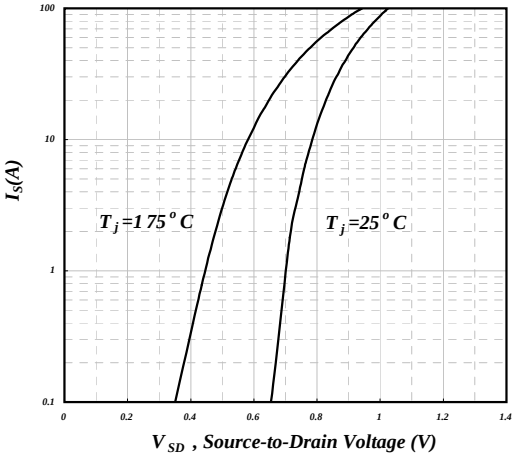


Fig 5. Forward Characteristic of Reverse Diode

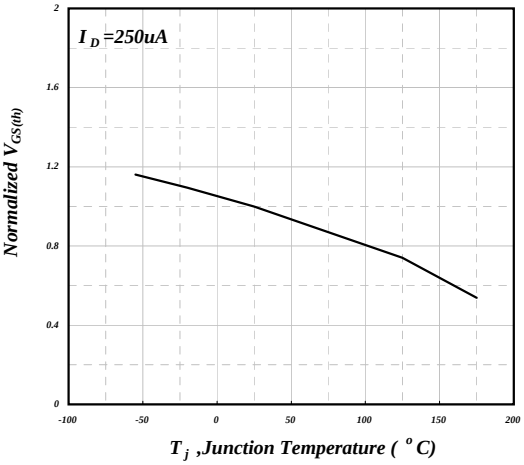


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

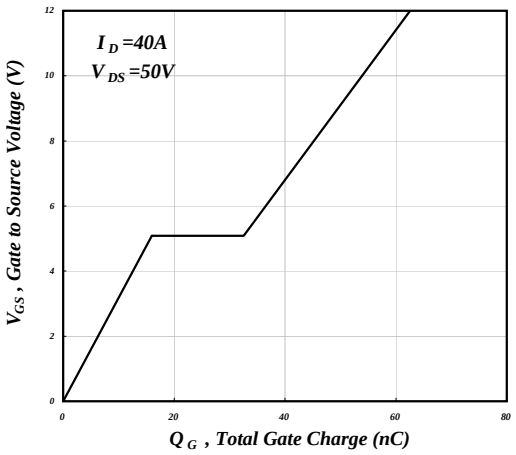


Fig 7. Gate Charge Characteristics

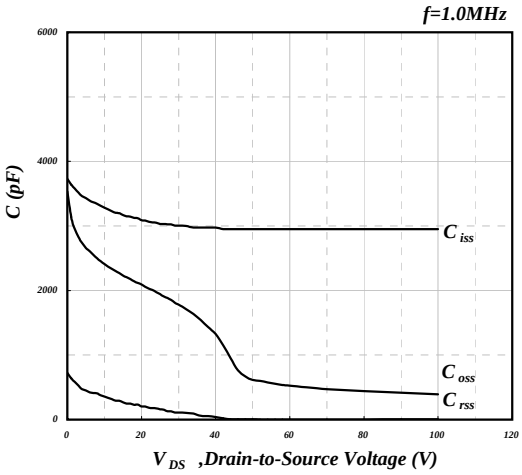


Fig 8. Typical Capacitance Characteristics

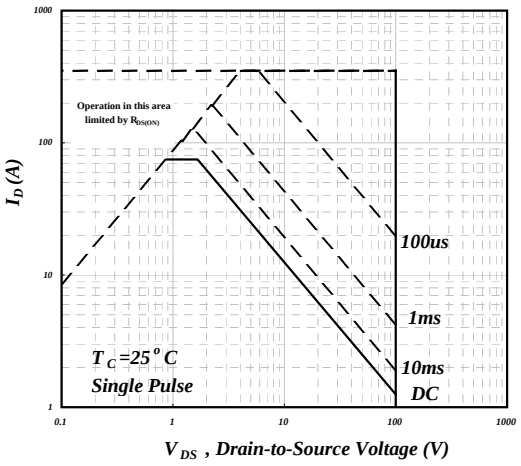


Fig 9. Maximum Safe Operating Area[6]

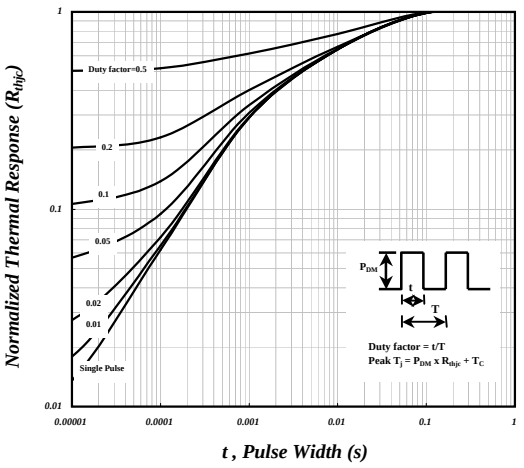


Fig 10. Effective Transient Thermal Impedance

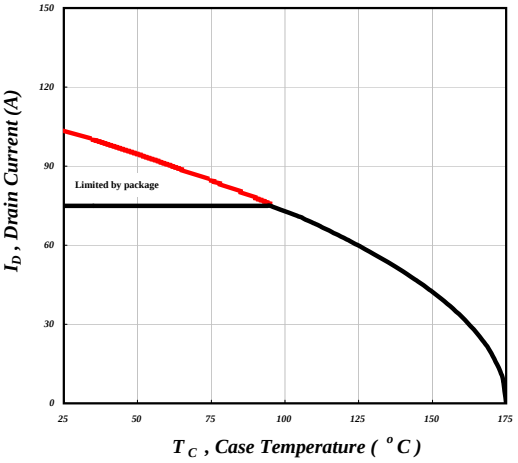


Fig 11. Drain Current v.s. Case Temperature

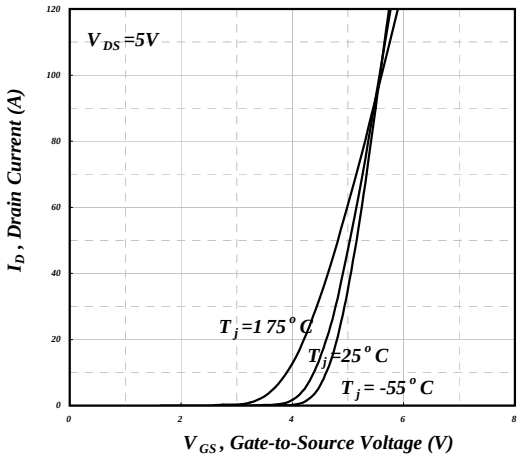


Fig 12. Transfer Characteristics

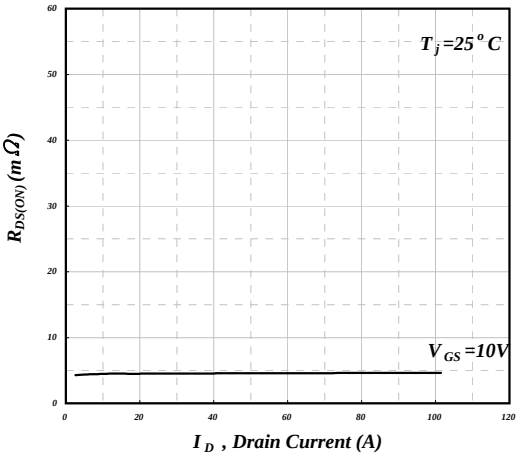


Fig 13. Typ. Drain-Source on State Resistance

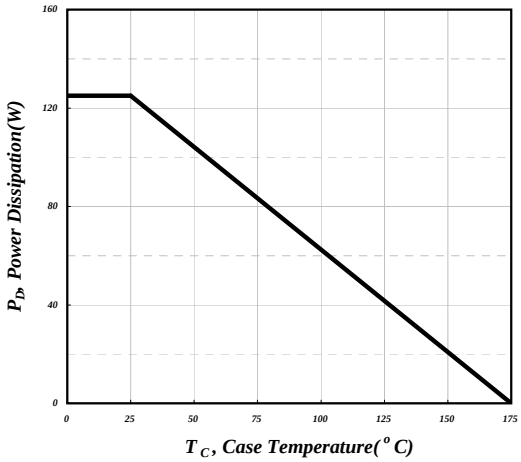


Fig 14. Total Power Dissipation

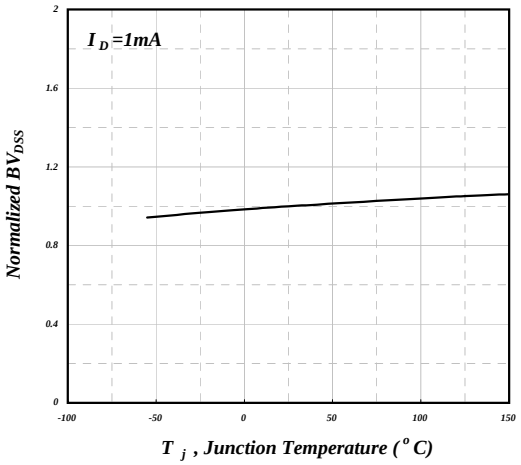
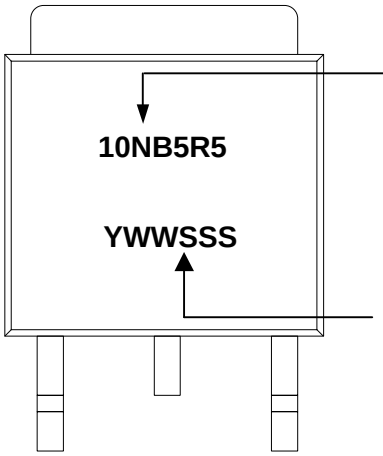
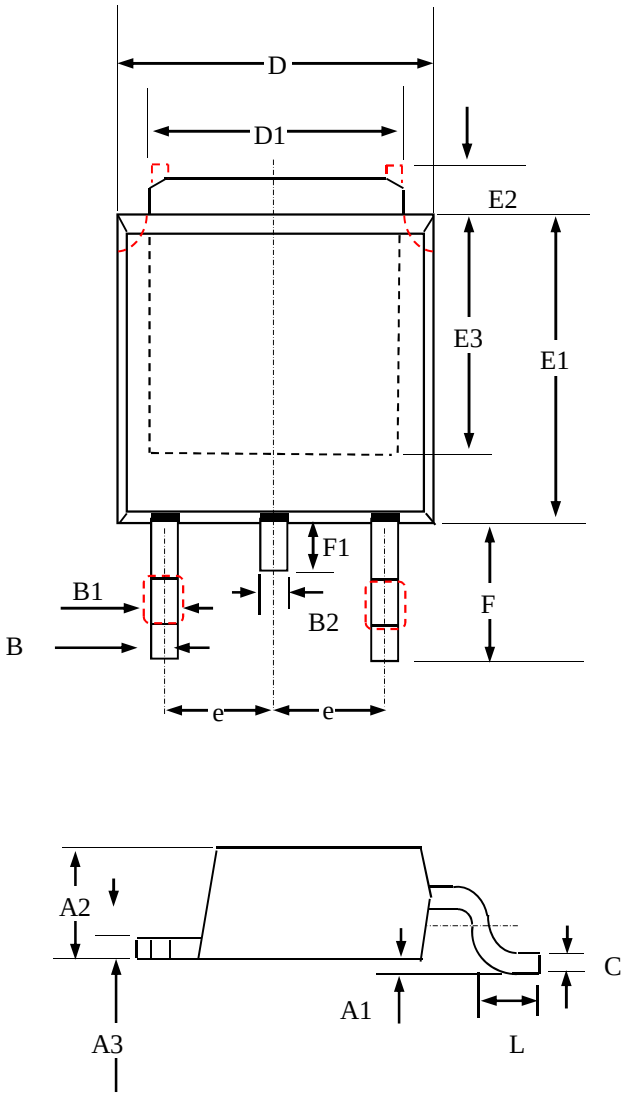


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION



Package Outline : TO-252



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A2	2.18	2.30	2.40
A3	0.40	0.50	0.65
B	0.40	0.70	1.00
B1	0.50	0.85	1.20
D	6.00	6.50	6.80
D1	4.80	5.35	5.90
E3	4.00 (ref.)		
F	2.00	2.63	3.05
F1	0.50	0.85	1.20
E1	5.00	5.70	6.30
E2	0.50	1.10	1.80
e	2.3 (ref)		
C	0.35	0.525	0.70
A1	0.00	—	0.25
B2	—	—	1.25
L	0.90	1.34	1.78

1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.

3. Thermal PAD, Body and Pin contour is for reference, it may has little difference by option.

Draw No. M1-H3EFIMT-G-v10

TO-252 FOOTPRINT：