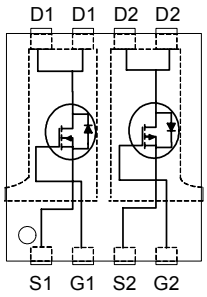
XP10C036LMT

Halogen-Free Product

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- **Simple Drive Requirement**
- **Good Thermal Performance**
- **Fast Switching Performance**
- **RoHS Compliant & Halogen-Free**

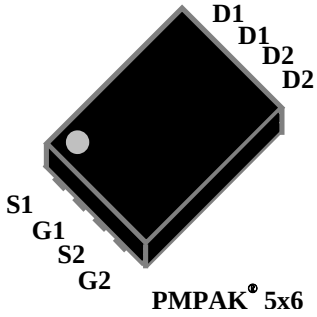


N-CH	BV_{DSS}	100V
	$R_{DS(ON)}$	36mΩ
P-CH	BV_{DSS}	-100V
	$R_{DS(ON)}$	60mΩ

Description

XP10C036L series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK ® 5x6 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



PMPAK® 5x6

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	100	-100	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	18.4	-14.6	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	7.6	-6	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	6.3	-5	A
I_{DM}	Pulsed Drain Current[1]	30	-30	A
P_D@T_A=25℃	Total Power Dissipation	4.28		W
T_{STG}	Storage Temperature Range	-55 to 175		℃
T_J	Operating Junction Temperature Range	-55 to 175		℃

Thermal Data

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
Rthj-c	Maximum Thermal Resistance, Junction-case	6	6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	35	35	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=6A	-	-	36	mΩ
		V_{GS}=4.5V, I_D=3A	-	-	60	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.3	-	2.5	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=6A	-	12	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[4]	I_D=6A	-	12.5	20	nC
Q_{gs}	Gate-Source Charge[4]	V_{DS}=50V	-	1.6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[4]	V_{GS}=10V	-	5	-	nC
$t_{d(on)}$	Turn-on Delay Time[4]	V_{DS}=50V	-	6	-	ns
t_r	Rise Time[4]	I_D=1A	-	8.5	-	ns
$t_{d(off)}$	Turn-off Delay Time[4]	R_G=5.1Ω	-	19	-	ns
t_f	Fall Time[4]	V_{GS}=10V	-	33	-	ns
C_{iss}	Input Capacitance[4]	V_{GS}=0V	-	395	632	pF
C_{oss}	Output Capacitance[4]	V_{DS}=80V	-	77	-	pF
C_{rss}	Reverse Transfer Capacitance[4]	f=1.0MHz	-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.5	1.25	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=3.3A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[4]	I_S=6A, V_{GS}=0V	-	33	-	ns
Q_{rr}	Reverse Recovery Charge[4]	dI/dt=100A/μs	-	26	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-4A	-	-	60	mΩ
		V_{GS}=-6V, I_D=-3A	-	-	98	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-2	-	-4	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-4A	-	10	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-80V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[4]	I_D=-4A	-	25	40	nC
Q_{gs}	Gate-Source Charge[4]	V_{DS}=-50V	-	5.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[4]	V_{GS}=-10V	-	8	-	nC
$t_{d(on)}$	Turn-on Delay Time[4]	V_{DS}=-50V	-	14	-	ns
t_r	Rise Time[4]	I_D=-1A	-	9	-	ns
$t_{d(off)}$	Turn-off Delay Time[4]	R_G=3.3Ω	-	29	-	ns
t_f	Fall Time[4]	V_{GS}=-10V	-	50	-	ns
C_{iss}	Input Capacitance[4]	V_{GS}=0V	-	1140	1824	pF
C_{oss}	Output Capacitance[4]	V_{DS}=-80V	-	205	-	pF
C_{rss}	Reverse Transfer Capacitance[4]	f=1.0MHz	-	15	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.8	3.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-3.3A, V_{GS}=0V	-	-	-1.3	V
t_{rr}	Reverse Recovery Time[4]	I_S=-4A, V_{GS}=0V,	-	55	-	ns
Q_{rr}	Reverse Recovery Charge[4]	dI/dt=-100A/μs	-	153	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 85°C/W at steady state.

4.Guaranteed by design.

5.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

N-Channel

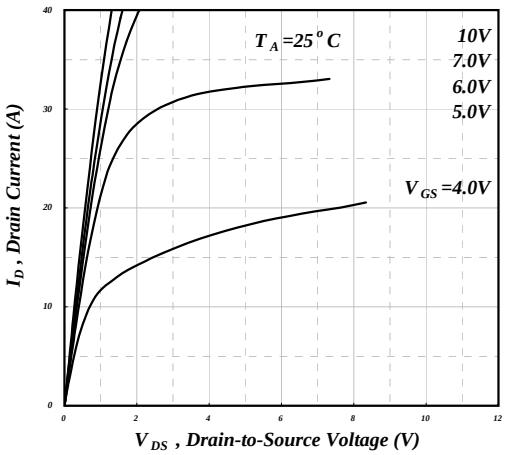


Fig 1. Typical Output Characteristics

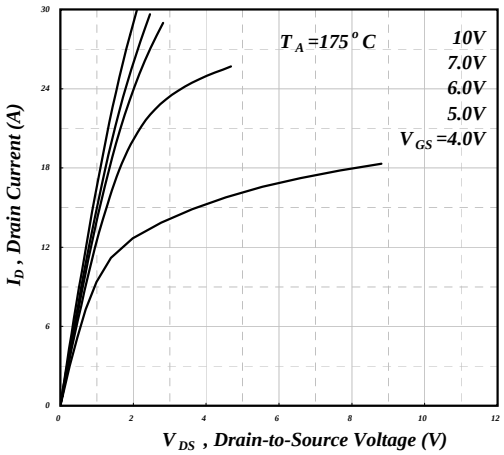


Fig 2. Typical Output Characteristics

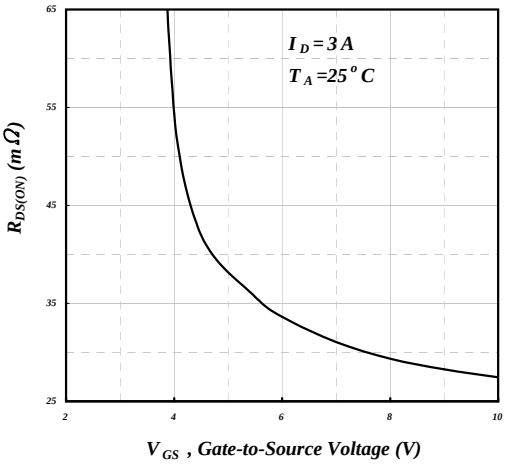


Fig 3. On-Resistance v.s. Gate Voltage

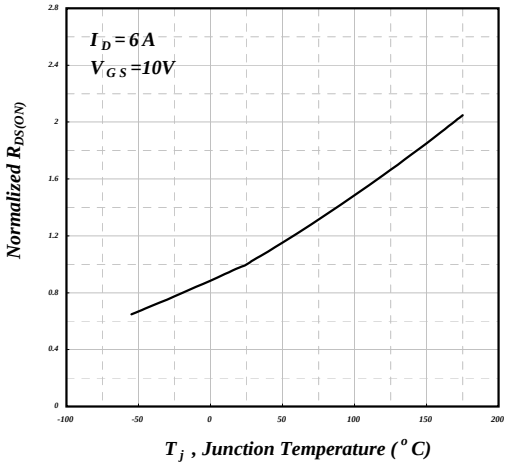


Fig 4. Normalized On-Resistance v.s. Junction Temperature

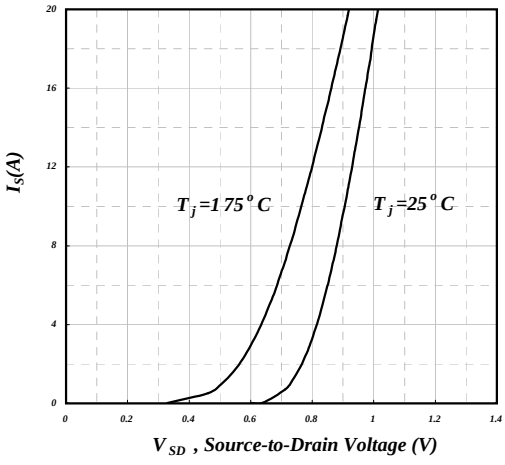


Fig 5. Forward Characteristic of Reverse Diode

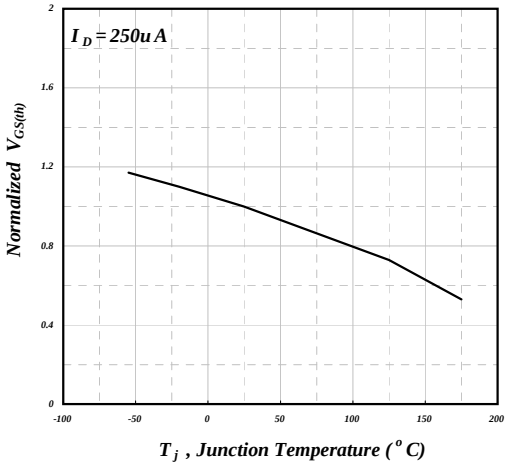


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

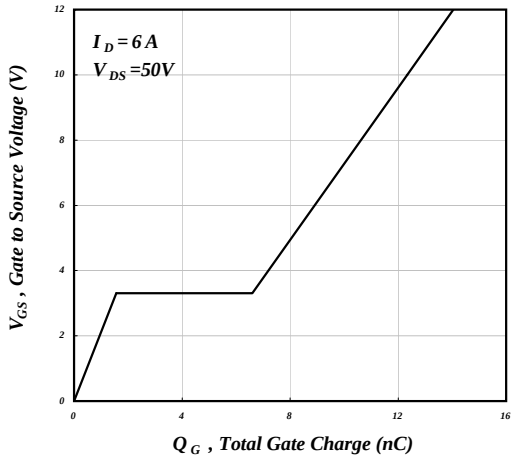


Fig 7. Gate Charge Characteristics

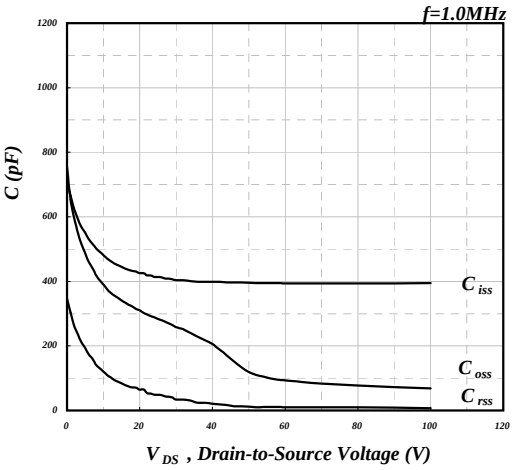


Fig 8. Typical Capacitance Characteristics

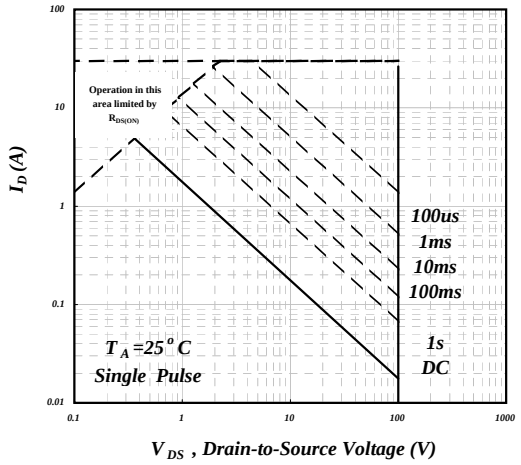


Fig 9. Maximum Safe Operating Area[5]

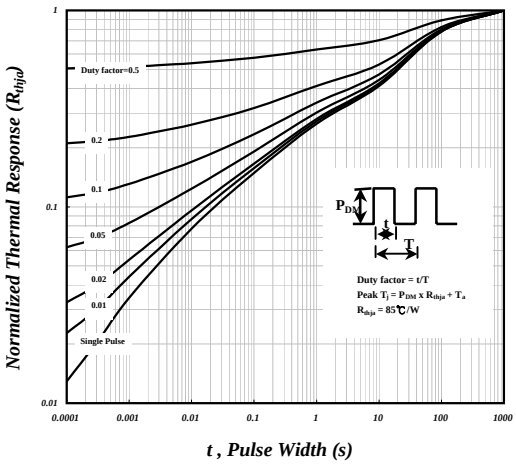


Fig 10. Effective Transient Thermal Impedance

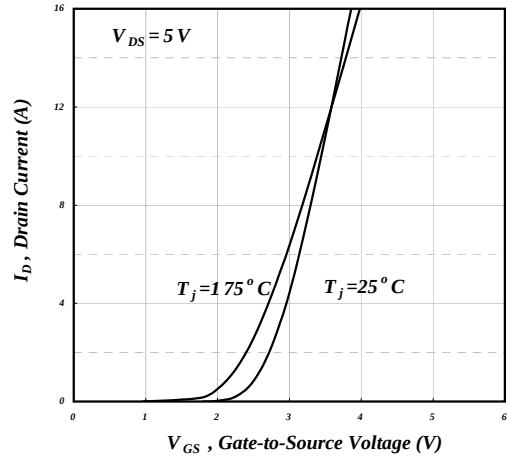


Fig 11. Transfer Characteristics

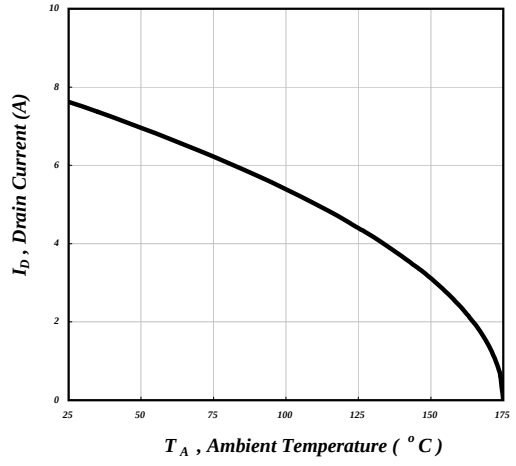


Fig 12. Drain Current v.s. Ambient Temperature

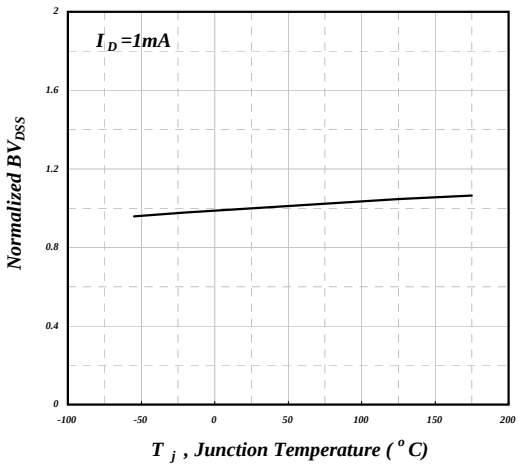


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

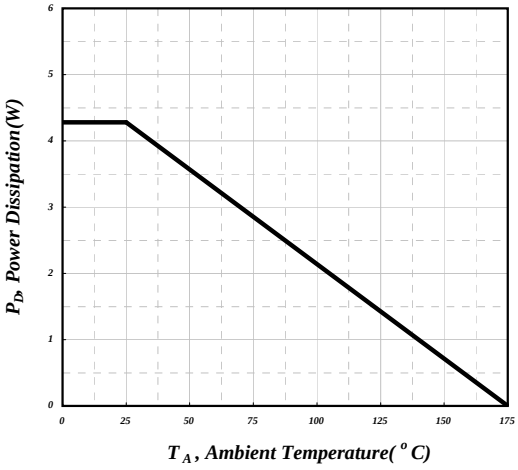


Fig 14. Total Power Dissipation

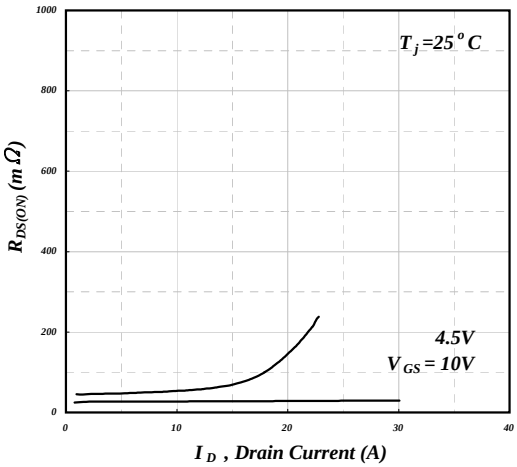


Fig 15. Typ. Drain-Source on State Resistance

P-Channel

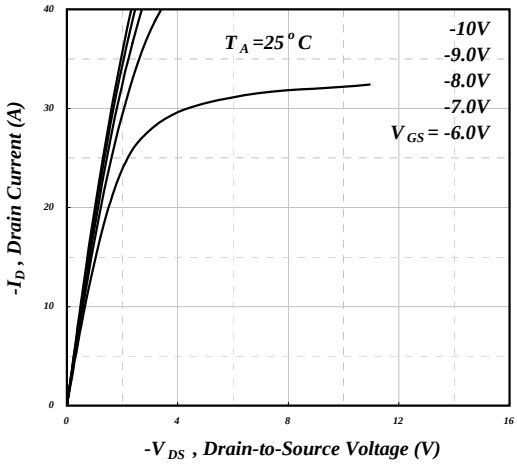


Fig 1. Typical Output Characteristics

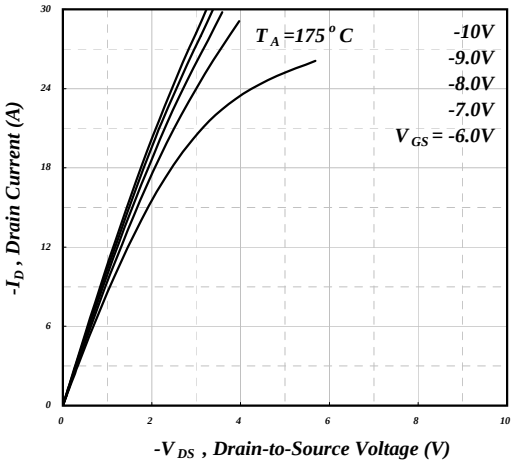


Fig 2. Typical Output Characteristics

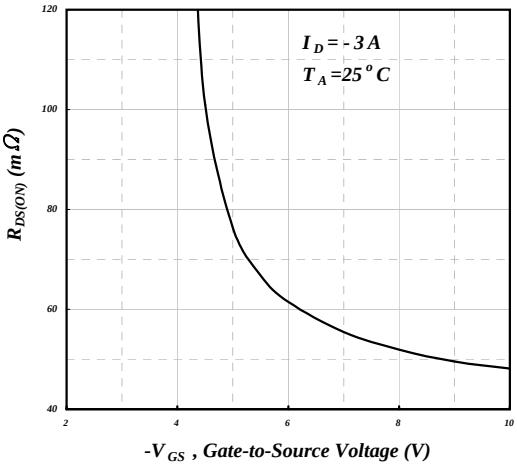


Fig 3. On-Resistance v.s. Gate Voltage

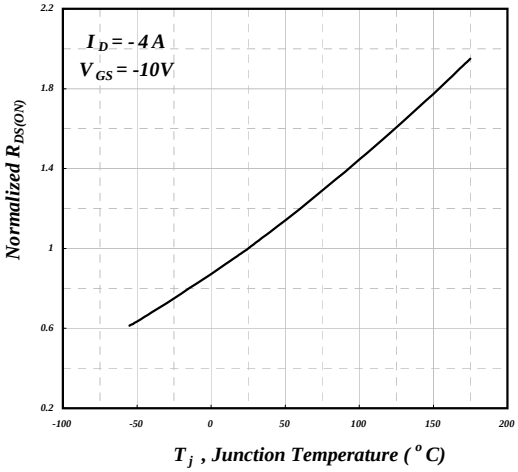


Fig 4. Normalized On-Resistance v.s. Junction Temperature

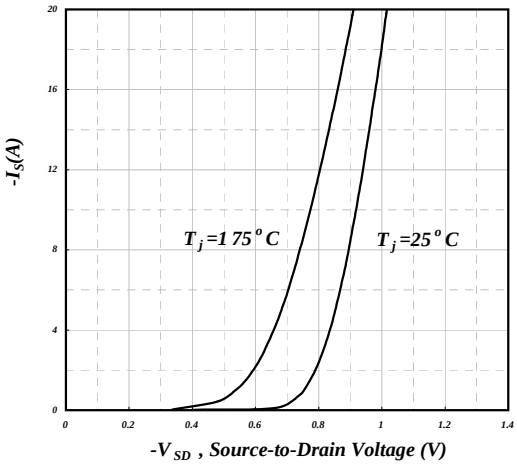


Fig 5. Forward Characteristic of Reverse Diode

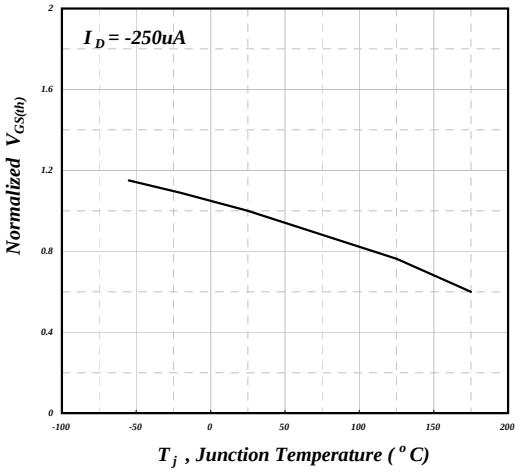


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

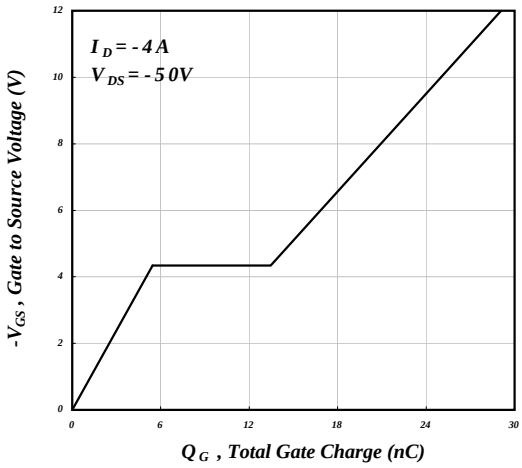


Fig 7. Gate Charge Characteristics

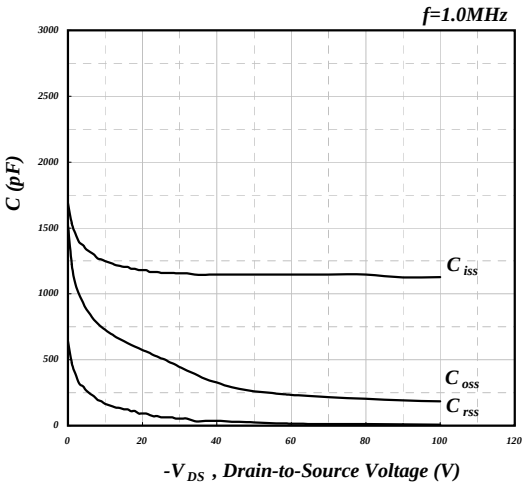


Fig 8. Typical Capacitance Characteristics

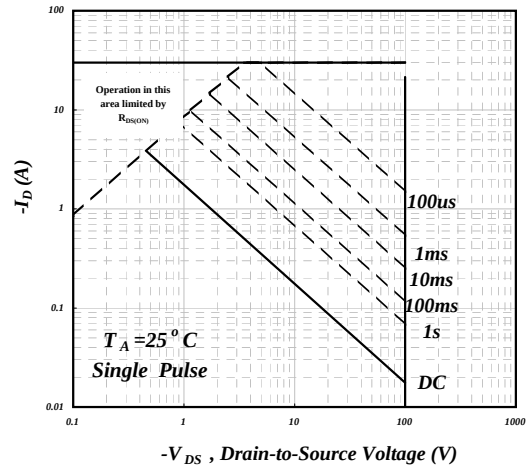


Fig 9. Maximum Safe Operating Area[5]

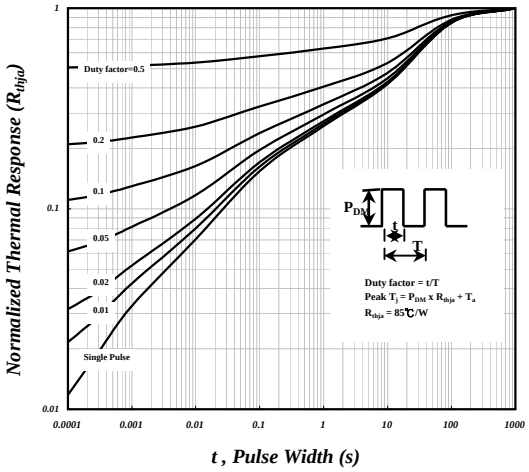


Fig 10. Effective Transient Thermal Impedance

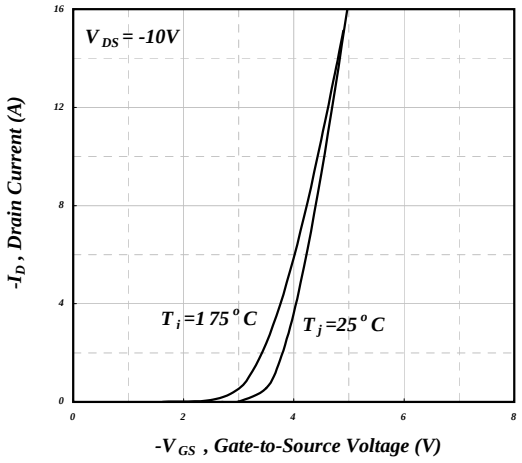


Fig 11. Transfer Characteristics

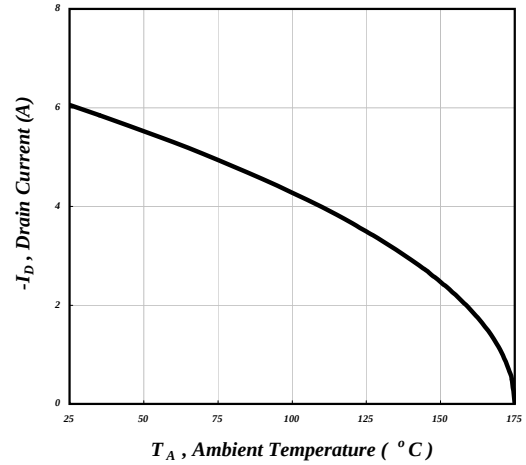


Fig 12. Drain Current v.s. Ambient Temperature

P-Channel

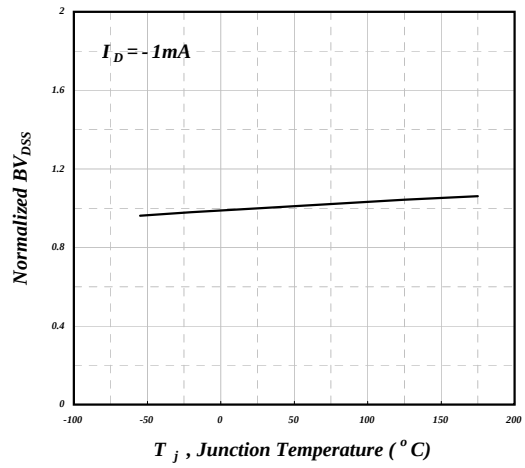


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

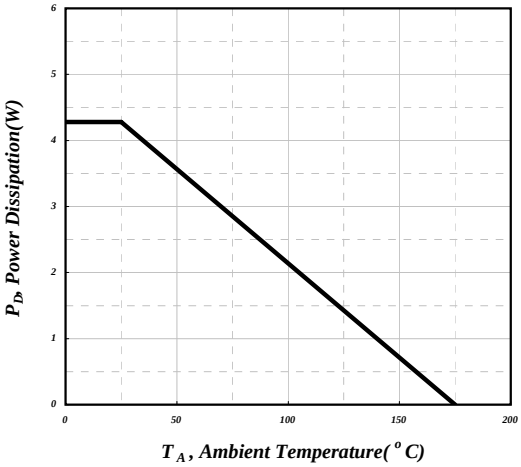


Fig 14. Total Power Dissipation

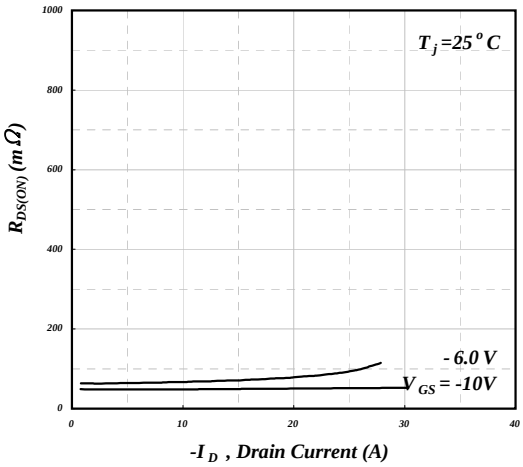
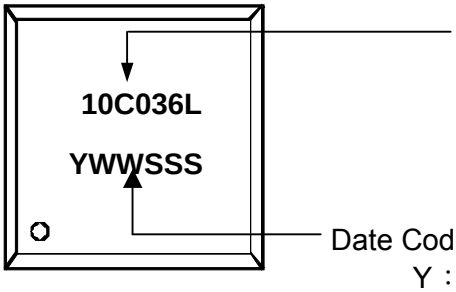
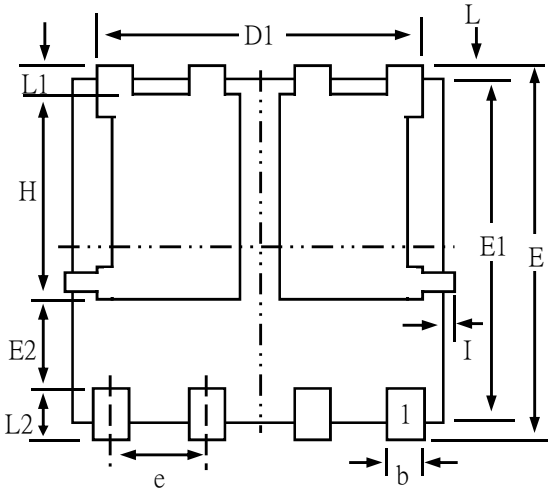


Fig 15. Typ. Drain-Source on State Resistance

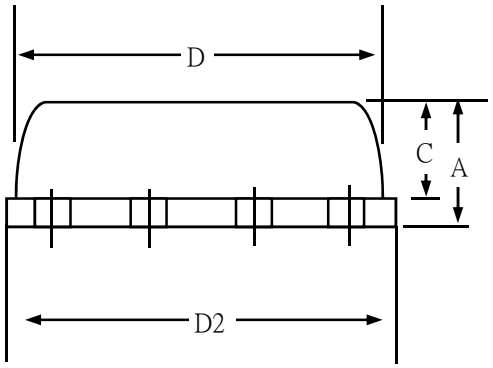
MARKING INFORMATION



Package Outline : PMPAK 5x6 (Dual Pad)



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	1.00	1.20
b	0.34	0.42	0.50
C	0.54	0.76	0.97
D	4.80	4.95	5.10
D1	4.11	4.21	4.31
E	5.90	6.05	6.20
E1	5.60	5.75	5.90
E2	1.60 (ref.)		
e	1.27 (ref.)		
L	0.05	0.15	0.25
L1	0.60 (ref.)		
L2	0.60 (ref.)		
H	3.60 (ref.)		
I	0.15 (ref.)		
D2	4.80	5.15	5.50

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Draw No. M2-1MT8-G-v02

PMPAK5X6(Dual Pad,左右) FOOTPRINT：