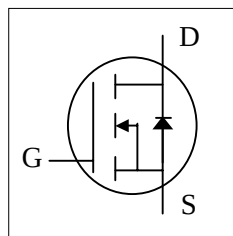


- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

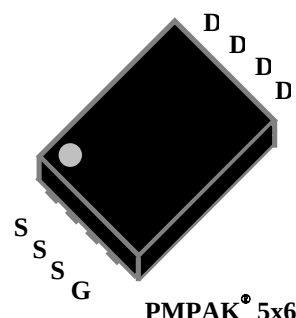


BV_{DSS}	40V
$R_{DS(ON)}$	9.5m Ω
I_D	46A

Description

XP0904 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D@T_C=25^\circ\text{C}$	Drain Current (Chip)	46	A
$I_D@T_A=25^\circ\text{C}$	Drain Current, V_{GS} @ 10V ³	17.5	A
$I_D@T_A=70^\circ\text{C}$	Drain Current, V_{GS} @ 10V ³	14	A
I_{DM}	Pulsed Drain Current ¹	160	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	34.7	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy ⁴	28.8	mJ
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.6	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W

Electrical Characteristics@T_J=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	-	-	9.5	mΩ
		V _{GS} =4.5V, I _D =20A	-	-	15	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	-	45	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =40V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =20A	-	9	14.4	nC
Q _{gs}	Gate-Source Charge	V _{DS} =20V	-	2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	6	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =20V	-	6.5	-	ns
t _r	Rise Time	I _D =1A	-	6.5	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	20	-	ns
t _f	Fall Time	R _D =20Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	680	1080	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	160	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	95	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.1	4.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =10A, V _{GS} =0V,	-	22	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	16	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec, 60°C/W at steady state.
- 4.Starting T_J=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω , I_{AS}=24A.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

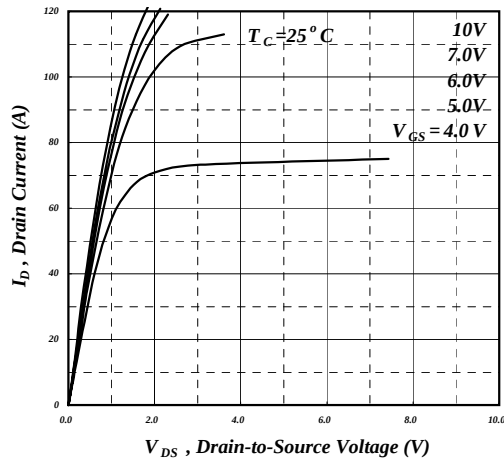


Fig 1. Typical Output Characteristics

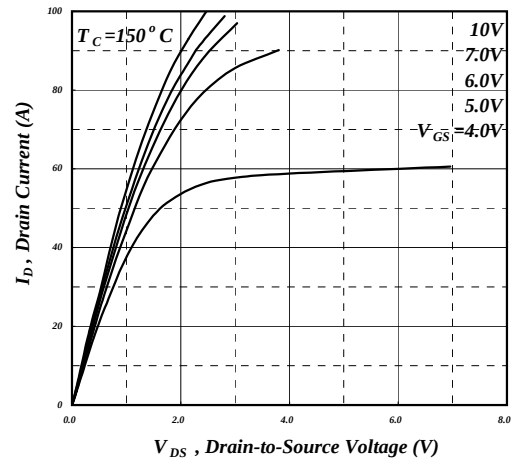


Fig 2. Typical Output Characteristics

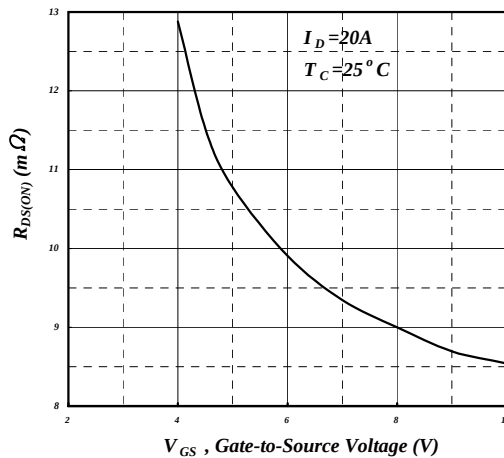
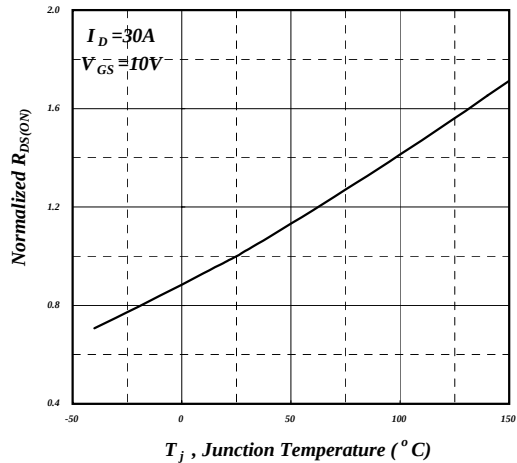
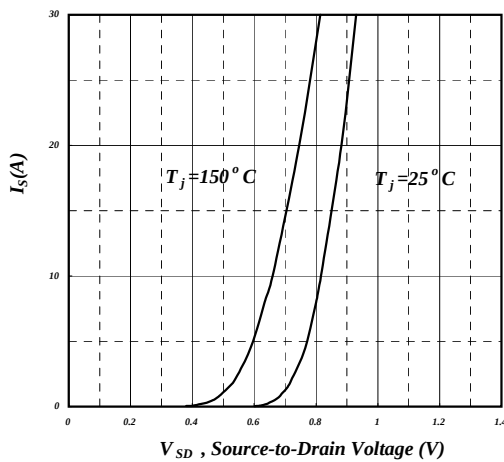


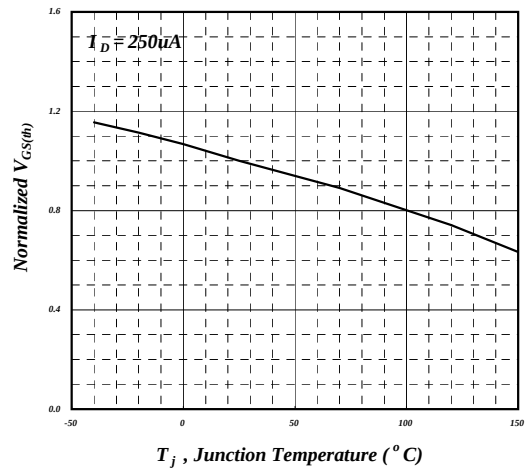
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

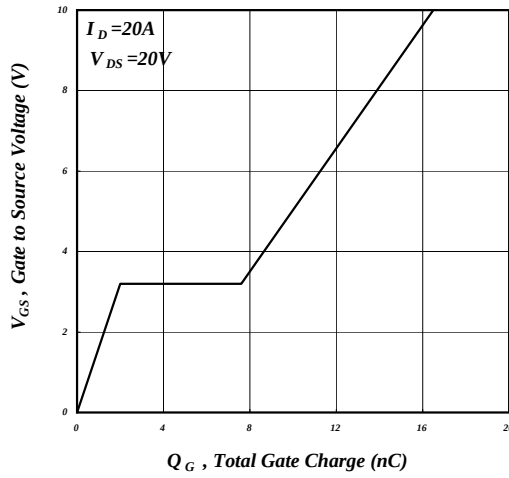


Fig 7. Gate Charge Characteristics

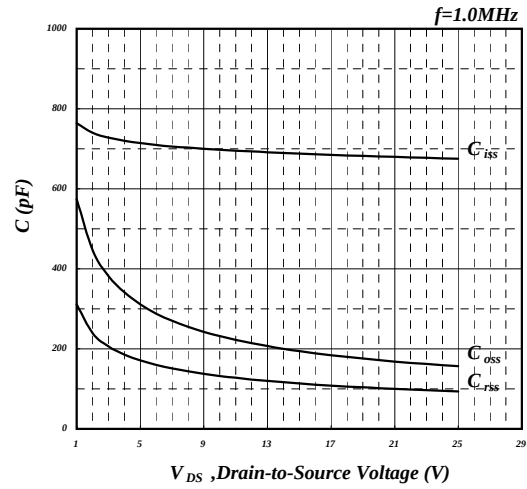


Fig 8. Typical Capacitance Characteristics

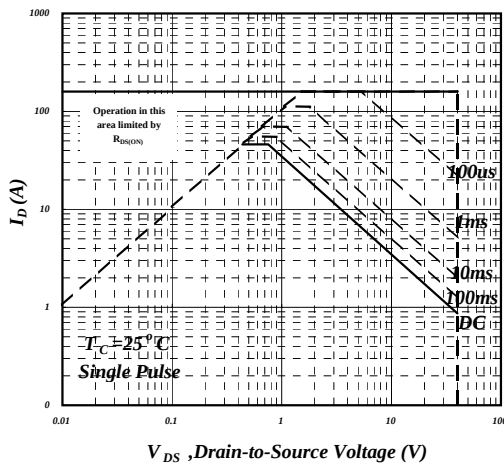


Fig 9. Maximum Safe Operating Area

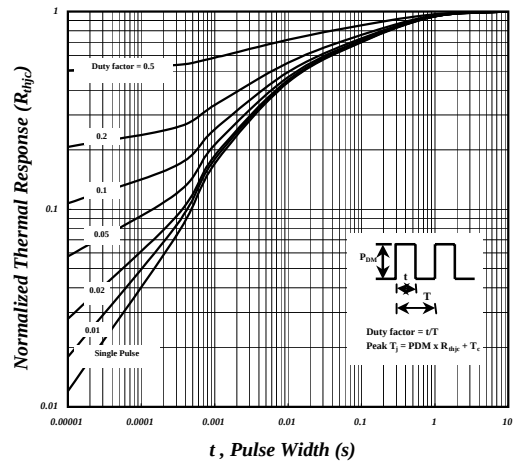


Fig 10. Effective Transient Thermal Impedance

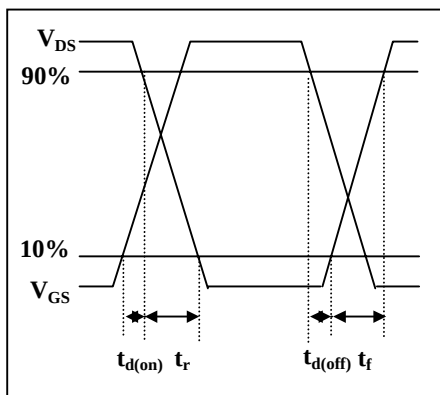


Fig 11. Switching Time Waveform

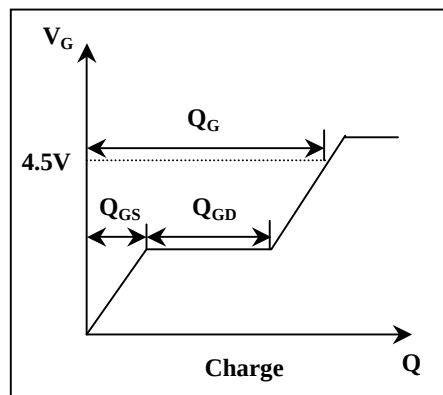
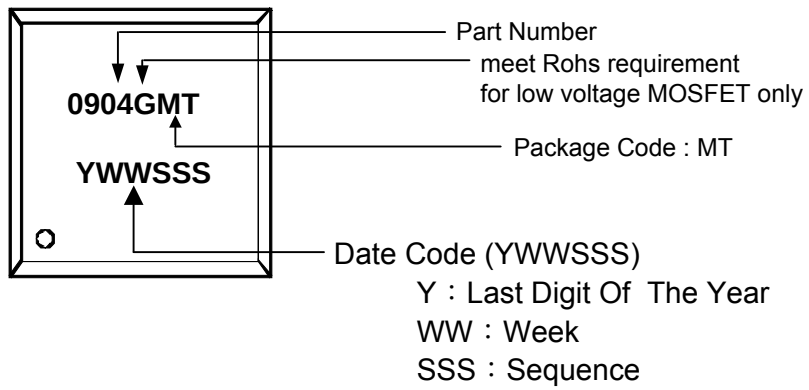
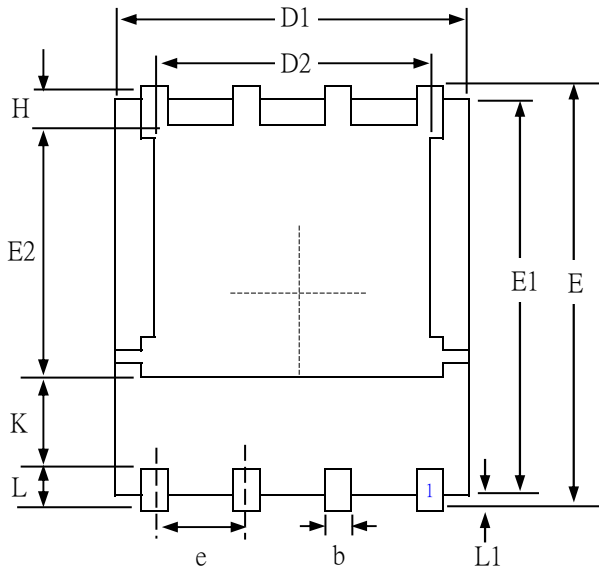


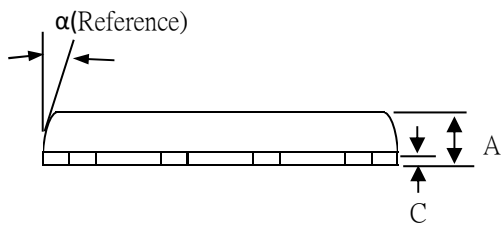
Fig 12. Gate Charge Waveform

MARKING INFORMATION

Package Outline : PMPAK 5x6



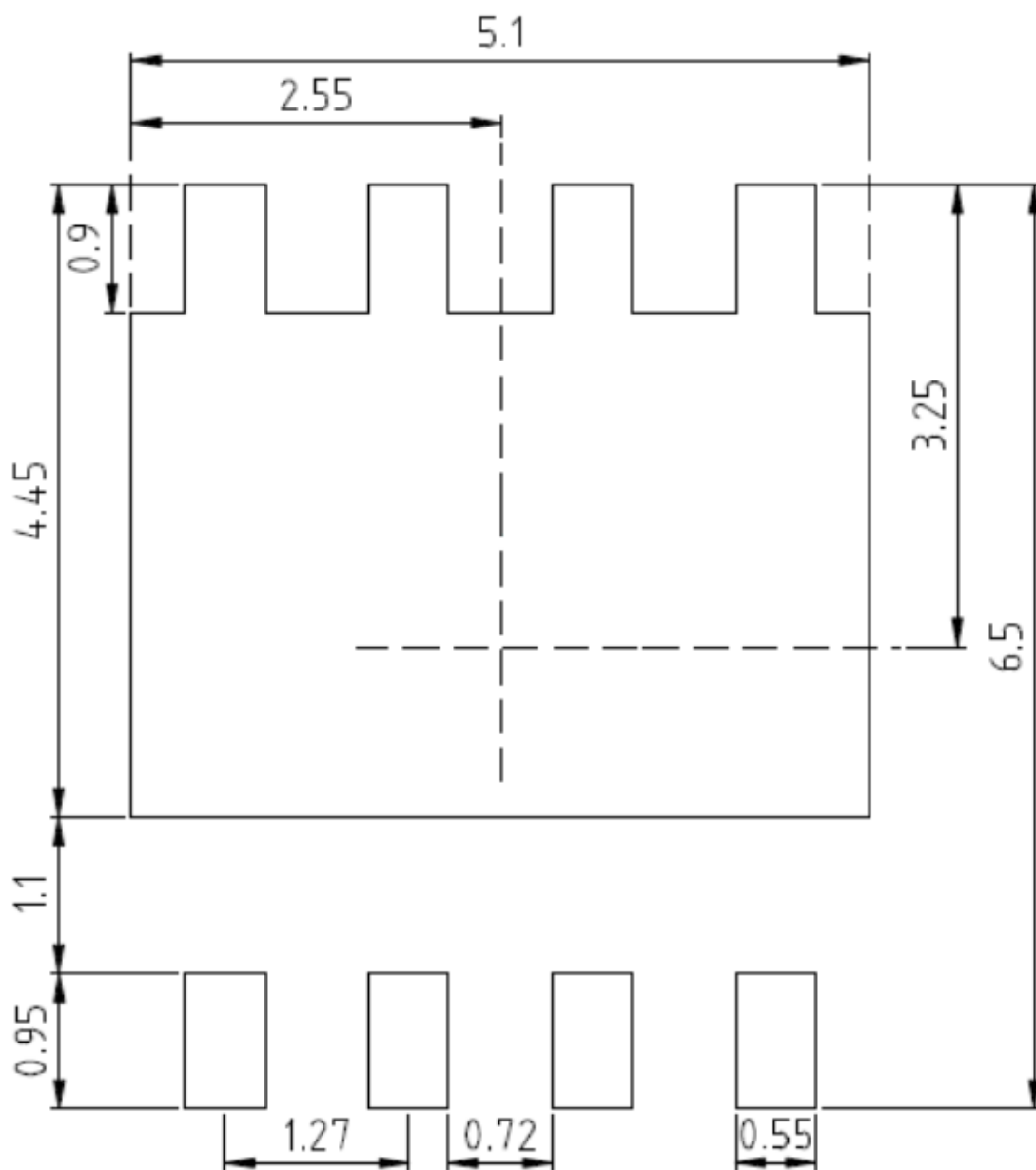
BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
$\alpha(\text{Ref.})$	0°	—	12°

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

PMPAK 5X6(E-TYPE) FOOTPRINT :



UNIT: mm