XDPS2201E Hybrid-flyback controller

Datasheet

Features

- Digital controller for DC-DC hybrid-flyback in DSO-14 (150mil) package
- Novel ZVS hybrid-flyback (asymmetrical half-bridge) topology for ultra-high system efficiency and high-density design
- Integrated half-bridge (HB) gate drivers supporting both GaN and Si switches
- 600 V high voltage start-up cell for fast VCC charging
- Burst mode operation control for lowest no-load stand-by power
- Configurable parameters for protection modes and system performance
- Pb-free lead plating, halogen-free (according to IEC61249-2-21), RoHS compliant
- Peak current mode control for robust and fast input and load control
- ZVS operation of high-side and low-side switch (with ZVS pulse insertion in DCM)
- Configurable multimode operation for improved average and light load efficiency

Potential applications

- Battery charger
- Lighting
- Power supply with high density/wide output voltage range
- High power density SMPS

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The XDPS2201E PWM controller is a highly integrated, multimode DC-DC hybrid-flyback controller supporting extra wide output voltage range designs.

Ordering information

Product name	Marking	Ordering code	Firmware version	Package
XDPS2201E	XDPS2201E	SP006063851	4.1.5	PG-DSO-14

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1 Pin configuration and functionality

The pin configuration is shown in the figure below and the functions are described in the following table.

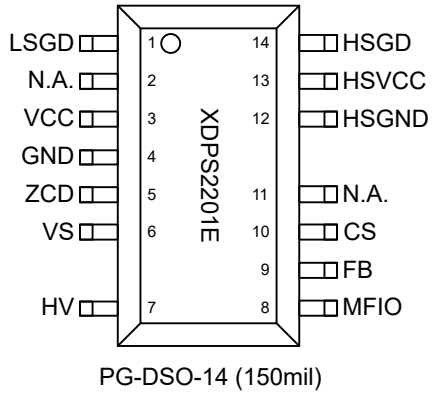

Figure 1 XDPS2201E pin configuration

Table 1 Pin definitions and functions

Symbol	Pin	Type	Function
LSGD	1	O	**Hybrid-flyback low-side gate driver** This pin drives the low-side transistor of the hybrid-flyback half-bridge via a resistor.
N.A.	2		**Not available** This pin is internally connected but not used and should be connected to GND.
VCC	3	I	**Power supply** This pin supplies the IC. During start-up VCC is supplied internally from the AC via the HV pin, while during normal operation VCC is supplied from the auxiliary winding to the hybrid-flyback stage.
GND	4	O	**Ground** Ground level of the IC for supply voltage, gate drive and sense signals.
ZCD	5	I	**Hybrid-flyback zero crossing detection** This pin provides zero-crossing detection after low-side gate driver is turned off, during pause phase in skip cycle and burst mode. Furthermore, the reflected output voltage at auxiliary winding can be measured during low-side gate driver turn-on phase.
VS	6	I	**Bus voltage sense** This pin is connected to a high impedance resistor divider for bus voltage sensing.
HV	7	I	**High voltage input** The HV pin is connected to the input AC voltage. An internal HV start-up cell is used for initial VCC charging.

(table continues...)

Table 1 (continued) Pin definitions and functions

Symbol	Pin	Type	Function
MFIO	8	I	**Multi-functional input output** This pin has different function depending on configuration. One example is to detect ambient temperature using an external NTC resistor connected between MFIO and GND. Furthermore, UART communication for parameter configuration and failure mode reporting is provided by this pin.
FB	9	I	**Feedback** Feedback signal indicating the required output current, typically connected to optocoupler for secondary side feedback.
CS	10	I	**Hybrid-flyback current sense** Input pin for current sensing during the hybrid-flyback high-side gate driver turn-on phase.
N.A.	11	O	**Not available** This pin is internally connected to a signal. It must be left open in application and shall NOT be connected to any external circuitry.
HSGND	12	I	**High-side ground** Ground reference node for hybrid-flyback floating high-side driver domain.
HSVCC	13	I	**High-side power supply** Power supply input for hybrid-flyback floating high-side driver domain.
HSGD	14	O	**High-side gate driver** This pin drives the high-side transistor of the hybrid-flyback half-bridge from the floating driver domain.

2 Representative block diagram

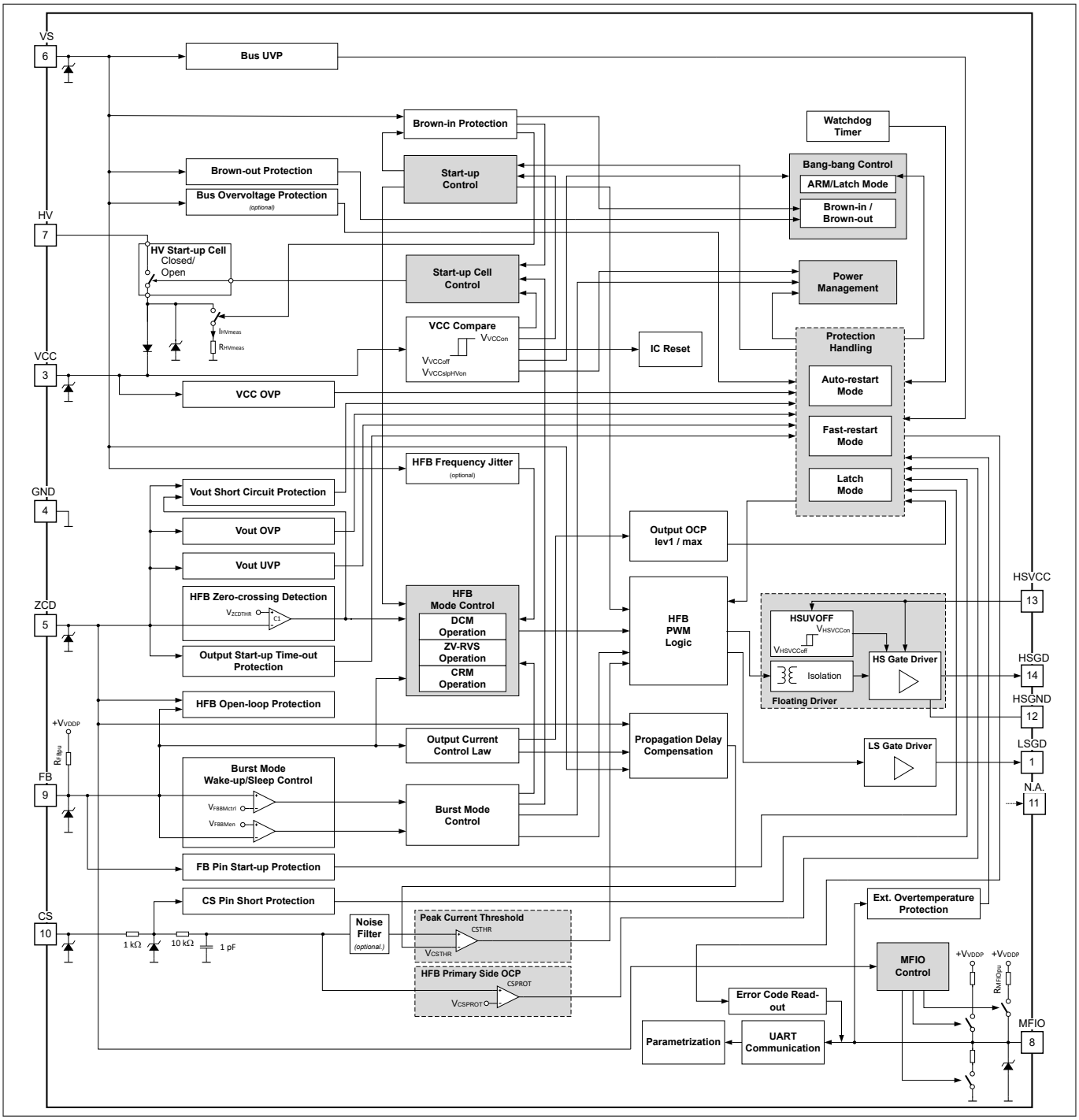

Figure 2 Block diagram

3 Introduction

The XDPS2201E PWM controller is a highly integrated, multimode DC-DC hybrid-flyback (HFB) controller. The controller enables reduction of external parts and optimizes performance. It serves applications with fixed output voltage and offers even more benefits for applications with wide output voltage range.

The system efficiency can further be increased using Infineon CoolMOS™, CoolGaN™ Transistor, CoolGaN™ Transistor Dual and OptiMOS™ transistors.

Figure 3, Figure 4 and Figure 5 show the potential application schematic using CoolGaN™ Transistor Single, CoolGaN™ Transistor Dual and OptiMOS™ transistor.

Figure 6 and Figure 7 show the potential application schematic using CoolMOS™ and OptiMOS™ transistors.

3 Introduction

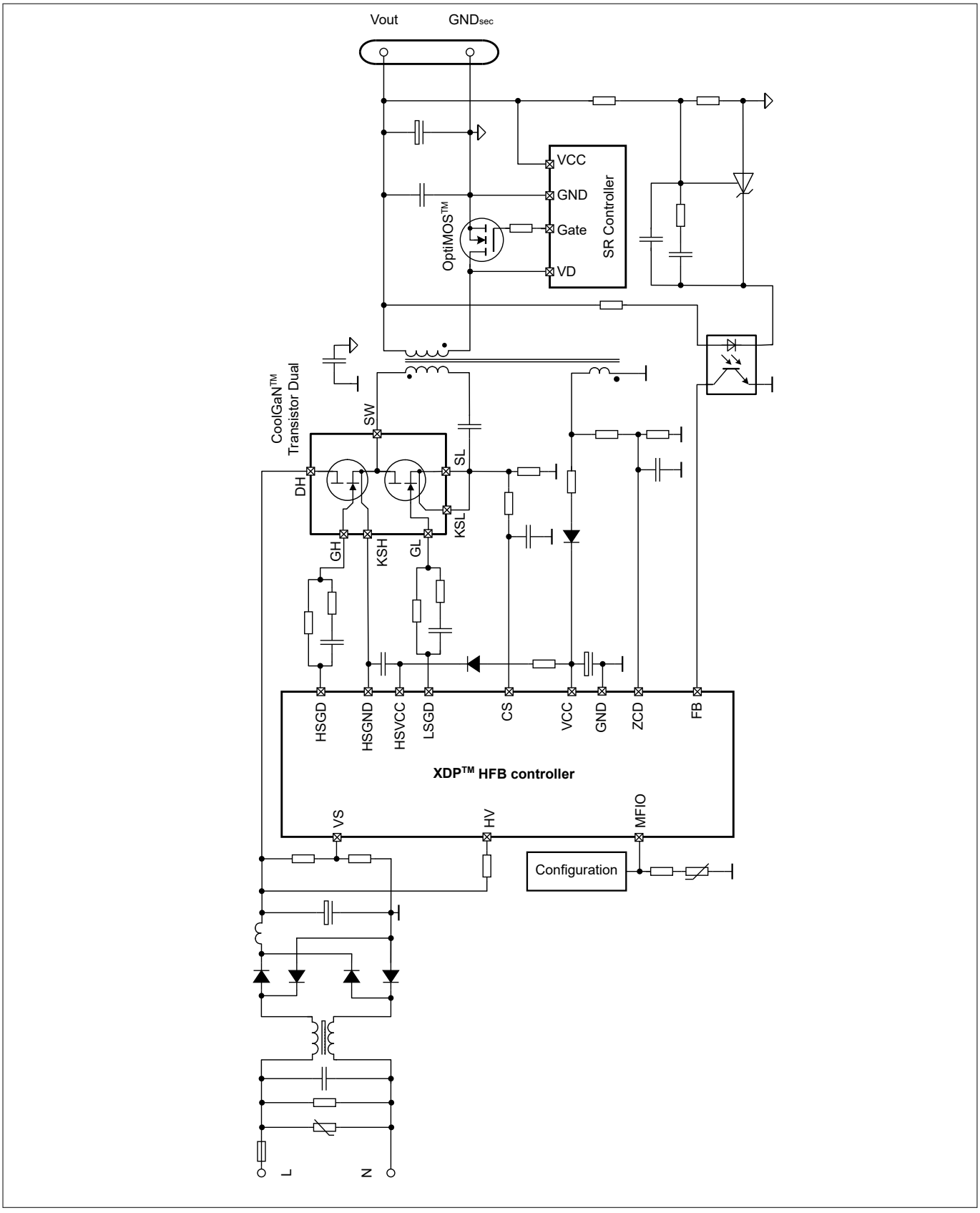

Figure 3 Typical SMPS application in combination with CoolGaN™ Transistor Dual

3 Introduction

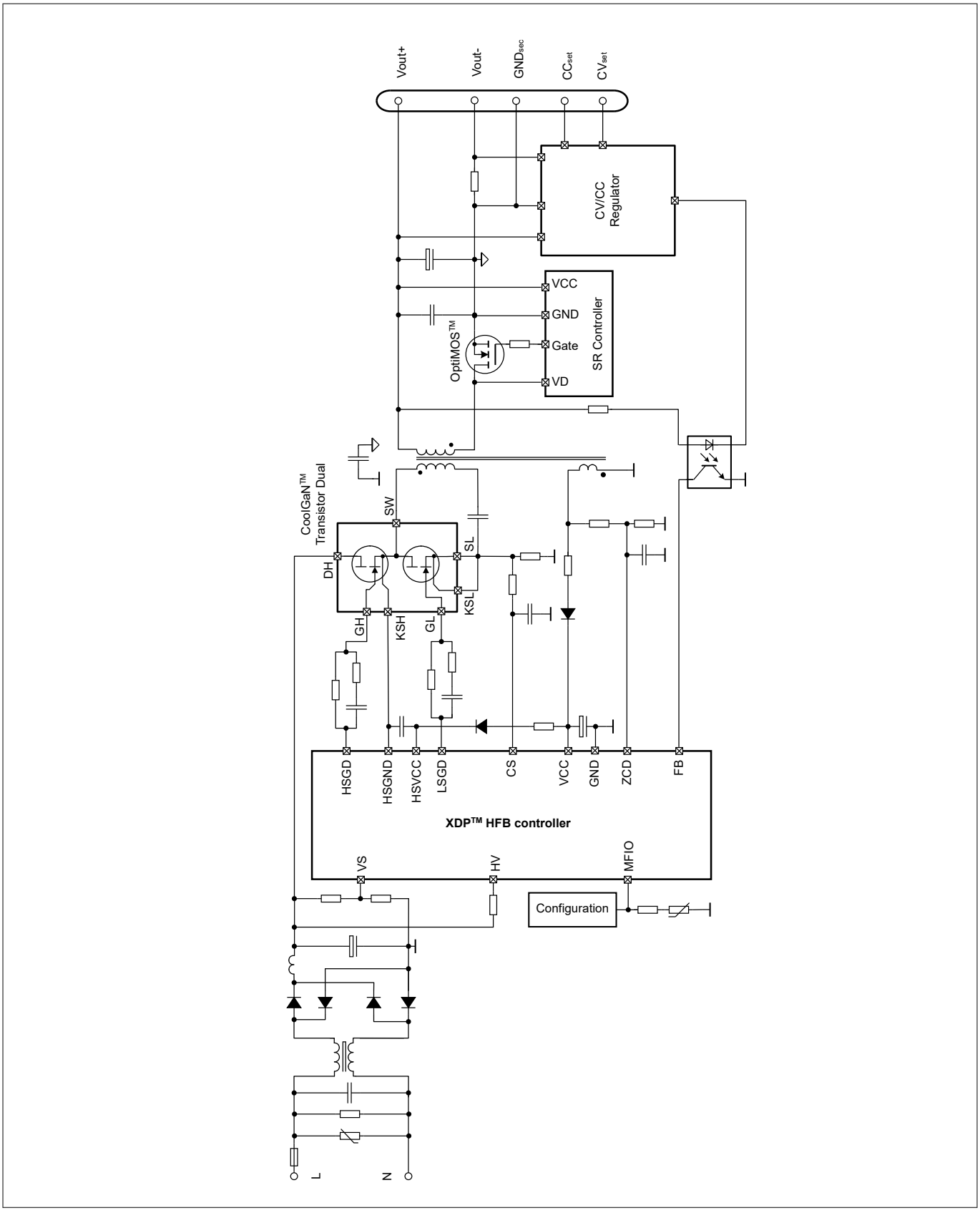

Figure 4 **Typical battery charger application in combination with CoolGaN™ Transistor Dual, single stage**

3 Introduction

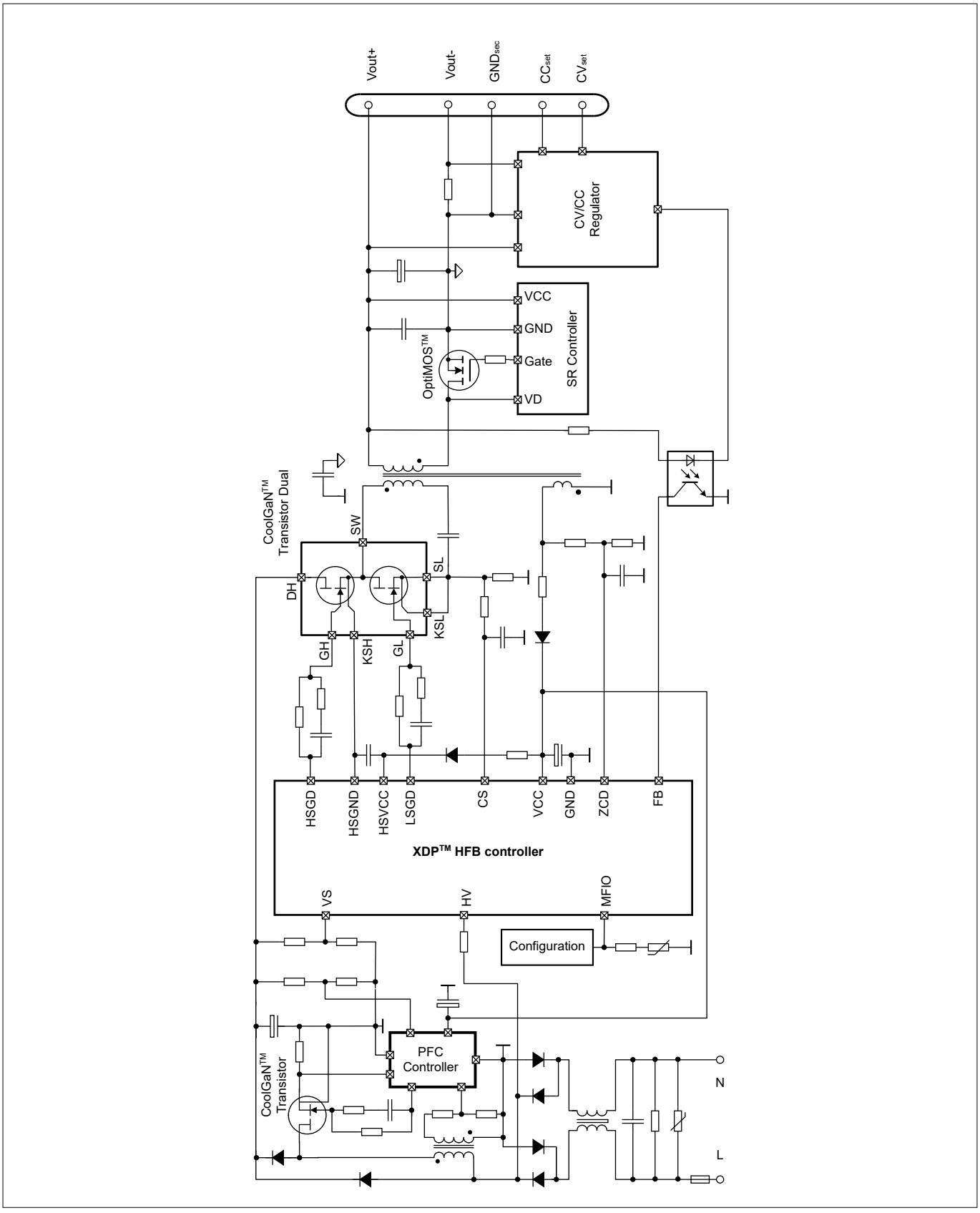

Figure 5 **Typical battery charger and lighting application in combination with CoolGaN™ Transistor Single and CoolGaN™ Transistor Dual, with external PFC**

3 Introduction

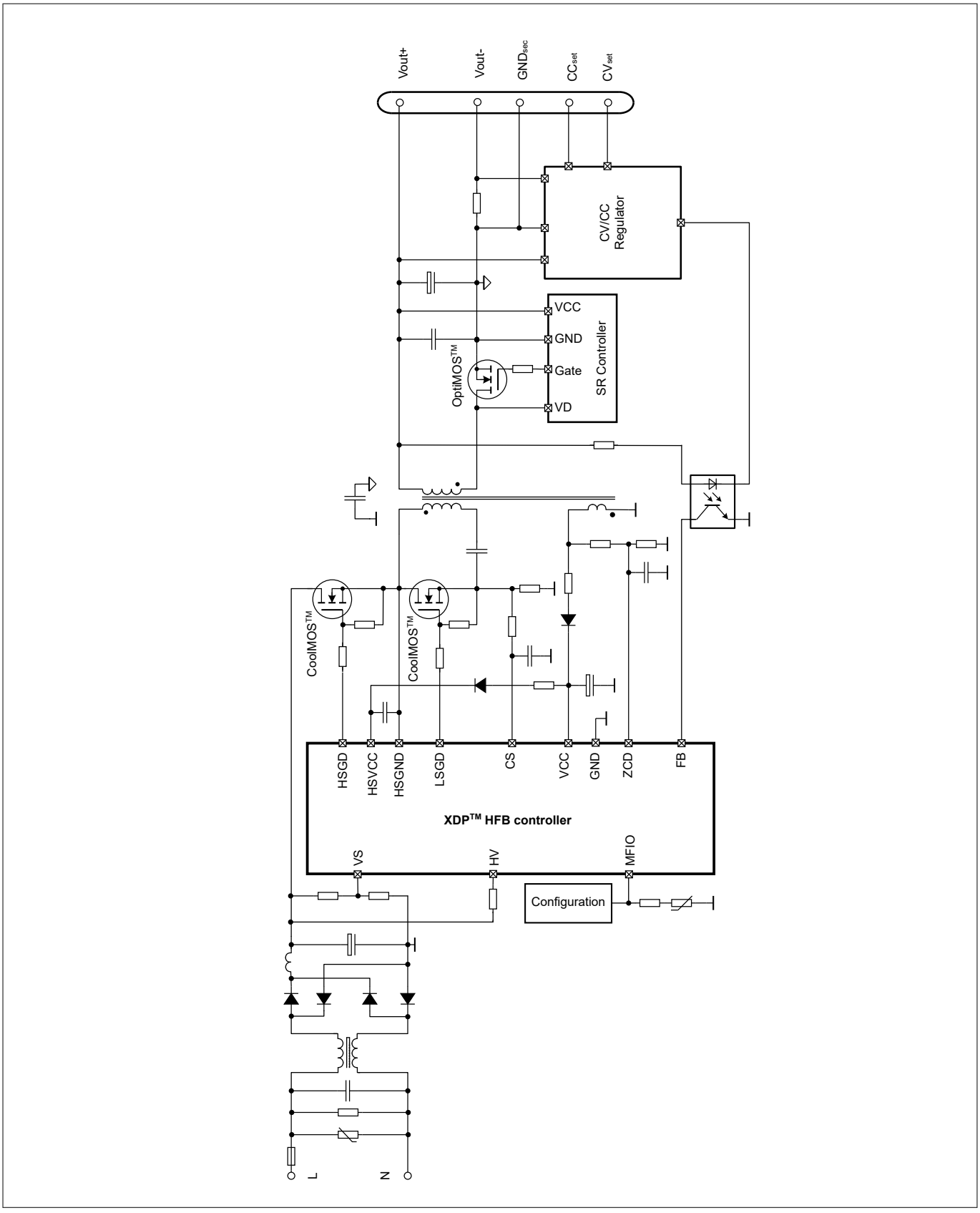

Figure 6 **Typical battery charger application in combination with CoolMOS™ transistors, single stage**

3 Introduction

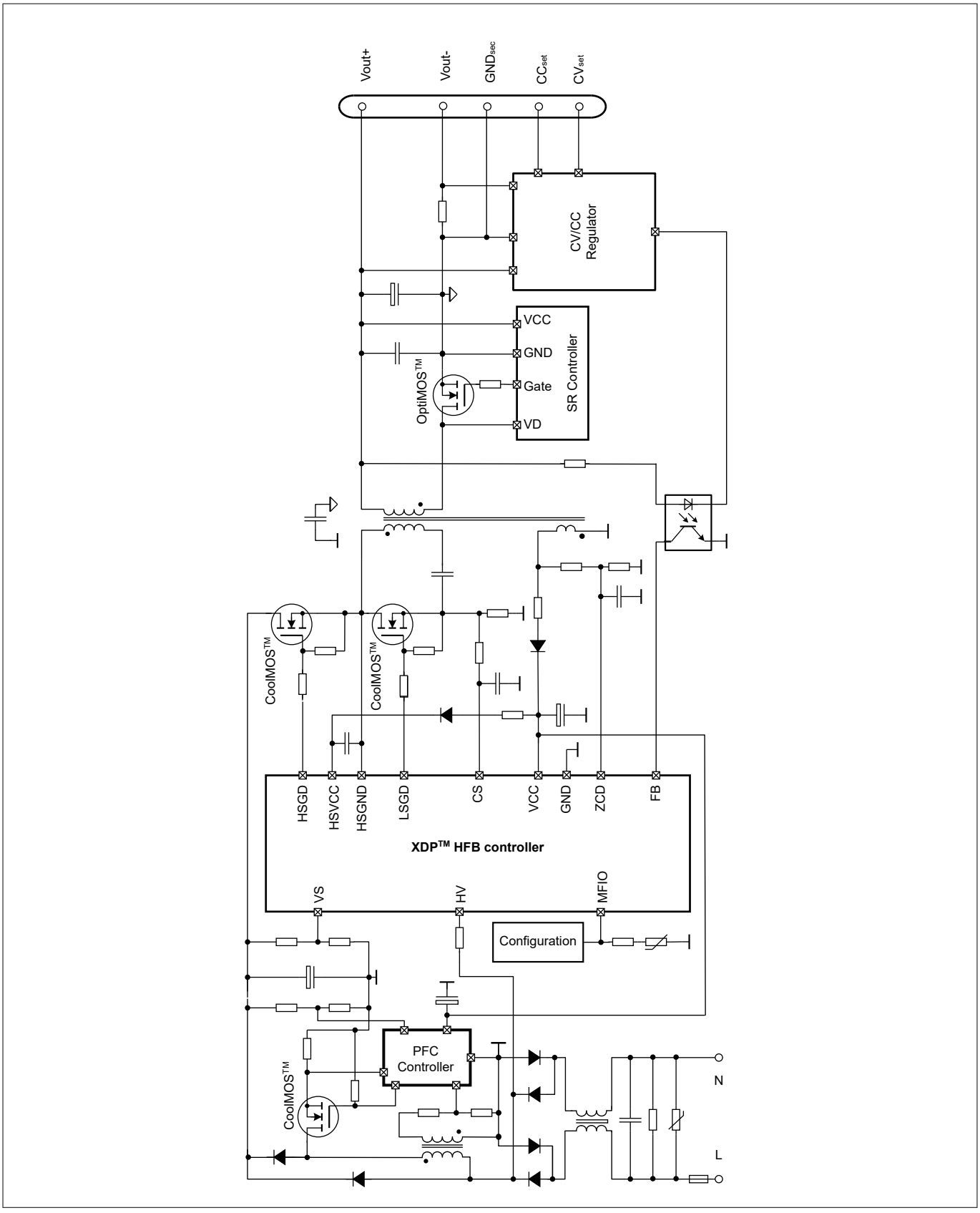

Figure 7 **Typical battery charger and lighting application in combination with CoolMOS™ transistors, with external PFC**

4 Functional description

4.1 VCC power supply and high voltage start-up cell management

The VCC supply management ensures a reliable and robust IC operation. Depending on the operation mode of the control IC, the power supply management unit runs in different ways for VCC supply, which are described as in the sequel.

4.1.1 VCC capacitor charge-up and start-up sequence

At VCC start-up, the capacitor C_{VCC} is charged by the internal HV start-up cell via HV pin (see Figure 8). The internal HV start-up cell is turned on when V_{VCC} is lower than the IC deactivation voltage threshold V_{VCCoff}. Once the voltage at pin VCC exceeds the threshold V_{VCCon} at time t_0, the HV start-up cell is turned off and the IC starts its operation (see Figure 9).

At time t_1, the IC checks the start-up conditions.

Following conditions for proper start-up need to be fulfilled to start the hybrid-flyback operation at time t_2 (hybrid-flyback switching is indicated by signal V_{HBGD}):

1. Brown-in (BI) conditions: $V_{bus} > V_{inbi}$ (see Chapter 4.3.2.4)
2. No input overvoltage: $V_{bus} < V_{busovp}$ (see Chapter 4.1.1)
3. Feedback signal in regulation range: $V_{FB} > V_{FBBMctrl}$
4. No overtemperature condition when the MFIO pin is configured for overtemperature protection (OTP): $R_{MFIO} > R_{MFIOOTPrel}$. (see Chapter 4.3.2.13)

If the conditions are met within the time period t_{HVbito}, the hybrid-flyback starts switching and the external Vcc self-supply takes over the IC supply. In case one of those conditions is not met within the time period t_{HVbito}, the IC enters bang-bang mode (see Chapter 4.1.2).

Once the start-up conditions are fulfilled, the hybrid-flyback starts to operate. Figure 9 shows typical start-up.

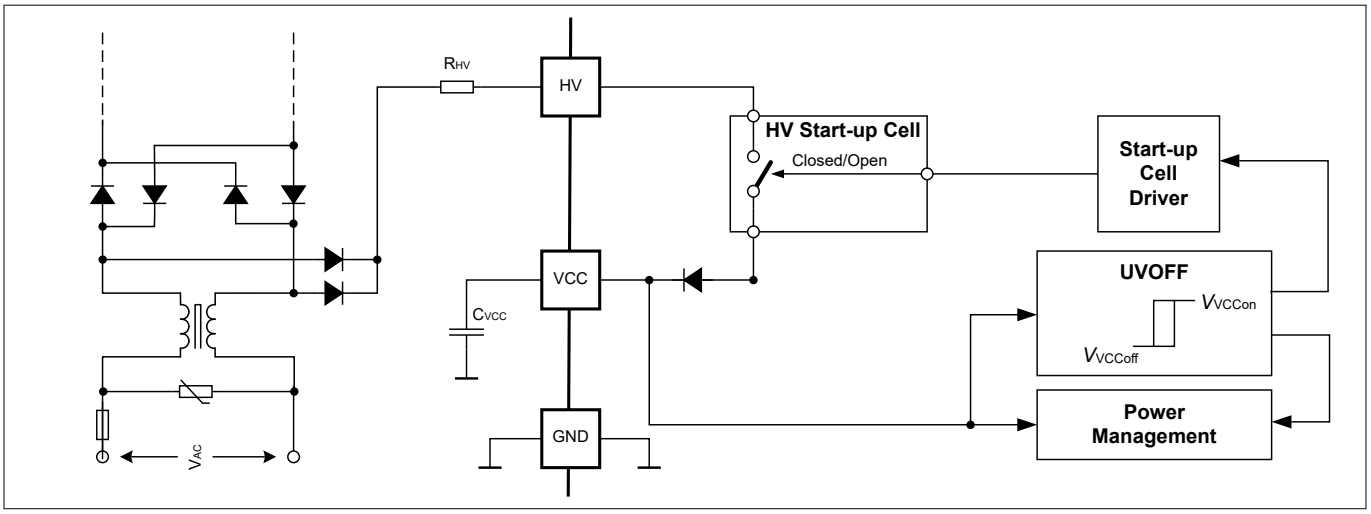

Figure 8 HV control for start-up

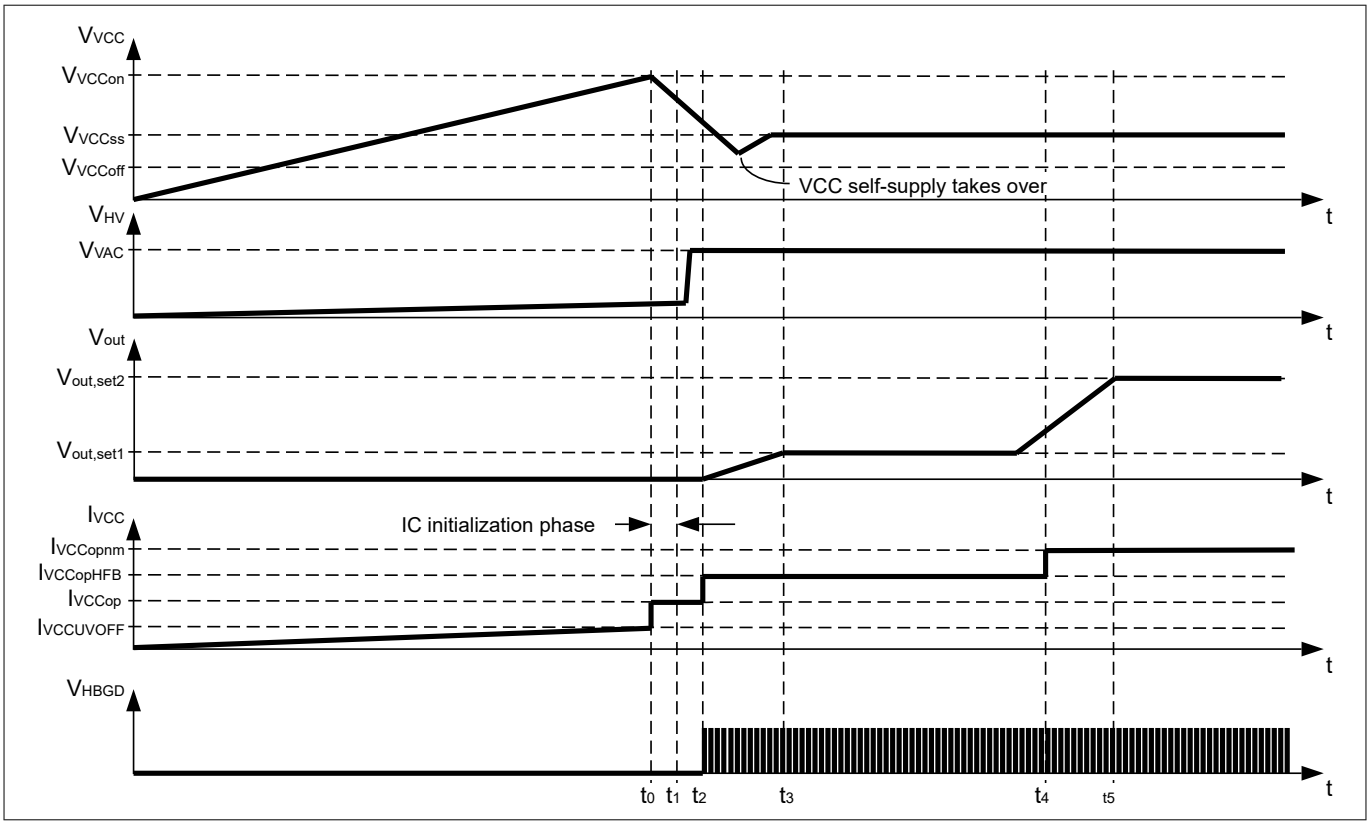

Figure 9 Typical start-up sequence

4.1.2 Bang-bang mode operation during brown-in phase

To support a fast activation as soon as brown-in condition is fulfilled, the VCC voltage is kept at a high level. A bang-bang mode operation for the start-up check phase ensures a high VCC level.

For example, the IC enters a sleep mode with reduced current consumption I_{VCCBB} after a brown-out (BO) event. Once the AC is available, the HV start-up cell turns on and charges up the VCC voltage to the threshold V_{VCCon}. Once the V_{VCC} reaches V_{VCCon}, the IC gets active for brown-in detection. If AC input voltage is high enough, the IC detects the brown-in condition.

4.1.3 Bang-bang mode during protection mode operation

In auto-restart operation, the HV start-up cell is regularly turned on after a time period $t_{ARMbase}$ and turned off when reaching VCC pin voltage threshold V_{VCCon}. During this bang-bang mode operation the VCC is kept at a high level to support a proper restart operation after the auto-restart time t_{ARM} is expired (see Figure 10).

In latch mode operation, the HV start-up cell is turned on at VCC pin voltage threshold $V_{VCCslpHVon}$ and turned off when reaching VCC pin voltage threshold V_{VCCon} (see Figure 11). A reset can only be achieved when the VCC voltage drops below the threshold V_{VCCoff}, for example, by disconnecting the AC line.

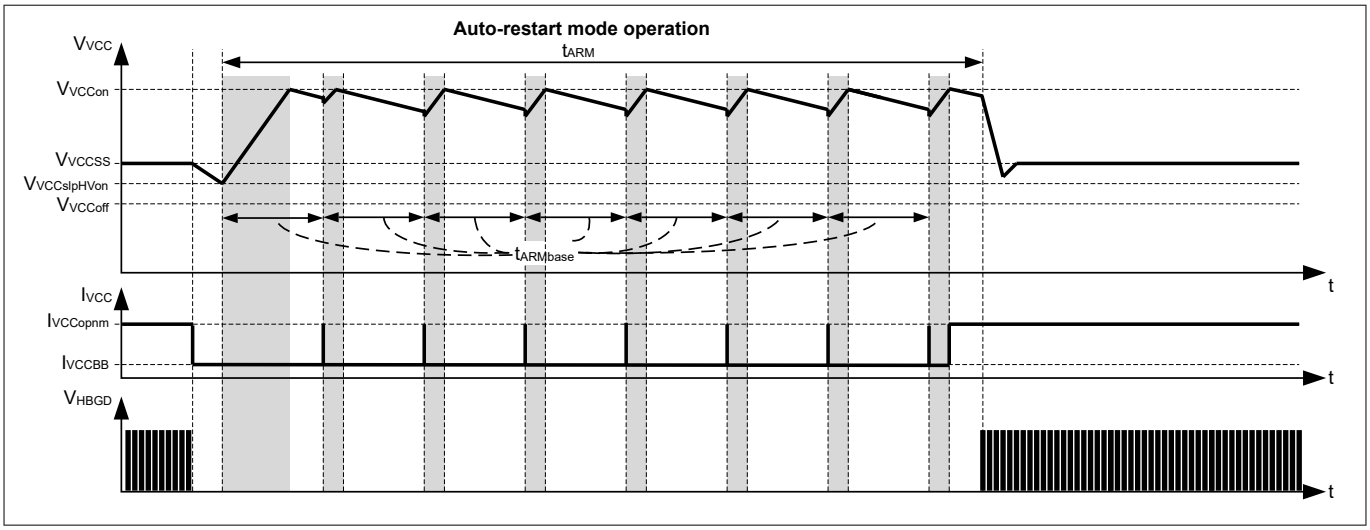

Figure 10 Auto-restart mode operation

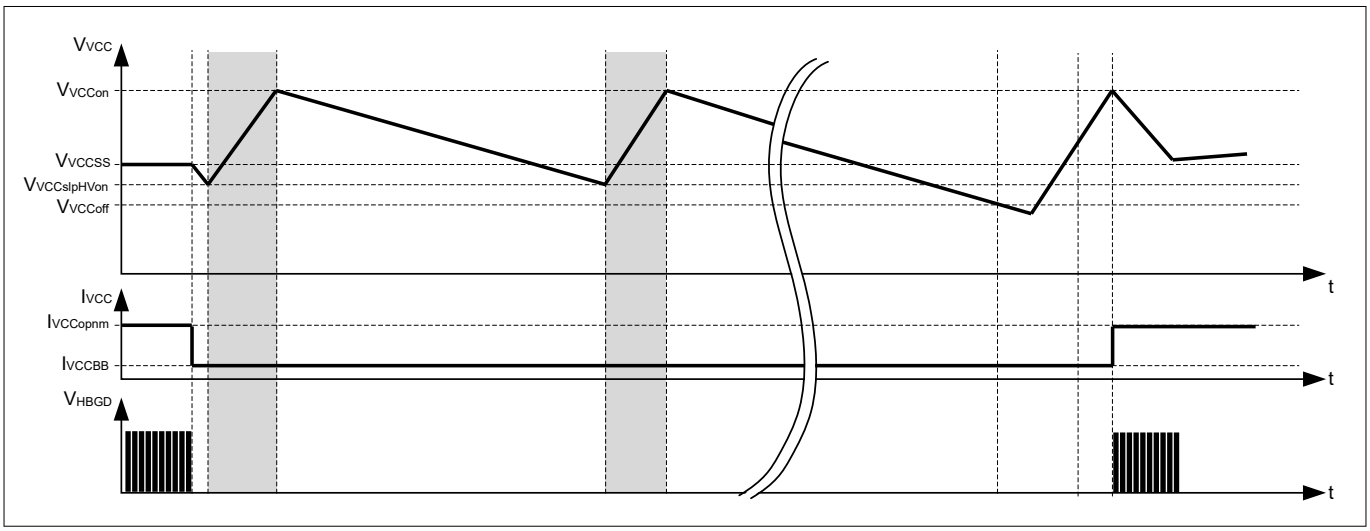

Figure 11 Latch mode operation

4.1.4 VCC supply during burst mode operation

During burst mode (BM) operation, the IC enters repeatedly a power saving mode in which the IC current consumption is reduced to $I_{VCCBMpsm0}$.

If the VCC voltage drops below the threshold $V_{VCCslpHVon}$ during BM operation, the HV start-up cell is activated to charge up the VCC capacitor. Special care for proper Vcc self-supply is required to avoid high stand-by power due to start-up cell activation during BM.

4.2 Hybrid-flyback control

The hybrid-flyback converter is based on a resonant asymmetrical half-bridge topology and combines advantages of forward and flyback converters. Figure 12 shows the hybrid-flyback stage with the associated control blocks.

With this controller, the hybrid-flyback power stage can achieve zero voltage switching (ZVS) operation on primary side and zero current switching (ZCS) operation on secondary side under normal operation with proper system design. To achieve ZVS operation and best efficiency, two control methods are implemented:

- Continuous resonant mode (CRM) operation
- Zero voltage resonant valley switching (ZV-RVS) operation

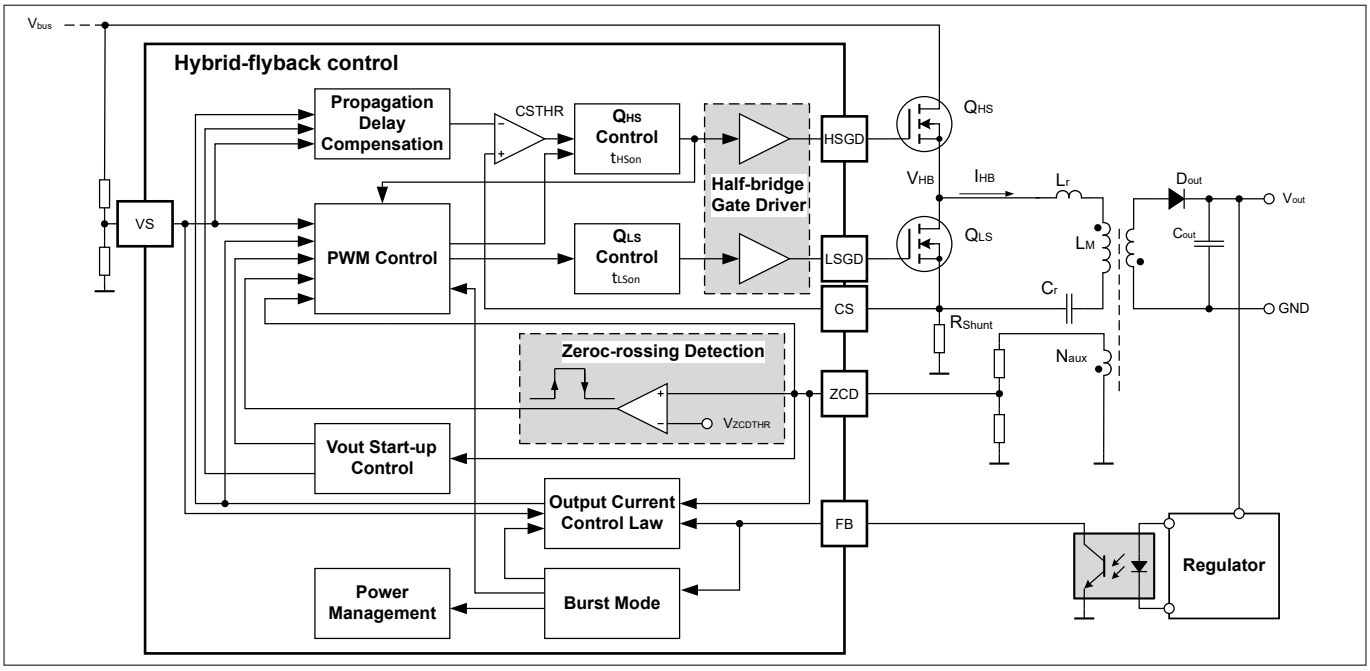

Figure 12 Hybrid-flyback circuit arrangement with associated control blocks

The output current control uses the CSTHR-comparator for peak current control during high-side switch on-time t_{HSon}.

4.2.1 PWM control schemes

In the following chapter, the pulse width modulation (PWM) control methods for the different control modes and the associated mode transition are discussed. Depending on load, output voltage and bus voltage, the control scheme is adjusted to ensure ZVS operation for both low-side (LS) and high-side (HS) switches.

4.2.1.1 Continuous resonant mode control scheme

In continuous resonant mode (CRM), the switching of HS switch and LS switch are activated in a continuous alternating manner with short dead-times: t_{deadHS} applied before the HS switch turn-on and t_{deadLS} applied before the LS switch turn-on.

It targets a ZVS operation for every half-bridge switching cycle by tuning the negative current level I_{MAGneg}.
In Figure 13, typical waveforms are shown. The dead-time t_{deadLS} between HS and LS switch is fixed as the peak current is high enough to provide proper ZVS operation for LS switch.

In CRM operation, the dead-time t_{deadHS} consists of two time intervals:

$$t_{deadHS}(CRM) = t_{LS2ZCD} + t_{ZCD2HS}$$

Equation 1

The LS on-time is adjusted cycle-by-cycle based on the parameters $t_{TRANSnom}$, $I_{MAGnegNom\%}$, $t_{TRANSRVS0V\%}$, and V_{out} sensed at the ZCD pin, while t_{LS2ZCD} plays an subordinate role for the LS on-time determination, but is used to ensure the HS turn-on after ZCD event.

The time period t_{ZCD2HS} (t_2 - t_1) is delaying the HS switch turn-on at time t_2 to achieve ZVS for the HS switch.

The HS switch is activated when the dead-time t_{deadHS}(CRM) is over or when the switching period reaches the value defined by the minimum switching frequency $f_{swDCMmin}$.

After the HS switch is activated, the peak current control determines the HS on-time. The magnetizing current can be measured after a leading-edge spike blanking period t_{HSleb}. This time t_{HSleb} determines the minimum on-time of HS switch operation.

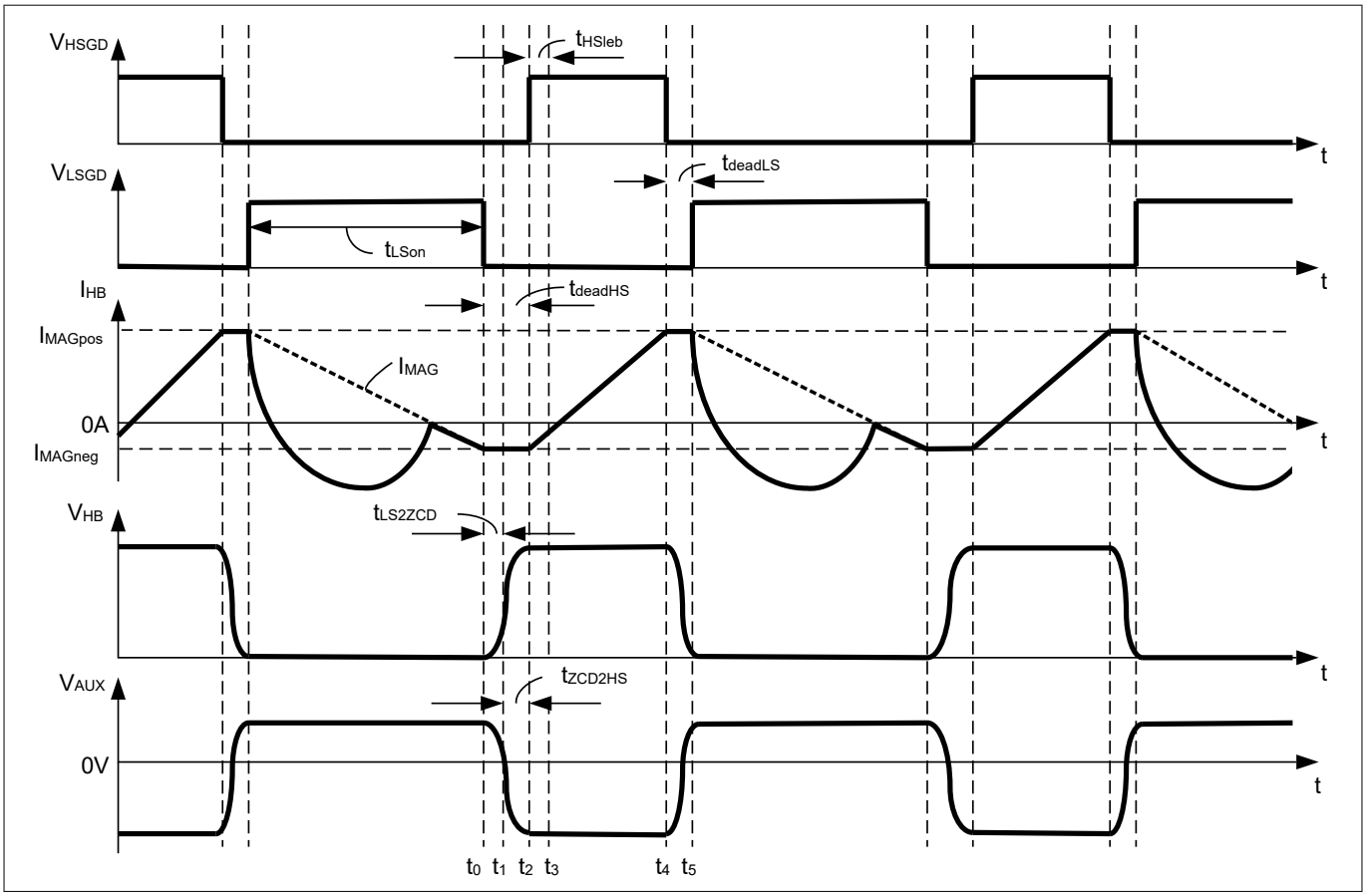

Figure 13 Half-bridge timings for CRM operation

4.2.1.2 Zero voltage resonant valley switching mode control scheme

With decreasing load, CRM mode operation normally leads to high circulating current. In addition, with decreasing V_{out}, the demagnetization time is becoming much longer than half of the resonant period determined by L_r and C_r, which can lead to further resonant half-bridge oscillations. Turning off the LS switch while current flows in the secondary side may lead to voltage spikes across the secondary rectifier.

To overcome these issues, the zero voltage resonant valley switching (ZV-RVS) mode is applied. It keeps the peak magnetizing current in the desired range while maintaining soft switching for both HS and LS switches. Lower load is addressed by lower switching frequency with valley synchronization. Figure 14 shows typical waveforms when operating in the second valley.

In ZV-RVS mode, each HFB cycle consists of two LS pulses, one HS pulse and a waiting time $t_{waitgap}$. The first LS pulse (ZVS-pulse) is synchronized to the valley, so that the LS switch is turned on at a valley of its drain-source voltage and zero magnetizing current. This pulse introduces a small negative current which ensures ZVS for the follow HS switch turn-on.

The required width of the ZVS-pulse t_{ZVS} is determined by the target negative magnetization level I_{MAGneg}, the transformer magnetizing inductance L_m and the output voltage V_{out}. The minimum ZVS-pulse length occurs at lowest input and highest output voltage. In addition, a lower limit t_{ZVSmin} applies.

The waiting time $t_{waitgap}$ is inserted in ZV-RVS mode operation. During this waiting time, a free-wheeling oscillation takes place which is sensed by pin ZCD with a comparator.

The output voltage control is achieved by selecting the appropriate valley, therefore the proper $t_{waitgap,}$ and adjusting the HS on-time, therefore the magnetizing peak current, within the desired range.

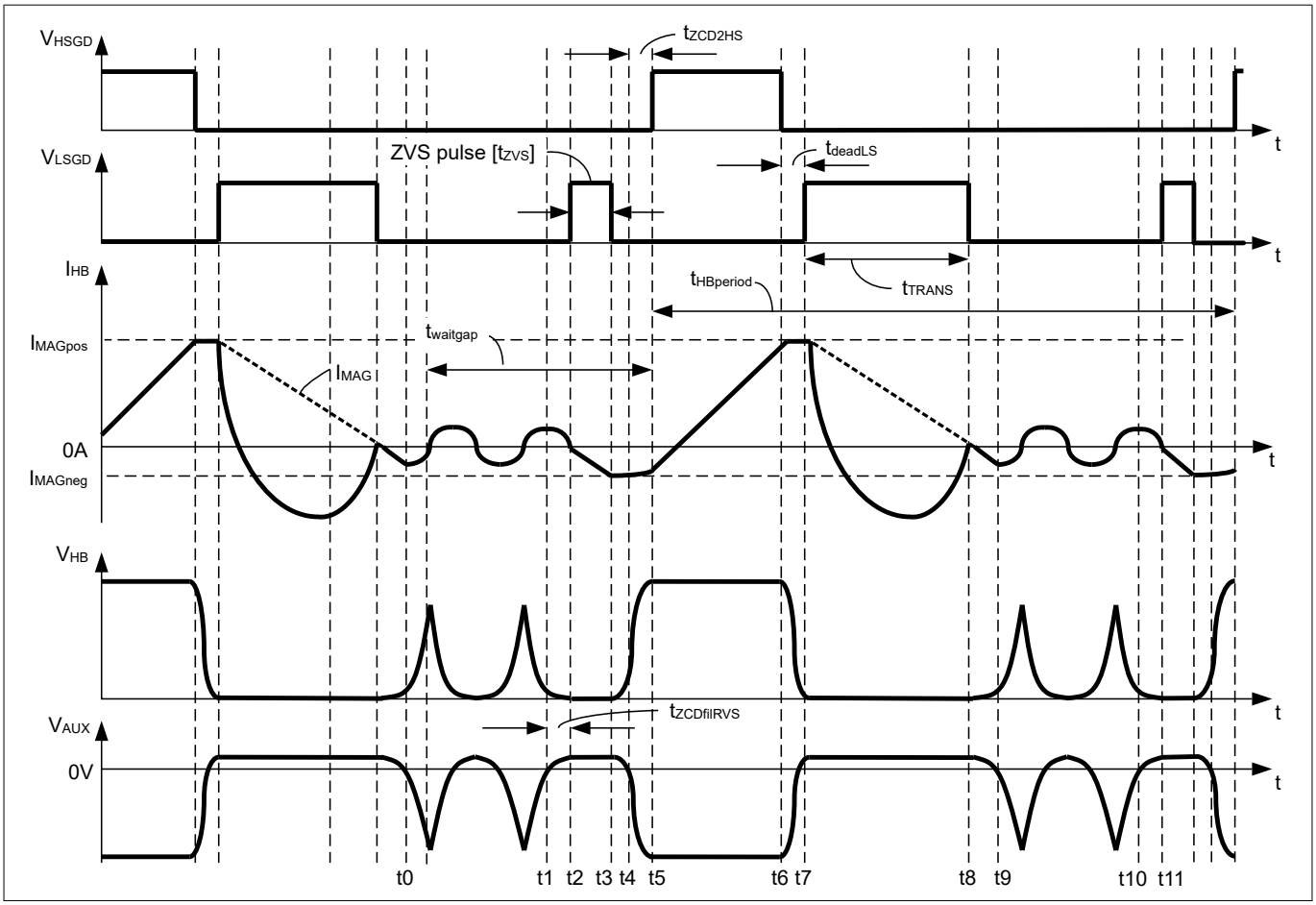

Figure 14 Hybrid-flyback operating in ZV-RVS operation

4.2.1.3 Valley skipping control

During operating in ZV-RVS mode, valley detection is taking place to determine the time for turning on the ZVS pulse. The waiting time $t_{waitgap}$ is controlled based on the target number of detected valleys. If the target valley cannot be detected, the switching frequency will be controlled instead.

4.2.1.4 Mode transition between CRM and ZV-RVS

The mode transition control is based on the target peak current I_{MAGpos} and the voltage measured at the ZCD pin. First, a transition from CRM to ZV-RVS mode, and vice versa, is only possible in case the output voltage, sensed via ZCD, has a certain value. The transition from ZV-RVS to CRM is only possible with a detected output voltage greater than $V_{outRVS2CRM}$ (to have some hysteresis, the transition from CRM back to ZV-RVS only happens for an output voltage smaller than $V_{outCRM2RVS}$). Second, the feedback signal V_{FB} is determining the internal current set-point I_{SET} and compared with the internal thresholds for changeover.

4.2.2 Output control

The HFB controller targets an output current proportional to the feedback voltage level.

In CRM mode, the following equation is valid for the output current, assuming an ideal system:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{1}{2} \cdot N \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 2

Compared to CRM operation, the ZV-RVS mode is adding waiting time gaps $t_{waitgap}$, where no energy transfer is happening. The average output current I_{out} decreases with increasing $t_{waitgap}$ according to

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{t_{HBperiod} - t_{waitgap}}{t_{HBperiod}} \cdot \frac{1}{2} \cdot N \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 3

The output current is mainly regulated by modulating the positive magnetization current level I_{MAGpos}. In CRM operation, the output current I_{out} is controlled by means of a linear relationship between the feedback voltage at FB pin and the associated internal current set-point I_{SET}, which is described in Chapter 4.2.2.1. The negative current I_{MAGneg} is modulated so that ZVS of the HS is achieved.

The output voltage is measured via pin ZCD at the auxiliary winding and filtered inside the controller IC, and the result is used for protection features, for compensation to ensure ZVS operation over wide output voltage range.

4.2.2.1 Output current control law

The positive magnetization level I_{MAGpos} is controlled by comparing the voltage in the shunt resistor R_{shunt} with an internal value:

$$V_{CSpeak} = I_{MAGpos} \cdot R_{Shunt}$$

Equation 4

Peak current regulation is prone to error due to noise. CS pin related PCB design should consider this sensitivity. An external RC-filter at CS pin is recommended. In addition, a digital filter using a filter time $t_{CSTHRfil}$ can be set to blank the CSTHR comparator event.

Figure 15 shows the control path from feedback signal input at FB pin to peak current setting at CS pin. The requested output current equals to the internal I_{SET} for the corresponding feedback signal. The required peak current setting is then calculated based on V_{bus} measurement and mode operation.

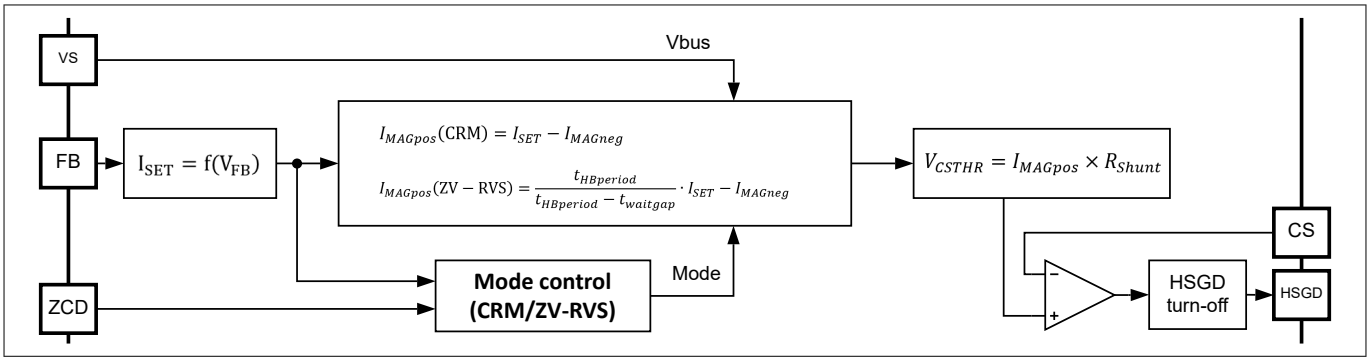

Figure 15 Control path from feedback input to peak current setting

The feedback pin has a pull-up resistor R_{FBpu} to the internal reference voltage (V_{FBoc}). The feedback voltage V_{FB} has a linear correlation with the output current I_{out} between burst mode entry current level $I_{outBMen}$ and the maximum output current $I_{outOCPmax}$. Figure 16 shows the relationship between output current and feedback voltage.

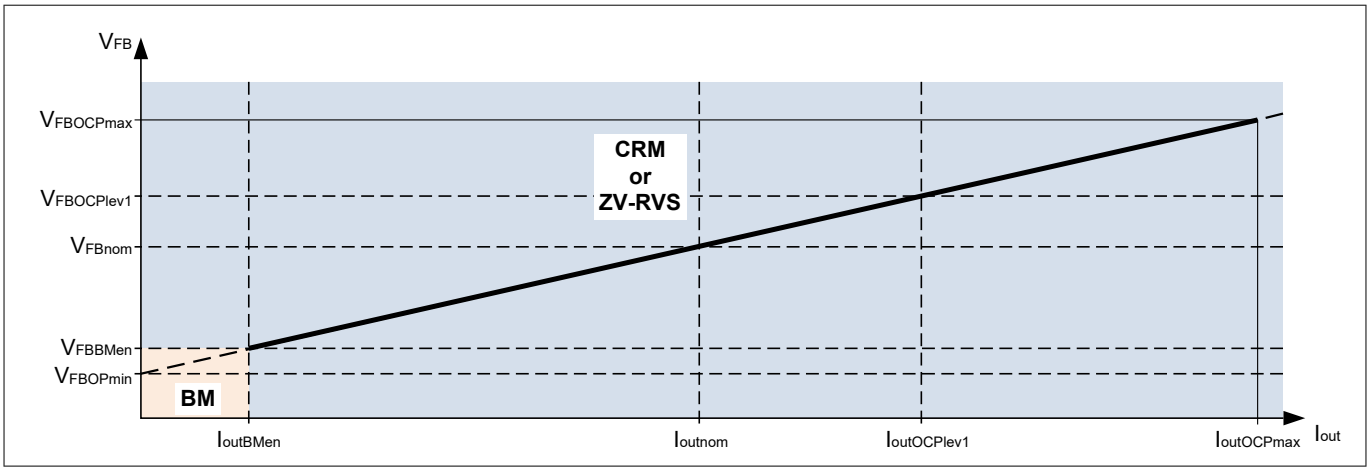

Figure 16 Control law for feedback voltage at FB pin

The output current I_{out} is represented by the equivalent internal current set-point I_{SET}, which is then mapped to the positive magnetization level I_{MAGpos}. The peak current I_{MAGpos} is controlled by a comparator with variable threshold at pin CS. The relation between I_{SET} and I_{MAGpos} is different for CRM and ZV-RVS mode.

4.2.2.2 Keeping ZVS operation for wide Vbus voltage range

The ZVS operation in CRM is explained in Chapter 4.2.1.1. In ZV-RVS, the ZVS pulse length is set targeting a negative current I_{MAGneg} as described in Chapter 4.2.1.2. Here, $I_{MAGnegnom}$ is the minimum negative current. For other bus voltage levels, the negative magnetizing current is adjusted automatically for zero voltage switching.

4.2.2.3 Keeping ZVS operation for wide output voltage range

When output voltage V_{out} is decreasing, the demagnetization takes longer. In CRM, ZVS operation is ensured by adjusting the on-time of the LS switch t_{LSon} to match with the changed V_{out}. In ZV-RVS, the ZVS pulse width t_{ZVS} is calculated from I_{MAGneg} and V_{out} while the LS on-time t_{TRANS} decreases with increasing V_{out} (see Figure 17).

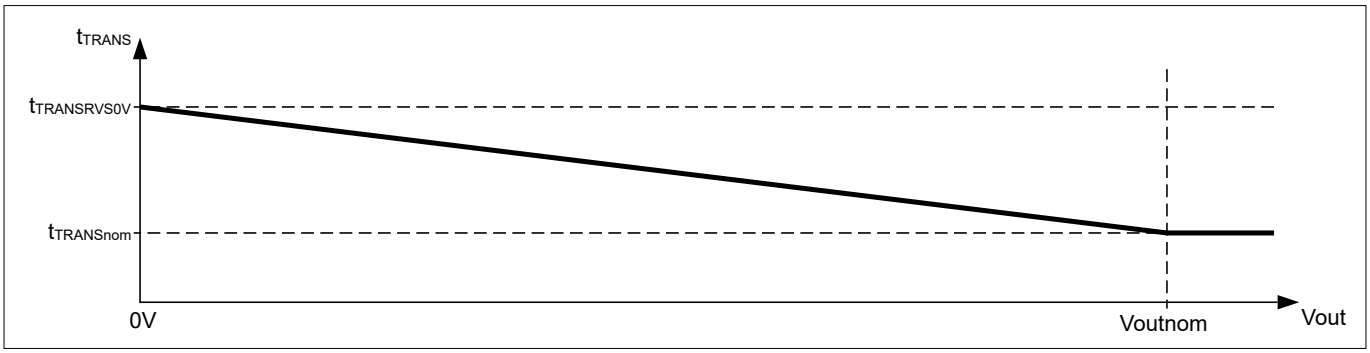

Figure 17 t_{Trans} modulation vs. V_{out}

4.2.2.4 ZVS operation and body-diode cross-conduction prevention during CRM operation

A too short LS on-time can cause hard switching or even body-diode cross-conduction if the magnetizing current is still positive at HS turn-on; on the other hand, a too long LS on-time increases the reactive current and conduction losses and can even saturate the transformer. To exclude hard switching and body-diode cross-conduction, the controller activates the HS switch only after the voltage at pin ZCD indicates a changing of the half-bridge switching node voltage V_{HB} (ZCD event). The controller adjusts the LS on-time to ensure ZVS condition.

4.2.2.5 Propagation delay compensation

During peak current control, a propagation delay is impacting the peak current resulting in higher values. The overshoot depends on both the input voltage V_{bus} and the reflected output voltage at resonant capacitor V_{Cr}. This dependency on V_{bus} and V_{Cr} impacts the current set-point threshold accuracy in the application and is compensated to avoid errors on the feedback signal V_{FB} and the internal current set-point I_{SET}.

4.2.3 Vout start-up control

A hybrid-flyback start-up takes place after the start-up conditions are met, see Chapter 4.1.1. In a first step, several LS pulses are applied to precharge the bootstrap capacitor at HSVCC pin. After that, ZV-RVS switching cycles follow and the output voltage smoothly ramps up. Here, the first switching cycles run with a low and fixed frequency until the voltage at pin ZCD is high enough for valley detection. The start-up phase is finished once the feedback loop takes over the peak current control.

During the first HS pulse, the CS pin voltage is checked for shunt resistor short circuit. A maximum time applies to the ZVS pulse width to prevent too long ZVS pulse due to very low voltage measured at the ZCD pin. A transition from ZV-RVS to CRM takes place during the start-up phase when the voltage sampled at pin ZCD exceeds the related thresholds.

During the first switching cycles of the hybrid-flyback start-up, the dead-time for turning on the HS switch after the ZVS pulse is fixed at the value $t_{deadHSRVS}$, while the dead-time t_{deadLS} is same as in CRM operation.

4.2.4 Frequency jitter

To reduce the EMI noise amplitude, a switching frequency jitter is implemented for the HFB stage. The jitter function is activated in both CRM and ZV-RVS operation if the parameter $I_{MAGnegjitter\%}$ has a non-zero value and the output current is below its OCP levels. The time step of the frequency jitter is defined by the parameter $t_{JitterStep}$.

4.2.5 Half-bridge gate driver

The half-bridge gate driver consists of a low-side gate driver for LS switch supplied by VCC and GND pin, and a floating high-side gate driver supplied by HSVCC and HSGND. The floating HS domain is galvanically isolated and steered via a coreless transformer. The LS and HS gate drivers are enabled/disabled based on the corresponding undervoltage lockout thresholds (V_{VCCon}, V_{VCCoff}) and ($V_{HSVCCon}$, $V_{HSVCCoff}$) (see Chapter 4.3.2.1 and Chapter 4.3.2.2). Both drivers are clamped to their maximum gate driver output voltage, $V_{LSGDhigh}$ and $V_{HSGDhigh}$. If disabled, the gate driver outputs are actively kept pulled down. When HSVCC exceeds the threshold $V_{HSVCCon}$, the high-side gate driver is enabled after a time period of $t_{HSGDendel}$.

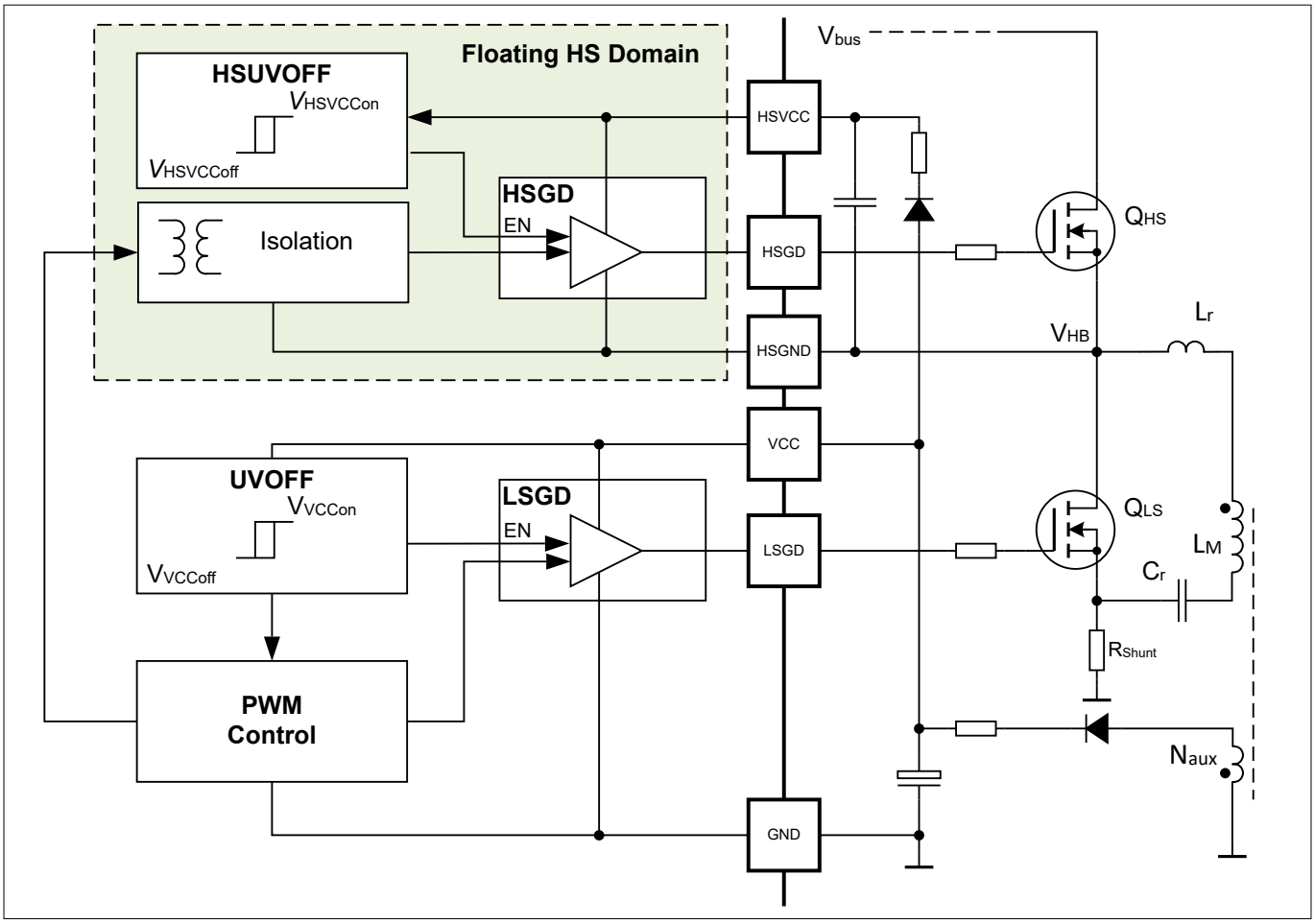

Figure 18 Half-bridge gate driver with MOSFET switches

To drive discrete CoolGaN™ devices in the half-bridge, a dedicated external RC-network is recommended, see Figure 4.

4.2.6 Burst mode control

The IC contains a burst mode control block to enter a highly efficient operation mode at light load. By introducing long non-switching phases where the IC is in a sleep mode, the average switching and bias losses are reduced during burst mode operation. The hybrid-flyback operates in burst mode at low load. The burst mode operation is controlled in relation to the output current reflected by the feedback voltage V_{FB}. Figure 19 shows the main functions for the burst mode control.

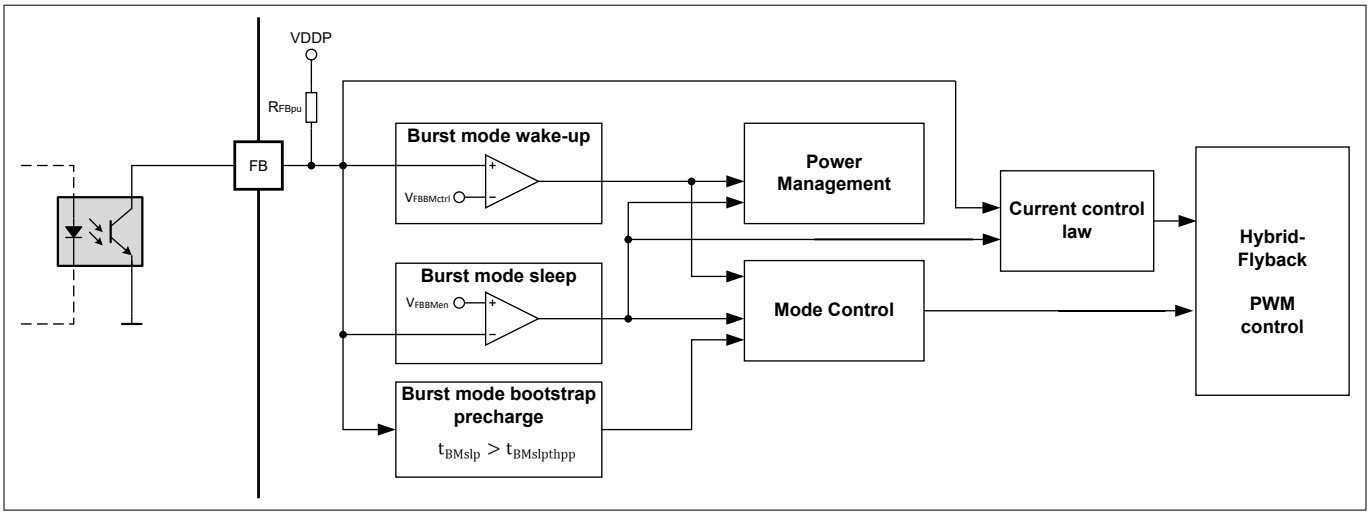

Figure 19 Burst mode control block

4.2.6.1 Burst entry

Once V_{FB} is dropping below V_{FBBMen}, the generation of next switching pulse is stopped and burst mode is enabled. The HV start-up cell is turned on to charge up C_{VCC} until V_{VCCon} is reached, then IC enters sleep phase and its current consumption reduces to $I_{VCCBMpsm0}$.

4.2.6.2 Burst mode operation

The burst frame ON (burst) and OFF (sleep) is controlled by comparing the voltage at FB pin with the thresholds V_{FBBMen} and $V_{FBBMctrl}$. Once the FB voltage sinks and crosses the threshold V_{FBBMen}, the IC enters the sleep phase. During the sleep phase, FB voltage arises. When it goes above the threshold $V_{FBBMctrl}$, the IC wakes up and bursts till the FB voltage reaches V_{FBBMen} and the IC enters sleep phase again. The burst frame duty cycle and frequency is fully controlled by means of V_{FB}.

4.2.6.3 Burst mode bootstrap precharge

Operation in burst mode at very light load results in long sleep phases without switching activities. During this sleep time period, V_{HSVCC} voltage may drop below the off-threshold $V_{HSVCCoff}$ and the floating HS gate driver is then deactivated. To ensure that a proper HSVCC supply is in place for turning on the HS switch after a long IC sleep phase, but only when the captured burst mode sleep time exceeds the threshold $t_{BMslpthrpp}$, a train of $N_{BMprepulse}$ precharge pulses is introduced before the first ZV-RVS switching cycle. Figure 20 shows a precharge pulse train pattern for the case $N_{BMprepulse} = 3$.

***Note**: If a HS pulse is missing due to improper HSVCC supply, the subsequent LS pulse may lead to hard switching. Therefore, the controller tries to detect this case and may stop the switching operation.*

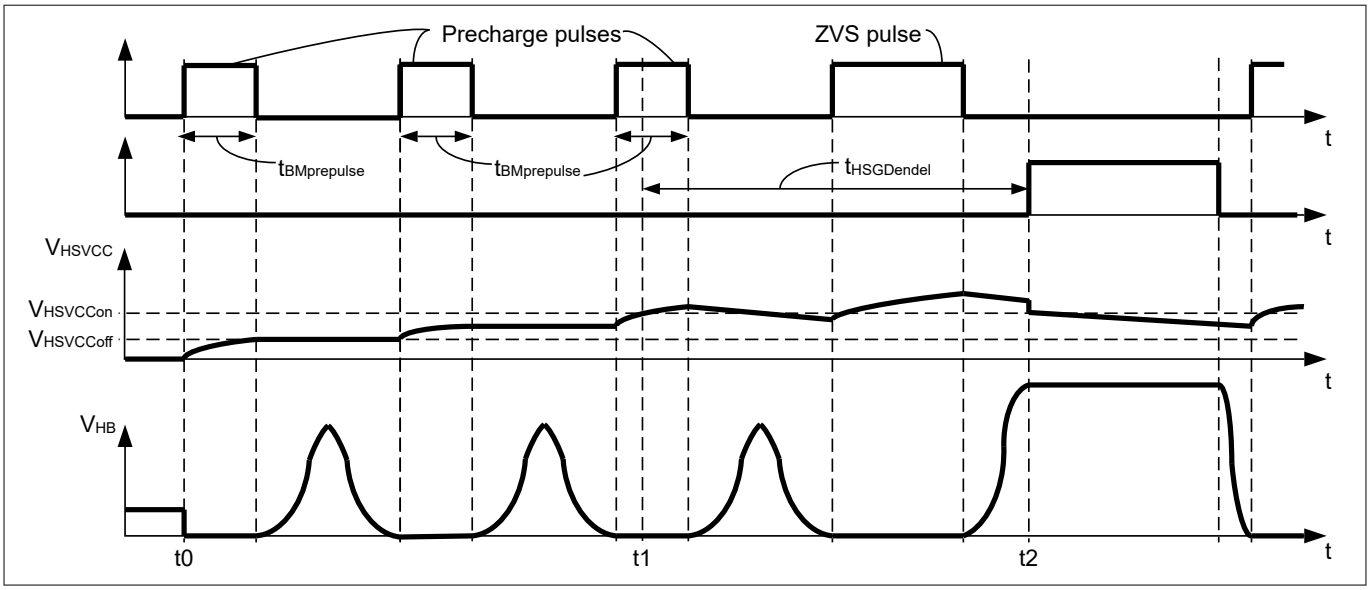

Figure 20 Precharge pulse train pattern

4.3 Protections

The IC supports several protection functions resulting in different protection reactions.

For most protection events, the IC enters a protection mode (see Chapter 4.3.1). The protection is configurable, including the triggering value and/or its reaction mode. The error code is sent out by toggling the MFIO pin once a protection is triggered.

Table 2 Protection features and reaction

Protection feature	Symbol	Error code	Protection reaction
VCC undervoltage lockout	UVOFF		HW reset and restart
HSVCC undervoltage lockout	HSUVOFF		Disable HS gate driver
VCC overvoltage protection	VCCOVP	25	Configurable: Auto-restart or latch
Brown-in protection	BIP	18	Bang-bang mode, waiting for brown-in in start-up check phase
Brown-out protection	BOP	2	Fast-restart mode
Output start-up timeout protection	VoutSTTOP	4	Configurable: Auto-restart or latch
Bus overvoltage protection	ACOVP	12	Auto-restart
Bus undervoltage protection	BusUVP	29 at start-up; 11 during operation	Fast-restart mode
Output overcurrent protection level 1	OCPlev1	9	Configurable: Auto-restart or latch
Output maximum current protection	OCPmax	8	Configurable: Auto-restart or latch

(table continues...)

Table 2 (continued) Protection features and reaction

Protection feature	Symbol	Error code	Protection reaction
HFB primary side overcurrent protection	CSPROT	13	Configurable: Auto-restart or latch
Vout overvoltage protection	VoutOVP	6	Configurable: Auto-restart or latch
Vout undervoltage protection	VoutUVP	7	Configurable: Auto-restart or latch
Vout short circuit protection	VoutSCP	27	Latch
CS pin short protection	CSSCP	3	Configurable: Auto-restart or latch
FB pin start-up protection	FBSTUP	14	Stop operation and enter bang-bang mode for start-up check phase
HFB open-loop protection	HFBOLP	26	Latch
External overtemperature protection	extOTP	16 during operation 17 at start-up	Configurable: Auto-restart or latch
Watchdog timer	WDOG	19	Auto-restart
Memory parity check	MEMPAR	23	Auto-restart

4.3.1 Protection modes

Once the protection mode is entered, the IC stops the gate driver switching at the LSGD and HSGD pins and enters stand-by mode. During stand-by mode, the HV start-up cell is operating in the bang-bang mode (see Chapter 4.1.3) to keep the VCC voltage at a high level to have enough energy stored in the VCC capacitor for the system start-up. Three protection modes are supported as described in the sequel.

4.3.1.1 Deactivate IC after undervoltage lockout

In case VCC drops below V_{VCCoff} the undervoltage lockout protection is triggered, the IC is completely deactivated and is only restarted with the regular start-up mechanism (see Chapter 4.1.1).

4.3.1.2 Auto-restart mode

When auto-restart mode is activated, the controller stops switching at the gate driver pins. After the auto-restart time t_{ARM}, the control IC resumes its operation. During the auto-restart time t_{ARM} the controller wakes up very $t_{ARMbase}$ to re-charge VCC to V_{VCCon} (see Chapter 4.1.3).

4.3.1.3 Latch mode

In latched operation the system stays in stand-by mode without any restart attempt. The latched operation can only be reset by VCC dropping below the UVOFF HW reset threshold V_{VCCoff}. In latch mode operation, the HV start-up cell is turned on at VCC pin voltage threshold $V_{VCCslpHVon}$ and turned off when reaching VCC pin voltage threshold V_{VCCon} (see Chapter 4.1.3).

4.3.1.4 Fast-restart mode

In fast-restart mode operation, the start-up cell is blocked, all gates pulled down. The core is running further and consumes the energy stored in the VCC capacitor. After the V_{VCC} drops below V_{VCCoff}, the controller is forced with a new cold restart.

4.3.2 Protection features

4.3.2.1 VCC undervoltage lockout

The VCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the IC operation depending on the supply voltage at pin VCC. The UVOFF contains a hysteresis with the bottom voltage threshold V_{VCCoff} for deactivating the IC and the upper voltage threshold V_{VCCon} for activating the IC. Once the VCC voltage level drops below the bottom threshold V_{VCCoff}, IC is fully reset and deactivated. In reset state, the HV start-up cell is turned on until the VCC voltage exceeds V_{VCCon}, and then a fresh IC start-up begins (see Chapter 4.1.1).

4.3.2.2 HSVCC undervoltage lockout

The implemented HSVCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the floating high-side driver. The HSUVOFF contains a hysteresis with the upper voltage threshold $V_{HSVCCon}$ for activating the high-side gate driver. A HSVCC voltage level dropping below the bottom threshold $V_{HSVCCoff}$ turns off and deactivates immediately the high-side driver. During deactivation phase the high-side driver current consumption is reduced.

4.3.2.3 VCC overvoltage protection

There is an overvoltage detection at pin VCC. The detection function consists of a threshold V_{VCCOVP} and a blanking time of t_{VCCOVP}. Once the V_{VCC} is above the voltage threshold for longer the blanking time, the VCC overvoltage protection is triggered and the control IC enters the configured protection mode.

4.3.2.4 Brown-in protection

One condition must be fulfilled for successful brown-in:

- Bus voltage above the threshold with $V_{bus} > V_{busbi}$, as sensed via pin VS

For system to start up after a detected brown-in, the other conditions are checked, as well (Chapter 4.1.1).

4.3.2.5 Start-up time-out protections

A start-up time-out function is implemented for the hybrid-flyback output. In case of overload during start-up, the output voltage V_{out} may not reach the regulation target voltage, preventing the system from entering regulation. A time-out is detected if the current set-point determined by V_{FB} is not dropping below the current set-point determined by V_{out} within the time period $t_{startto}$.

4.3.2.6 Bus overvoltage protection

Once the measured bus voltage is above the threshold V_{busOVP} and for longer than $t_{VbusOVP}$, the HFB operation is stopped and the controller enters the set protection mode.

4.3.2.7 Bus undervoltage protection

Undervoltage detection of the bus voltage is done indirectly by observation of the HFB switching time.

Once the protection is triggered, the system enters fast-restart mode.

4.3.2.8 Hybrid-flyback overcurrent protection

The hybrid-flyback overcurrent protection contains several detection functions, which protect the application against operating under output overcurrent conditions or exceeding a primary side peak current (see Figure 21).

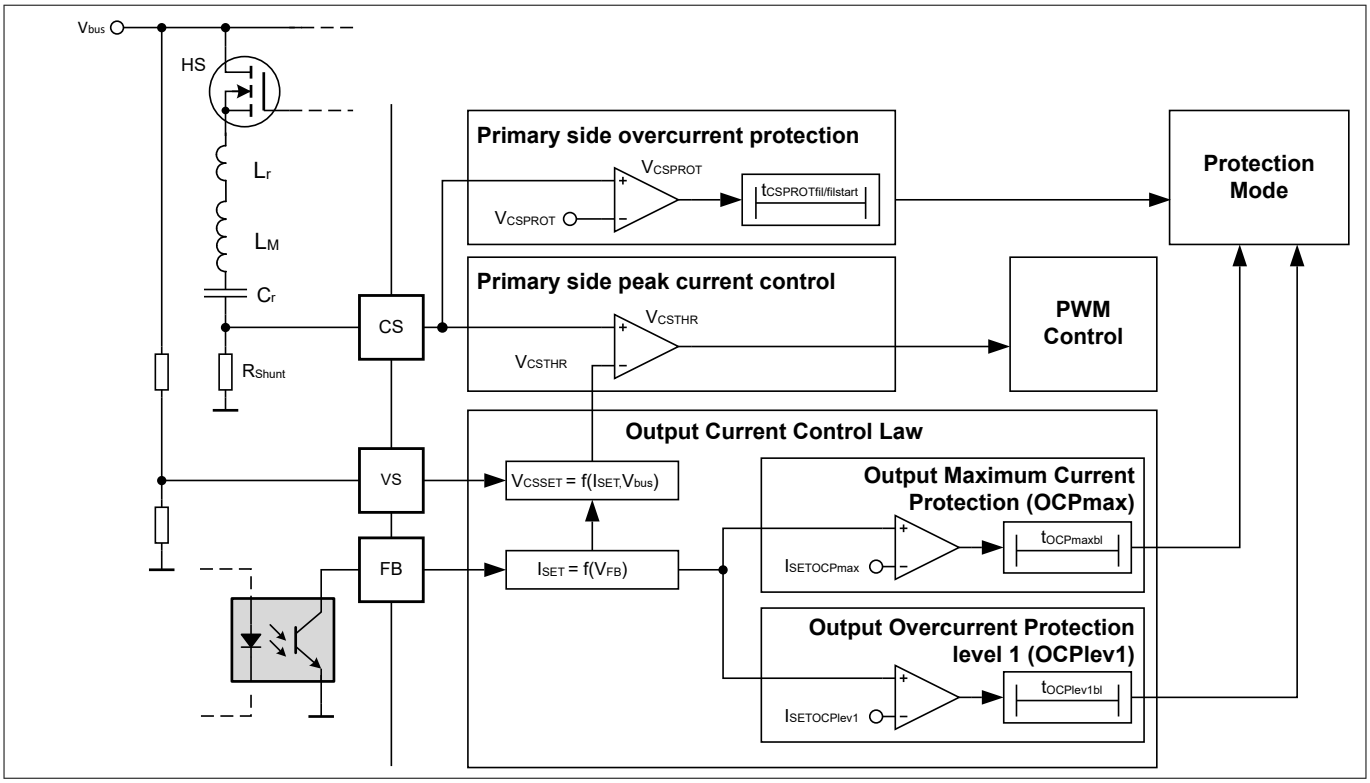

Figure 21 Overcurrent protection overview

4.3.2.8.1 Output overcurrent protection

The output overcurrent protection has two levels:

- Output overcurrent protection level 1, with thresholds $I_{OUTOCPlev1}$ and blanking time $t_{OCPlev1bl}$
- Output maximum current protection, with thresholds $I_{OUTOCPMax}$ and blanking time $t_{OCPMaxbl}$

Based on the defined output overcurrent protection levels $I_{SETOCPlev1/max}$, internal thresholds $I_{SETOCPlev1/max}$ are derived from the output current control law. Once the current set-point I_{SET} crosses the threshold levels, a timer is started. The configured protection mode (auto-restart or latch) is entered when the timer reaches the thresholds $t_{OCPlev1bl/maxbl}$. The timer is reset when I_{SET} drops below the thresholds.

Once a higher output current corresponding to a current set-point $I_{SET} > I_{SETOCPmax}$ is requested via V_{FB} control, the HFB current is kept limited. During this phase, the output voltage drops because the output current is higher than that provided by the converter.

4.3.2.8.2 Primary side overcurrent protection CSPROT

V_{CSPROT} is a fixed threshold and above $V_{CSTHRmax}$. The CSPROT function is not blanked during the leading-edge blanking time t_{HSleb}. Once the voltage at CS pin exceeds V_{CSPROT}, the configured protection mode (auto-restart or latch) is entered.

To avoid false CSPROT events, blanking times $t_{CSPROTfilstart}$ and $t_{CSPROTfil}$ apply.

4.3.2.9 Output over- and undervoltage protection

The IC provides two output voltage Vout protection mechanisms for output undervoltage and output overvoltage to ensure a reliable operation within a defined Vout operating range. The measurement is done at pin ZCD via the reflected voltage at the auxiliary winding of the transformer during the demagnetization phase when the LS switch is turned on (see Figure 22). Furthermore, the zero-crossing detection during start-up phase is monitored to detect short circuit at the output.

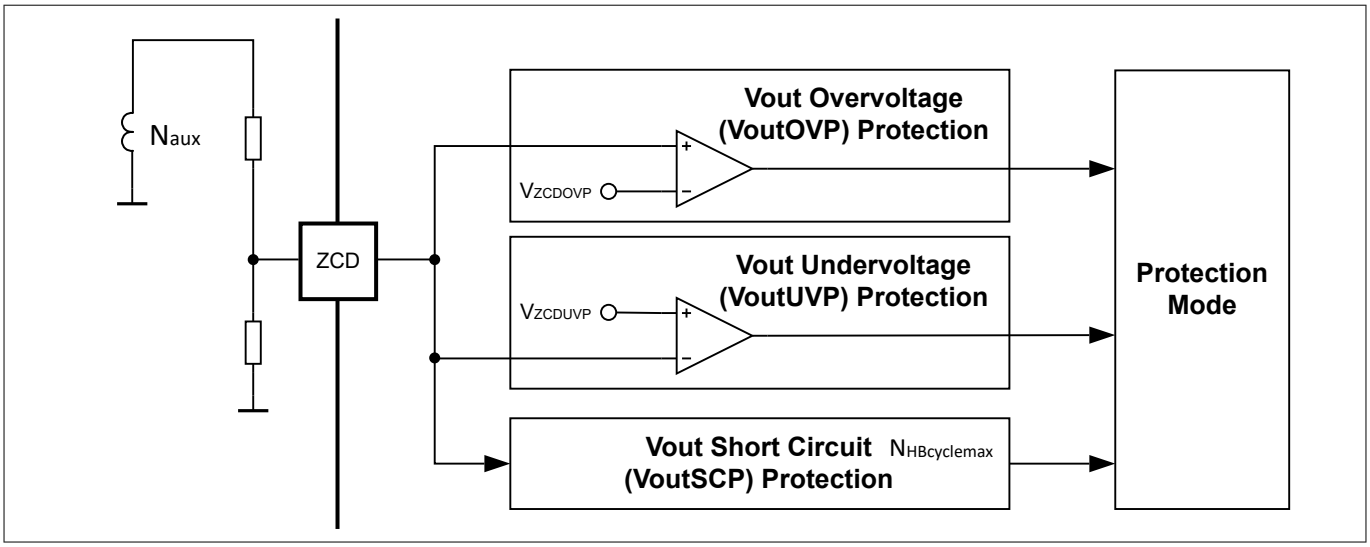

Figure 22 Output voltage protections

4.3.2.9.1 Vout overvoltage protection

The IC provides output overvoltage detection. This is achieved at primary side via the voltage measured at the ZCD pin, which comes from the transformer auxiliary winding, and during the LS on-time in every switching cycle. Output overvoltage is detected when the reflected output voltage exceeds the threshold V_{ZCDOVP} (corresponding to the threshold V_{outOVP}) for longer than the blanking time $t_{outOVPbl}$. Once an overvoltage event is detected, the protection mode is triggered.

4.3.2.9.2 Vout undervoltage protection

Output undervoltage detection is detected via the voltage measured at the ZCD pin. After the start-up is finished, Vout undervoltage is triggered when the voltage measured at pin ZCD is dropping below the threshold V_{ZCDUVP}, which corresponds to the threshold V_{outUVP}. Once the protection is triggered, the respective protection mode is entered.

After wake-up from sleep in burst mode operation, the voltage measured at pin ZCD might be distorted due to various reasons. To avoid mis-triggering the output undervoltage protection, the output undervoltage detection is blanked by the a time defined by $CFG_{VoutUVPBM}$.

4.3.2.9.3 Vout short circuit protection

For a short circuit protection at the output, two different mechanisms are implemented. One is only active during start-up, the another one after start-up.

During start-up, the Vout short circuit protection is achieved by limiting the number of half-bridge switching cycles. A maximum of $N_{HBcyclemax}$ consecutive half-bridge switching cycles are allowed without zero-crossing detected. If $N_{HBcyclemax}$ is exceeded while no zero-crossing is detected, the start-up phase is stopped and the configured protection mode is entered.

During operation after start-up, another Vout short circuit protection mechanism is active. If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold $\Delta V_{ZCDshort}$, which is corresponding to the parameter ΔV_{outSCP}, the output short circuit protection is triggered and the protection mode is entered.

4.3.2.10 CS pin short circuit protection

A short circuit detection at CS pin is activated for the very first HS switch pulse to protect the application operating with a shortened R_{Shunt}.

4.3.2.11 FB pin start-up protection

At the start-up condition check phase, the voltage at pin FB is evaluated. The system starts up only when $V_{FB} > V_{FBBMctrl}$ is also fulfilled. Otherwise, the protection is triggered and enters the mode defined by parameter $EV_{StartFBlow}$.

4.3.2.12 Hybrid-flyback open-loop protection

The open control loop protection is using a similar method as the output short protection (see Chapter 4.3.2.9.3). Only in case of a saturated feedback voltage at FB, the reflected output voltage measured via ZCD pin is evaluated: If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold ΔV_{ZCDolp}, which is related to the configurable output voltage threshold ΔV_{outolp}, an open-loop protection is triggered and the configured protection mode is entered.

4.3.2.13 External overtemperature protection

The external overtemperature protection (ExtOTP) is based on measuring an external NTC thermistor at pin MFIO, see Figure 23. Once the external resistance is falling below the threshold $R_{MFIOOTPtrig}$, overtemperature protection mode is entered. The controller tries with auto-restart first, but only for $N_{OTPevmax}$ times of the OTP event, then latch mode is entered. In case of an auto-restart, a restart cycle takes place only when the value of the external resistance exceeds the threshold $R_{MFIOOTPrel}$.

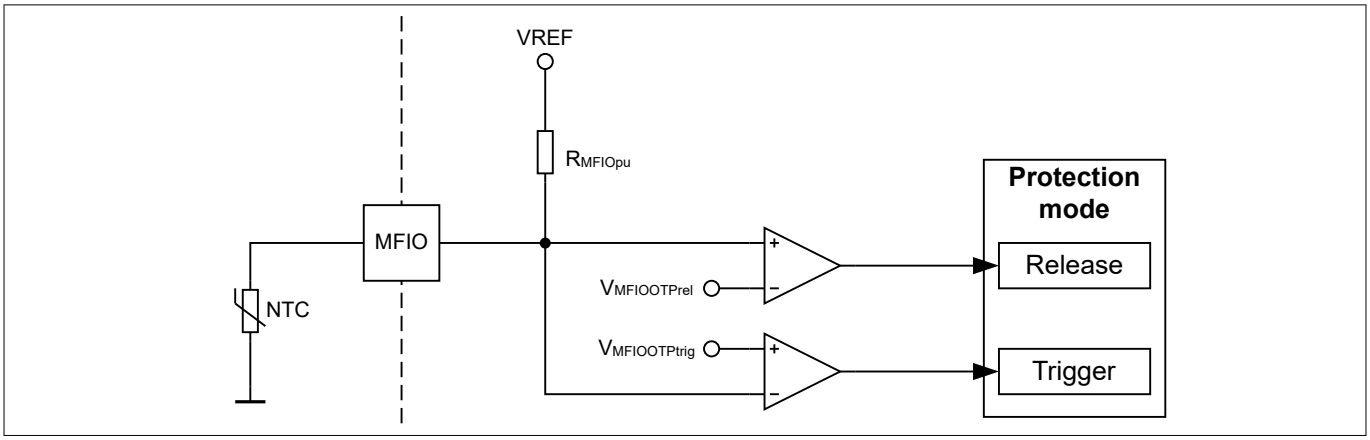

Figure 23 External overtemperature protection using NTC-thermistor at MFIO pin

Optionally, in case of an overtemperature event is detected via the external thermal resistor (lower than $R_{MFIOOTPtrig}$), the primary side peak current set-point is reduced, resulting in power foldback, to avoid overheating of the power supply unit. Once the power unit is cooled down and the measured temperature comes back to the release set-point $R_{MFIOOTPrel}$, the primary side peak current is purely controlled by the feedback voltage again.

Besides the overtemperature protection with external NTC (OTP_NTC), three other functionalities are integrated by using the MFIO pin: ACT_EN (pin high at IC non-burst operation), OTP_NTC_Pder (external overtemperature protection with power derating once overtemperature triggered) and VoutTog (MFIO pin toggles depending on the output voltage level compared to $V_{outMFIOgoL}$ and $V_{outMFIOgoH}$). The final functionality depends on the configuration of $MFIO_{funct}$. Once configured, only that one of the four options is effective.

4.3.2.14 Memory parity check

For memory integrity a parity check is continuously provided during operation. Once a parity error is detected the controller is reset and the configured protection mode (auto-restart mode or latch) is entered.

4.3.3 Error read-out at MFIO pin

Once a protection is triggered, the respective error code (see Table 2) is sent out at pin MFIO.

5 Electrical characteristics

All signals are measured with respect to ground GND pin. The voltage levels are valid if other ratings are not violated.

Figure 24 illustrates the definition for the voltage and current parameters used in this datasheet.

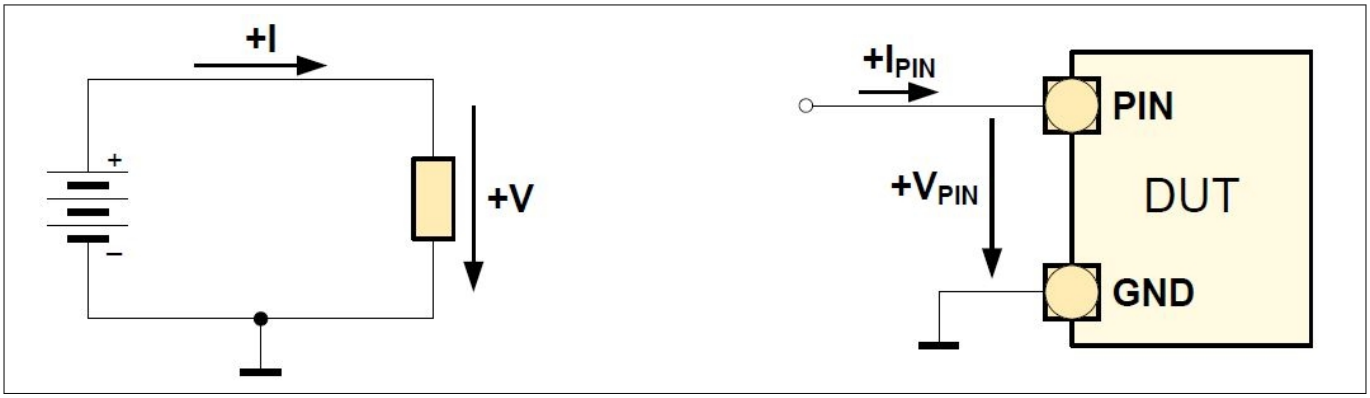

Figure 24 Voltage and current definitions

5.1 Absolute maximum ratings

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.

Table 3 Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at pin HV	V_{HV}	–0.3	–	600	V	1)
Maximum current into pin HV	I_{HV}	-	-	10	mA	1)
Voltage at pin MFIO	V_{MFIO}	–0.5	-	3.6	V	1)
Voltage at pin VS	V_{VS}	–0.5	-	3.6	V	1)
Voltage at pin FB	V_{FB}	–0.5	-	3.6	V	1)
Voltage at pin ZCD	V_{ZCD}	–0.5	-	3.6	V	1)
Maximum negative transient voltage at pin ZCD	$-V_{ZCDN\_TR}$	-	-	1.5	V	pulse < 500 ns
Maximum permanent negative clamping current for pin ZCD	$-I_{ZCDCLN\_DC}$	-	-	2.5	mA	RMS
Maximum transient negative clamping current for pin ZCD	$-I_{ZCDCLN\_TR}$	-	-	10	mA	pulse < 500 ns
Voltage at pin CS	V_{CS}	–0.5	-	3.6	V	1)
Maximum negative transient voltage at pin CS	$-V_{CSN\_TR}$	-	-	3	V	pulse < 500 ns

(table continues...)

1 Permanently applied as DC value.

Table 3 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum permanent negative clamping current for pin CS	$-I_{CSCLN\_DC}$	-	-	2.5	mA	RMS
Maximum transient negative clamping current for pin CS	$-I_{CSCLN\_TR}$	-	-	10	mA	pulse < 500 ns
Maximum permanent positive clamping current for pin CS	I_{CSCLP_DC}	-	-	2.5	mA	RMS
Maximum transient positive clamping current for pin CS	I_{CSCLP_TR}	-	-	10	mA	pulse < 500 ns
Voltage at pin LSGD	V_{LSGD}	–0.5	-	V_{VCC}+ 0.3	V	Limited by internal clamping
Voltage at pin HSVCC, HSGD and HSGND	V_{HSx}	-650	-	650	V	Isolation voltage, referred to GND
Voltage at pin HSVCC	V_{HSVCC}	–0.5	-	24	V	referred to HSGND
Voltage at pin HSGD	V_{HSGD}	–0.5	-	V_{HSVCC} +0.3	V	referred to HSGND
Slew-rate for floating high-side domain	dV_{HS}/dt	–50	-	50	V/ns	
Junction operation temperature	T_J	–40	-	125	°C	
Storage temperature	T_S	–55	-	150	°C	
Maximum power dissipation	P_{TOT}	-	-	0.63	W	T_A = 50 °C, T_J = 125 °C
Soldering temperature	T_{Sold}	-	-	260	°C	[2] Wave soldering
ESD HBM capability	V_{HBM}	-	-	2000	V	[3] Human body model
ESD CDM capability	V_{CDM}	-	-	500	V	[4] Charged device model
Latch-up capability	I_{LU}	-	-	150	mA	[5] Pin voltages acc. to abs. max. rating

2 According to JESD22-A111
3 According to ANSI/ESDA/JEDEC JS-001
4 According to JESD22-C101
5 According to JESD78, 85 °C (Class II) temperature

5.2 Package characteristics

Table 4 Package characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance from junction to ambient	R_{thJA}	-	-	119	K/W	JEDEC 1s0p
Thermal characterization parameter from junction to top	Ψ_{thJT}	-	-	2	K/W	PG-DSO-14, JEDEC 1s0p
Creepage distance between HV and HSxxx to GND-related pins	D_{crp}	2.1	-	-	mm	

5.3 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Table 5 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction operation temperature	T_J	-25	-	125	°C	
Voltage at pin HV	V_{HV}	–0.3	-	600	V	
External voltage at pin VCC	V_{VCC}	11	-	24	V	Max. value needs to consider internal power losses
Voltage at pin MFIO	V_{MFIO}	–0.3	-	3.3	V	
Voltage at pin FB	V_{FB}	–0.3	-	3.3	V	
Voltage at pin ZCD	V_{ZCD}	–0.3	-	3.3	V	
Voltage at pin CS	V_{CS}	–0.3	-	3.3	V	
Total maximum current out of pins FB and MFIO	$-I_{FB}-I_{MFIO}$	-	-	0.63	mA	During sleep phase in burst mode
Voltage at pin LSGD	V_{LSGD}	–0.3	-	V_{VCC} + 0.3	V	Internally clamped at $V_{LSGDhigh}$
Maximum low state output reverse current at pin LSGD	$-I_{LSGDLREV}$	-	-	100	mA	[6] Applies if V_{LSGD} < 0 V and driver at low state
Voltage at pin HSGD	V_{HSGD}	–0.3	-	V_{HSVCC} + 0.3	V	Internally clamped at $V_{HSGDhigh}$
Maximum low state output reverse current at pin HSGD	$-I_{HSGDLREV}$	-	-	100	mA	Applies if V_{HSGD} < 0 V and driver at low state

(table continues...)

6 Assured by design.

Table 5 (continued) Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at pin HSVCC	V_{HSVCC}	10	-	24	V	Referred to HSGND
Voltage at pin HSGND	V_{HSGND}	–0.3	-	600	V	
UART Baudrate at pin MFIO	t_{BD}	10k	-	115k	Bd	
Voltage at pin VS	V_{VS}	–0.3	-	3.3	V	

5.4 Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature. Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is VCC = 14.0 V if not otherwise specified.

5.4.1 High voltage (HV pin)

Table 6 Electrical characteristics of HV pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HV VCC charge current capability	$I_{HVchargeVCC}$	2.4	5.0	7.5	mA	[7] V_{VCC} = 1 V, V_{HV} = 30 V; Peak current limited in application by external resistors
Maximum leakage current at HV pin	I_{HVLK}	-	-	10	µA	V_{HV} = 600 V, HV start-up cell disabled

5.4.2 Power supply (VCC pin)

Table 7 Electrical characteristics of power supply (VCC pin)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Turn-on threshold	V_{VCCon}	19.0	-	22.0	V	Rising slope
Turn-off threshold	V_{VCCoff}	7.98	-	8.82	V	Falling slope, IC not in auto-restart or latch mode
Turn-off threshold	V_{VCCoff}	2.90	-	5.70	V	Falling slope, IC in auto-restart or latch mode

(table continues...)

[7] Max. peak charge current is limited in the application by external resistors connected to HV pin.

Table 7 (continued) Electrical characteristics of power supply (VCC pin)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Threshold to activate HV cell for VCC-supply during burst mode	$V_{VCCslpHVon}$	9.97	10.5	11.03	V	Falling slope
UVOFF current	$I_{VCCUVOFF}$	-	20	40	µA	$V_{VCC} < V_{VCCoff(min)} - 0.3$ V
Supply current	$I_{VCCopnm}$	-	11	14.5	mA	Without gate driver gate charge losses and during brown-in phase
Quiescent current during burst mode power-saving phase	$I_{VCCBMpsm0}$	-	0.7	3.4	mA	Burst mode entered; pin MFIO and FB open
Quiescent current during bang-bang mode	I_{VCCBB}	-	0.32	0.58	mA	Protection mode entered; pin MFIO and FB open
Overvoltage protection threshold	V_{VCCOVP}	22.0	23.0	24.0	V	
Overvoltage protection blanking time	t_{VCCOVP}	-	1.0	-	ms	

5.4.3 Floating HS domain (HSGND, HSVCC and HSGD pin)

Table 8 Electrical characteristics of HS domain pins

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSVCC turn-on threshold	$V_{HSVCCon}$	8.7	9.2	9.7	V	Rising slope
HSVCC turn-off threshold	$V_{HSVCCoff}$	6.2	6.7	7.2	V	Falling slope
HSVCC idle current	$I_{HSVCCidle}$	-	0.3	0.8	mA	Without gate driver gate charge losses, VHSVCC = 14 V
HSGD enabling delay time after HSVCC voltage is exceeding turn-on threshold	$t_{HSGDendel}$	-	2.3	4.1	µs	V_{HSVCC} = 11 V
HSGD voltage at high state	$V_{HSGDhigh}$	10	11	12	V	I_{HSGD} = –20 mA
HSGD voltage at active shutdown	$V_{HSGDaSD}$	-	25	200	mV	I_{HSGD} = 20 mA, V_{HSVCC} = 5 V
HSGD peak source current	$-I_{HSGDpksrc}$	130	-	-	mA	
HSGD peak sink current	$I_{HSGDpksnk}$	450	-	-	mA	
HSGD driver output low impedance	R_{HSGDLS}	-	-	5	Ω	I_{HSGD} = 100 mA

5.4.4 Bus voltage sensing (VS pin)

Table 9 Electrical characteristics of VS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{VSlk}	–0.2	-	0.2	µA	0 V < V_{VS} < 2.9 V
Dynamic voltage range	V_{VS}	0.13	-	2.75	V	
Second level overvoltage protection (OVP2) threshold	V_{VSovp2}	2.7	2.8	2.9	V	

5.4.5 Hybrid-flyback zero-crossing detection (ZCD pin)

Table 10 Electrical characteristics of ZCD pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{ZCDlk}	–10	-	10	µA	V_{ZCD} = 0 V / 3.0 V
Maximum pin voltage threshold for Vout overvoltage protection	$V_{ZCDOVPmax}$	-	2.75	-	V	
Zero-crossing detection threshold	V_{ZCDTHR}	15	40	70	mV	Falling slope
Input voltage negative clamping	$-V_{ZCDCLN}$	140	180	220	mV	

5.4.6 Multifunctional input and output (MFIO pin)

Table 11 Electrical characteristics of MFIO pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up resistor	R_{MFIOpu}	8.8	11	13.2	kΩ	[8] $MFIO_{funct}$ = ExtOTP
Open circuit output voltage	V_{MFIOoc}	-	V_{REF}	-	V	[8] $MFIO_{funct}$ = ExtOTP
Input high current with active weak pull-down	$-I_{MFIOhpd}$	90	-	300	µA	Measured at min. V_{MFIOIH}
Leakage current	I_{MFIOlk}	-5	-	1	µA	V_{MFIO} = 0 V / 3.0 V
Input capacitance	C_{MFIOIN}	-	-	10	pF	
Input threshold for logic “0”	V_{MFIOIL}	-	-	1	V	[8]
Input threshold for logic “1”	V_{MFIOIH}	2	-	-	V	[8]
Output voltage for logic “0”	V_{MFIOOL}	-	-	0.8	V	[8] I_{MFIOOL} = 2 mA
Output voltage for logic “1”	V_{MFIOOH}	2.2	-	-	V	[8] I_{MFIOOH} = –2 mA

(table continues...)

8 During active phase

Table 11 (continued) Electrical characteristics of MFIO pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum output sink current	I_{MFIOOL}	-	-	2	mA	8)
Maximum output source current	$-I_{MFIOOH}$	-	-	2	mA	8)
Output rise time (0 → 1)	$t_{MFIOrise}$	-	-	25	ns	20 pF load
Output fall time (1 → 0)	$t_{MFIOfall}$	-	-	25	ns	20 pF load

5.4.7 Hybrid-flyback current sensing (CS pin)

Table 12 Electrical characteristics of CS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{CSlk}	–10	-	10	µA	0 V < VCS < 2.8 V
Maximum operating current range	$V_{CSTHRmax}$	394	426	458	mV	
CSTHR propagation delay	$t_{CSTHRpd}$	121	213	305	ns	input signal slope, dVCS/dt = 150 mV/µs
CSPROT threshold	V_{CSPROT}	550	600	650	mV	

5.4.8 Hybrid-flyback output feedback (FB pin)

Table 13 Electrical characteristics of FB pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Open circuit output voltage	V_{FBoc}	3.04	3.2	3.36	V	
Threshold maximum usable range	$V_{FBOPmax}$	-	-	2.428	V	
Burst mode wake-up threshold	$V_{FBBMctrl}$	510	580	610	mV	During sleep phase in burst mode

5.4.9 LS gate driver (LSGD pin)

Table 14 Electrical characteristics of LSGD pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal output high voltage	$V_{LSGDhigh}$	9.9	10.5	11.1	V	I_{LSGD} = –20 mA

(table continues...)

8 During active phase

Table 14 (continued) Electrical characteristics of LSGD pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at active shutdown	$V_{LSGDaSD}$	-	-	1.6	V	I_{LSGD} = 5 mA, V_{VCC} = 5 V
Peak sink current	$I_{LSGDpksnk}$	800	-	-	mA	V_{LSGD} = 4.0 V
Peak source current	$-I_{LSGDpksrc}$	-	360	-	mA	
Driver output low impedance	R_{LSGDLS}	-	-	4.4	Ω	I_{LSGD} = 100 mA

5.4.10 Central control functions

Table 15 Electrical characteristics of central control functions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDP power supply	V_{VDDP}	3.04	3.2	3.36	V	
VREF reference voltage	V_{VREF}	2.391	2.428	2.465	V	
Main clock oscillation period time base	t_{MCLK}	15	15.8	16.6	ns	
Stand-by clock oscillation period time base	t_{STBCLK}	9	10	11.2	µs	
Slow task period time base	$t_{SLWTASK}$	111	120	129	µs	
Very slow task period time base	$t_{VSLWTASK}$	4.68	5	5.32	ms	
Sampling time period	t_{sample}	-	$t_{SLWTASK}$	-	µs	
Restart step time base for auto-restart mode	$t_{ARMbase}$	270	300	336	ms	Base for configurable auto-restart time t_{ARM} when auto-restart mode entered
Limited maximum change in on-time control for HS switch during CRM operation	$\Delta t_{HSonmaxCRM}$	75	80	85	ns	CRM operation, t_{HSon} not limited by V_{CSSET}, only applies for small V_{bus}
Blanking time for brown-out protection	t_{bo}	-	70	-	ms	

6 Package dimensions

You can find all of our packages, sorts of packing and others in our Infineon internet page “Products: http://www.infineon.com/products”.

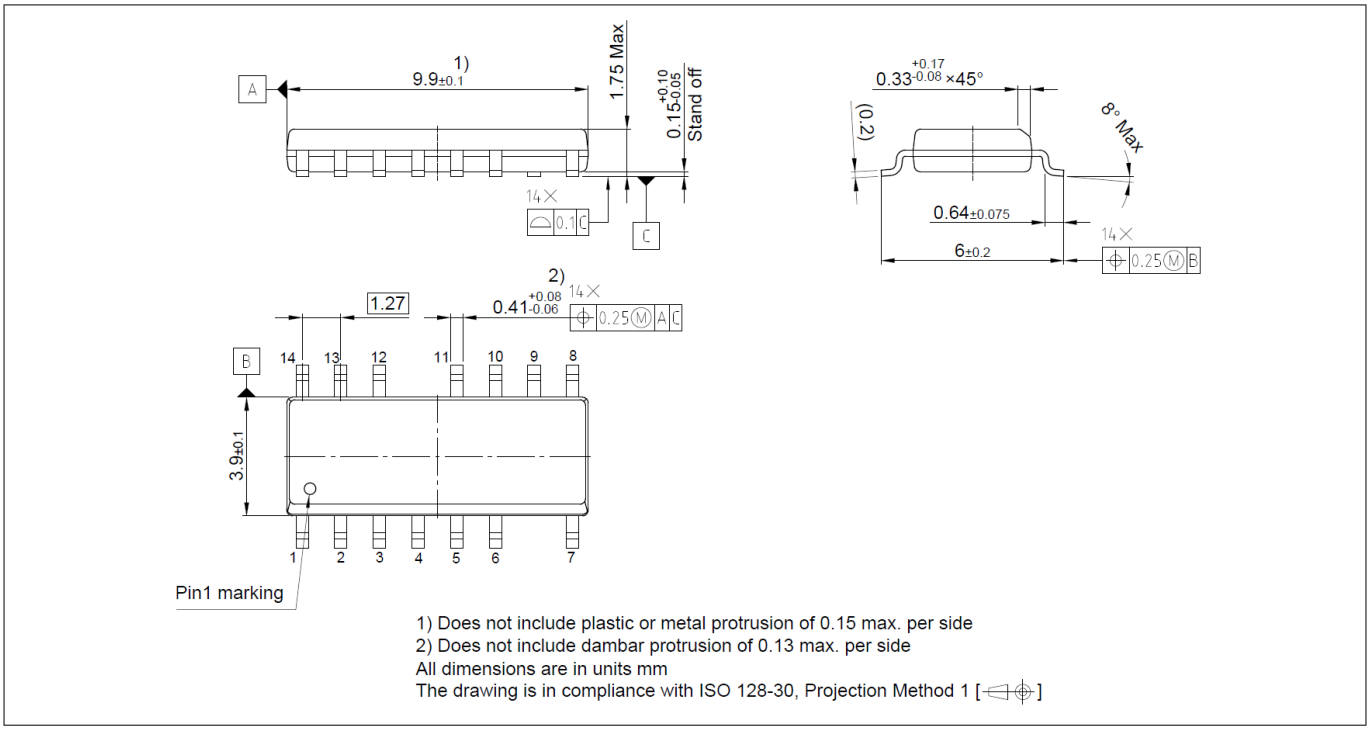

Figure 25 PG-DSO-14 outline

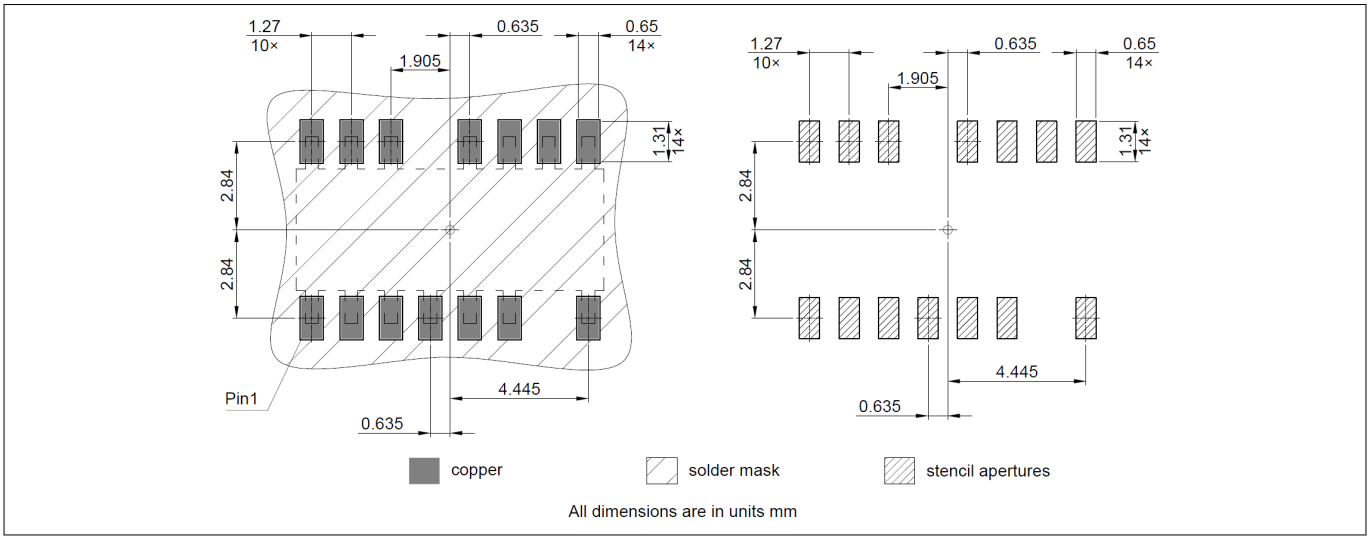

Figure 26 PG-DSO-14 footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

7 Revision history

Document version	Date of release	Description of changes
Rev 1.0	2025-02-18	Initial release

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