

**WUSB3801****USB Type-C Configuration Channel  
Flippable Adapter**<http://www.willsemi.com>**Description**

The WUSB3801 is a Type-C Configuration Channel (CC) Flippable Adapter chip with low power and high efficiency. The WUSB3801 supports channel identification of USB Type-C connector and auto detection of different power roles based on chip settings. This chip is compatible with USB Type-C Cable and Connector Specification Release 1.2 for varies of applications.

The WUSB3801 supports PIN control mode and I<sup>2</sup>C control mode through CTRL pin settings, and re-uses SDA (INOUT1)/SCL (INOUT2)/INTB (OUT3) pins to realize necessary functions in different control modes. ROLE pin is used for Source (SRC)/Sink (SNK)/Dual Role Power (DRP) mode selection of Type-C logic working state. The global enable signal comes from ENB pin with internal pull-up resistor for more feasibility.

**Applications**

- Smart-phones
- Laptops
- Tablets

**Features**

- USB Type-C Cable and Connector Specification Release 1.2 compatible
- Global power saving and active mode
- Pin or I<sup>2</sup>C controllable
- Support auto CC ports configuration
- Support SRC/SNK/DRP power mode
- Support DRP with Try.SNK or Try.SRC
- Support different current model controls and identifications (Default, 1.5A and 3.0A)
- Accurate internal CC termination resistance and current source with high precision
- High voltage EOS protection and DC 25V tolerance on CC1, CC2 and VBUSD pins
- Wide single power supply range: 2.7 ~ 5.5V
- QFN1616-12L packaging available (1.6x1.6x0.35mm)

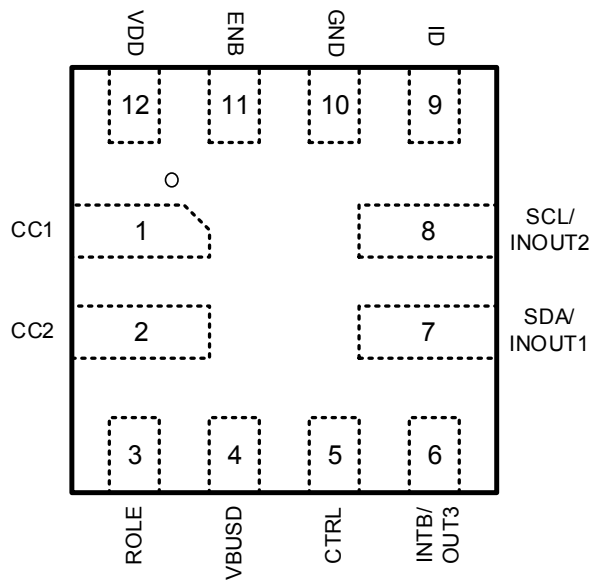
**Order Information**

Device	Package	Shipping
WUSB3801Q-12/TR	QFN1616-12L	3000/Reel&Tape

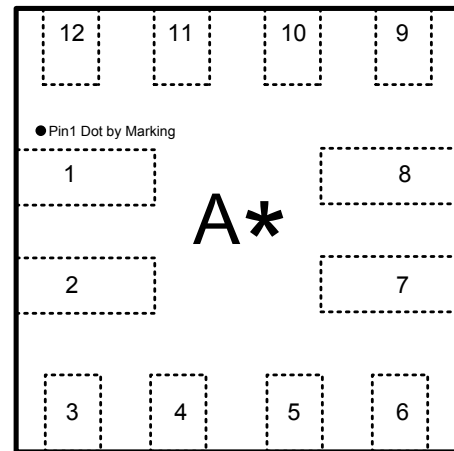
**Revision History**

Version	Date	Owner	Description
0.0	2015-03	Y. Shen	Initial draft
0.1	2015-03	Y. Shen	Support high voltage mode and ENB as global reset
0.2	2015-04	Y. Shen	Type-C 1.1 compatible
0.3	2015-08	Y. Shen	Update $I_{\text{host}}$ from 110 $\mu$ A to 122.5 $\mu$ A. Update $I_{\text{device}}$ from 28 $\mu$ A to 22.5 $\mu$ A
0.4	2015-10	Y. Shen	Support DRP with Try.SNK or Try.SRC
0.5	2015-11	Y. Shen	WUSB3801QB marking change from B* to G*
0.6	2015-11	Y. Shen	Add recommend land pattern
1.0	2016-05	X. Chen	Type-C 1.2 compatible Add general marking M Use a clear function description for ID pin Update high voltage DC from 20V to 25V Update ESD HBM from 3500V to $\pm 4000$ V Update ESD CDM from 1500V to $\pm 1500$ V Update USB Max tri-state input threshold from $V_{\text{DD}}-0.5$ to 2.9V Update $V_{\text{H}}$ and $V_{\text{L}}$ for logic threshold voltage from $0.8 \cdot V_{\text{DD}}$ to 1.05V and from $0.2 \cdot V_{\text{DD}}$ to 0.4V Update $V_{\text{th\_BUS}}$ from $0.78 \cdot V_{\text{DD}}$ to 3.2V Update $I_{\text{host max}}$ from 140 $\mu$ A to 160 $\mu$ A Correct figures for threshold of Comparison and Status Relationship Update all state diagrams based on chip functions Refine all descriptions and diagrams Remove repetitious descriptions as those in USB Type-C Specification

## Pin Configuration (Top View)

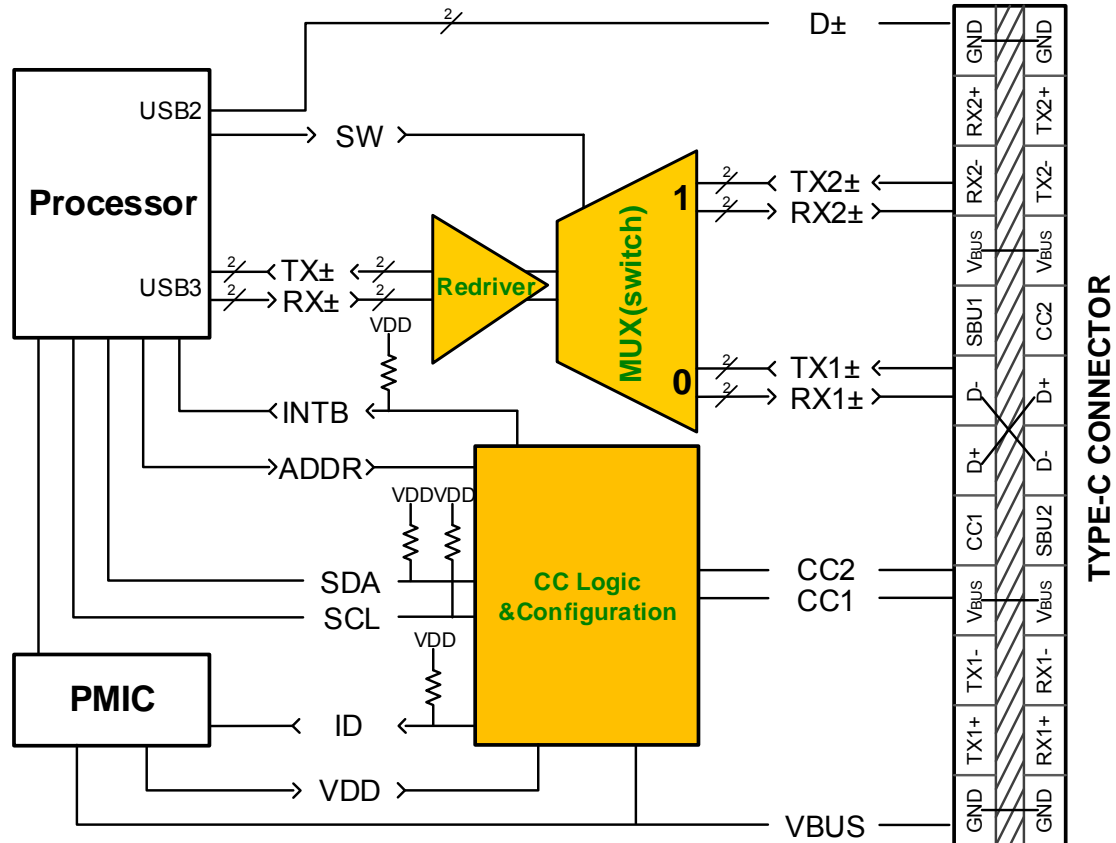


## Marking Information



**A** = Device Code  
**\*** = Month Code (A~Z)

## Application Block Diagram

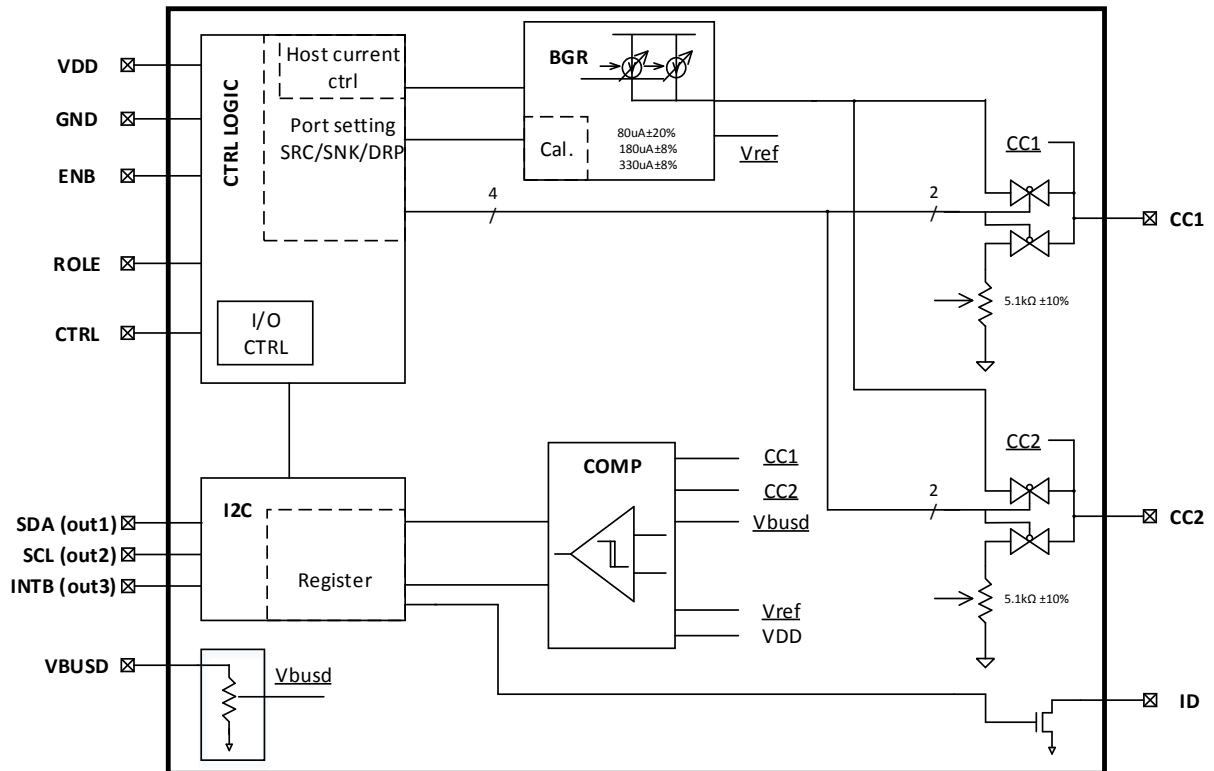


## Pin Descriptions

**Table 1. Pin Descriptions**

Pin	Name	Type	Function	Comments
1	CC1	I/O	Type-C CC logic channel signal High voltage EOS protection	Start from SNK when power on
2	CC2	I/O	Type-C CC logic channel signal High voltage EOS protection	Start from SNK when power on
3	ROLE	AI	Tri-state input control signal for working mode selection	Floating — DRP VDD — SRC GND — SNK
4	VBUSD	AI	V <sub>BUS</sub> detection and high voltage protection: DC 25V AC lighting surge	Detect V <sub>BUS</sub> voltage
5	CTRL	AI	Tri-state input control signal for PIN or I <sup>2</sup> C control mode selection	Floating — PIN control mode VDD — I <sup>2</sup> C control mode with control address 7b'1101000 GND — I <sup>2</sup> C control mode with control address 7b'1100000
6	INTB/ OUT3	DO	Interruption output signal for I <sup>2</sup> C control mode	INTB output Low active
			OUT3: Audio Acc. connection indication	H — No connection L — Audio Acc. connected
7	SDA/ INOUT1	I/O	I <sup>2</sup> C data input/output; INOUT1 and INOUT2 combined to identify the charging current mode when a SRC/SNK is connected	INOUT2 and INOUT1 in PIN control mode indications 2b'11 — Default
8	SCL/ INOUT2	I/O	I <sup>2</sup> C clock input; INOUT1 and INOUT2 combined to identify the charging current mode when a SRC/SNK is connected	2b'10 — 1.5A 2b'00 — 3.0A 2b'01 — No connection
9	ID	AO	Open drain output signal for SRC or DRP operating as SRC	Output Low when detects CC channel is connected as SRC or DRP operating as SRC
10	GND	G	Global ground	—
11	ENB	AI	Global enable signal	H — Power saving L — Active
12	VDD	P	Power	2.7 ~ 5.5V

## Block Diagram



## Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Description	Range	Unit
$V_{\text{BUSD}}$	$V_{\text{BUS}}$ pin voltage	-0.3 ~ 25	V
$V_{\text{CCx}}$	CC pin voltage	-0.3 ~ 25	V
$V_{\text{DD}}$	Power supply	-0.3 ~ 6.0	V
$V_{\text{IO}}$	Input IO voltage	-0.3 ~ 3.6	V
$T_{\text{sto}}$	Storage temperature	-65 ~ 150	°C
$V_{\text{HBM}}$	ESD HBM	±4000	V
$V_{\text{CDM}}$	ESD CDM	±1500	V

The range is for stress ratings only. Stress exceeding the range specified in the Absolute Maximum Ratings may cause substantial damage to the device. Prolonged exposure to extreme conditions within the range may also affect device reliability.

## Recommended Operation Conditions

Table 3. Recommended Operation Conditions

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
$V_{\text{DD}}$	Power supply	-	2.7	-	5.5	V
$V_{\text{EN\_L}}$	ENB pin Low voltage level	$V_{\text{DD}}=3.6\text{V}$	-	-	0.4	V
$V_{\text{EN\_H}}$	ENB pin High voltage level	$V_{\text{DD}}=3.6\text{V}$	1.15	-	-	V
$V_{\text{ID\_L/}}/$ $V_{\text{INTB\_L}}$	ID/INTB pin Low voltage level Open drain output	$V_{\text{DD}}=3.6\text{V}$ $I_{\text{Sink}} = -2\text{mA}$	-	-	0.4	V
$V_{\text{IO3\_th}}$	USB tri-state input threshold	$V_{\text{DD}}=3.6\text{V}$	0.7	-	2.9	V
$T_{\text{j}}$	Junction temperature	-	-40	-	125	°C

**Electronics Characteristics ( $V_{DD}=3.6V$ ,  $T_a=25^{\circ}C$ , unless otherwise noted)**
**Table 4. Electrical Characteristics**

Parameters	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Active current	$I_{DD\_active}$	ENB=Low CC pins unattached	-	22.5	45	$\mu A$
		ENB=Low In Attached.SRC state Default current mode	-	122.5	160	$\mu A$
Power saving current	$I_{DD\_disab}$	ENB=High	-	-	1	$\mu A$
Logic threshold voltage	$V_H$	$V_{DD}=3.6V$	1.05	-	-	V
	$V_L$	$V_{DD}=3.6V$	-	-	0.4	V
Current source	$I_H$	3.0A mode setting	304	330	356	$\mu A$
	$I_M$	1.5A mode setting	166	180	194	$\mu A$
	$I_D$	Default mode setting	64	80	96	$\mu A$
Resistor load	$R_d$	-	4.6	5.1	5.6	$k\Omega$
Comparator threshold voltage	$V_{th\_H}$	3.0A mode setting	1.16	1.23	1.31	V
	$V_{th\_M}$	1.5A mode setting	0.61	0.66	0.70	V
	$V_{th\_D}$	Default mode setting	0.15	0.2	0.25	V
$V_{BUS}$ detection threshold voltage	$V_{th\_BUS}$	$V_{DD}=3.6V$	2.9	3.2	3.5	V

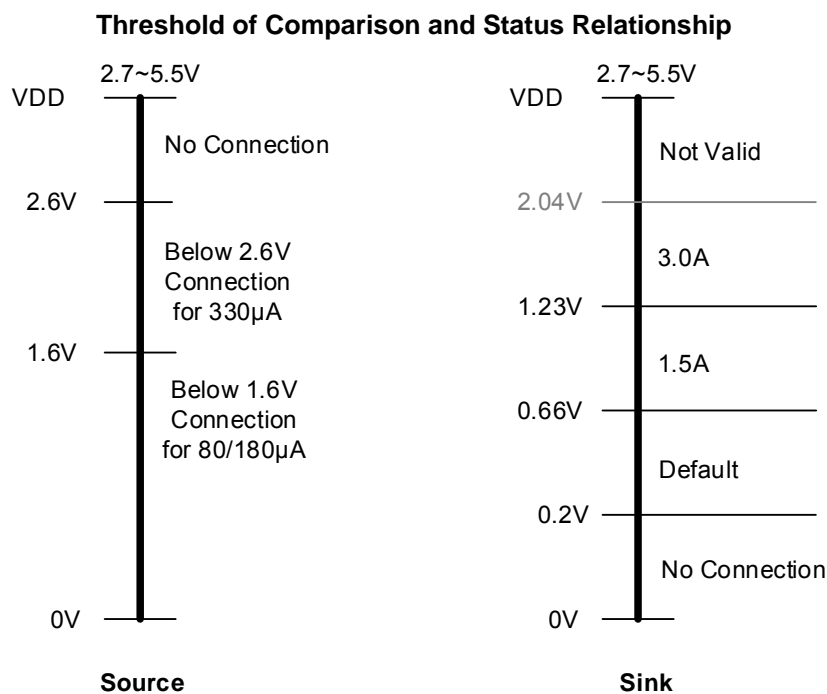
## Function Descriptions

### General Description

The WUSB3801 is a Type-C Configuration Channel Flippable Adapter chip with low power and high efficiency. The WUSB3801 supports channel identification of USB Type-C connector and auto detection of different power roles based on chip settings. It has high voltage protection circuits on CC1/CC2/VBUSD pins and supports both DC up to 25V and AC lighting surge. This chip is compatible with USB Type-C Cable and Connector Specification Release 1.2 for varies of applications.

### Logic Control Block

The logic control block receives the outer control signals, detects CC connection status using voltage level comparisons of CC pins for different connection topologies and settings, and outputs the detected information of communication path. Comparison results showing CC signals voltage range are sent to logic control block for state machine and then the connection status of related working mode will be identified. When connection status changes, the logic control block will update outputs of pins and registers. The figures as below show the boundaries of status.

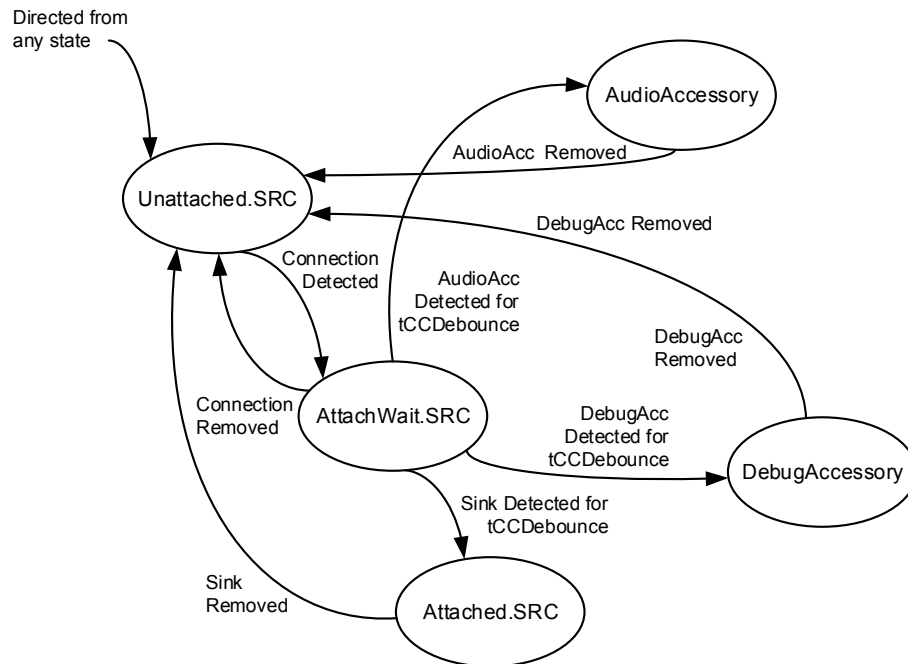




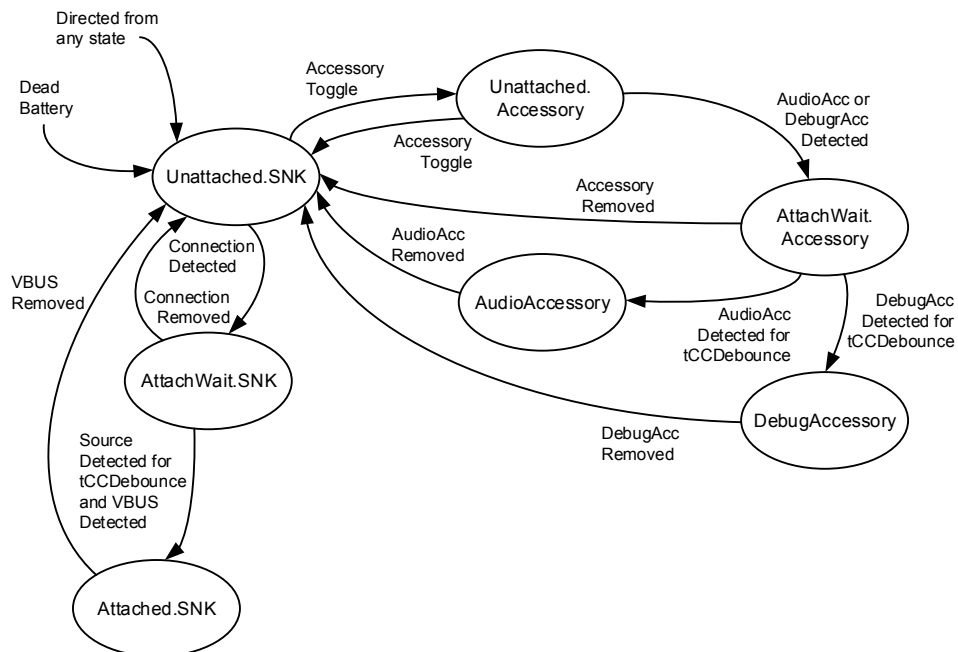
## Work Mode Feature

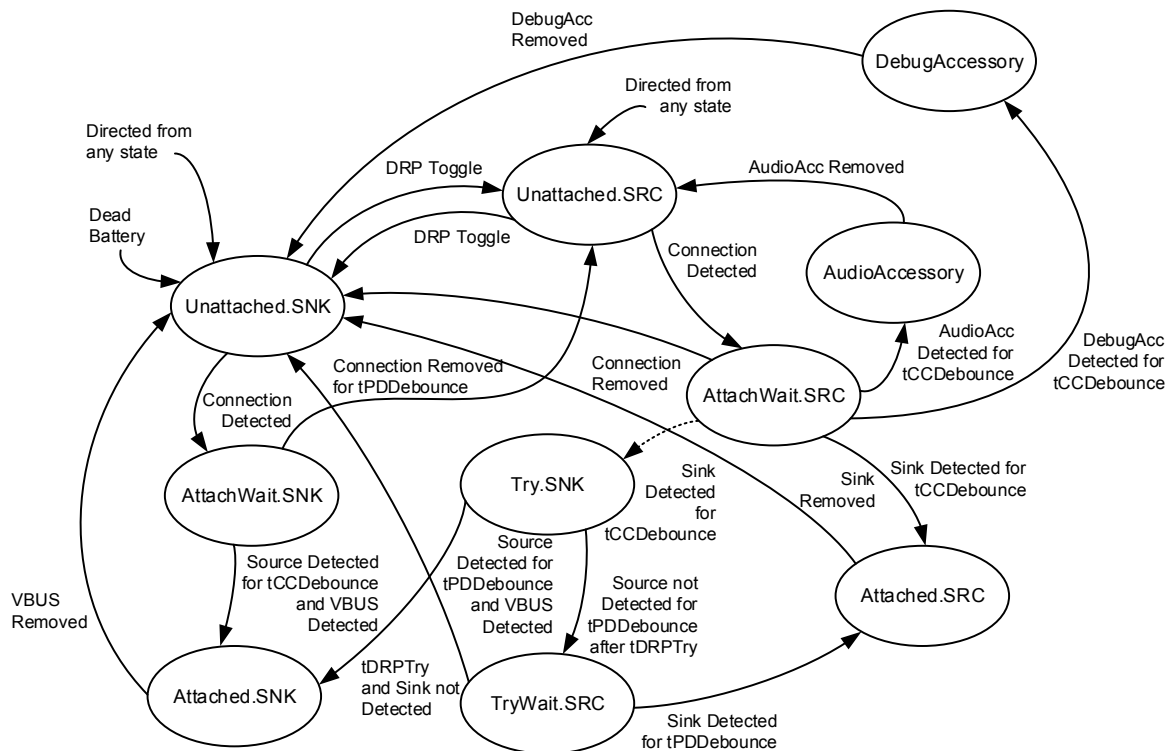
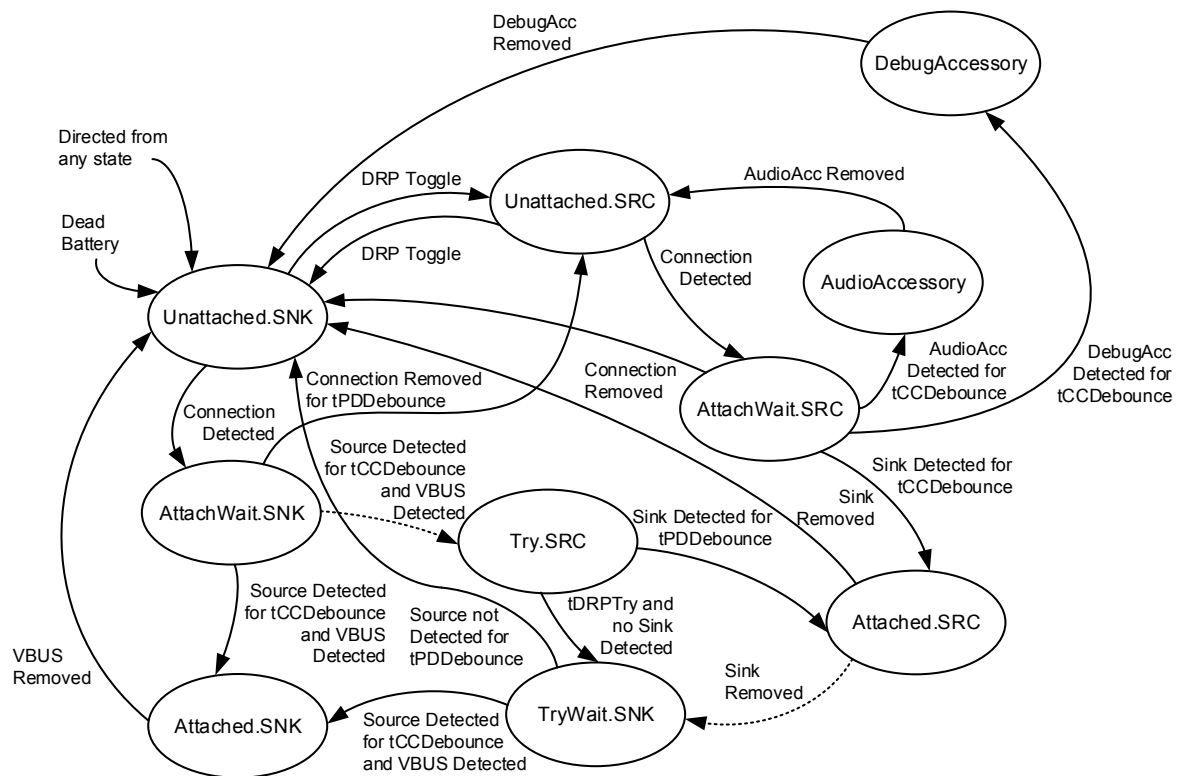
According to CC connection status and detection results, the chip can work as SRC (Host), SNK (Device) or DRP mode which are shown in the following figures.

**SRC State Diagram**



**SNK with Accessory Support State Diagram**





## Communication Interfaces

### I<sup>2</sup>C Interface

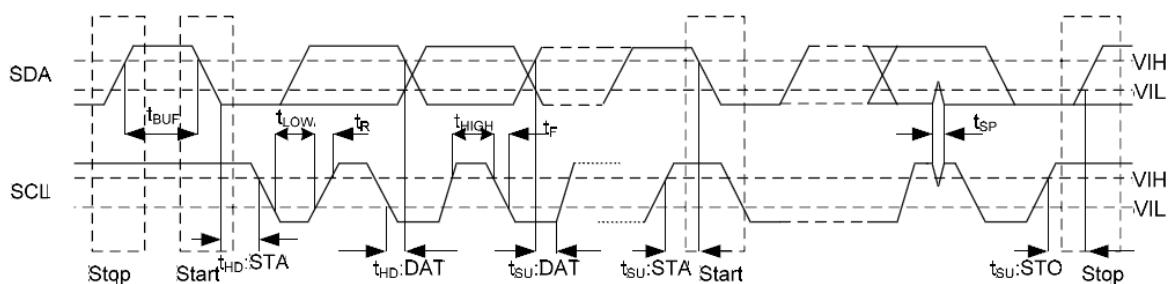
The chip can take communications over I<sup>2</sup>C bus which supports up to 400 kHz clock when CTRL pin is not floating (connected to VDD or GND). Two setting values would result in different I<sup>2</sup>C device addresses as shown in Table 7.

**Table 7. Address Table Controlled by CTRL Pin**

	Pin Setting	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
Address 1	VDD	1	1	0	1	0	0	0
Address 2	GND	1	1	0	0	0	0	0

### I<sup>2</sup>C Bus Timing

**I<sup>2</sup>C BUS Timing Diagram**



Electrical Characteristics of I<sup>2</sup>C

Table 8. Electrical Characteristics of I<sup>2</sup>C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f <sub>SCL</sub>	SCL clock frequency	-	-	-	400	kHz
V <sub>DD_I2C</sub>	Power supply range for I <sup>2</sup> C	-	1.65	-	3.6	V
V <sub>IH</sub>	Logic high level voltage (Note 1)	-	1.2	-	-	V
V <sub>IL</sub>	Logic low level voltage (Note 1)	-	-	-	0.4	V
I <sub>sink</sub>	Sink current at low level (open drain) (Note 1)	-	-	1.6	-	mA
t <sub>BUF</sub>	Bus free time between a STOP and START condition	-	1.3	-	-	μs
t <sub>HD_STA</sub>	Hold time START condition. After this period, the first clock pulse is generated	-	0.6	-	-	μs
t <sub>LOW</sub>	LOW period of the SCL clock	-	1.3	-	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	-	0.6	-	-	μs
t <sub>SU_STA</sub>	Set-up time for a repeated START condition	-	0.6	-	-	μs
t <sub>HD_DAT</sub>	Data hold time between SDA and SCL falling edge	-	0	-	-	μs
t <sub>SU_DAT</sub>	Data set-up time	-	100	-	-	ns
t <sub>r</sub>	Rise time for SDA and SCL signals (Note 2)	-	-	-	300	ns
t <sub>f</sub>	Fall time for SDA and SCL signals (Note 2)	-	-	-	300	ns
t <sub>SU_STO</sub>	Set-up time for STOP condition	-	0.6	-	-	μs
T <sub>deg</sub>	Width of deglitch at input termination	SCL	-	200	-	ns
		SDA	-	250	-	ns
C <sub>b</sub>	Capacitive load for each bus line	-	-	-	400	pF

Note 1: Guaranteed by design

Note 2: t<sub>r</sub> and t<sub>f</sub> are timing from 0.3\*VDD to 0.7\*VDD

**I<sup>2</sup>C Register Map**
**Table 9. I<sup>2</sup>C Register Map**

Addr.	Register	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01H	Device ID	R	Version ID: 00010					Vendor ID: 110		
02H	Control	R/W	Acc. Support	Try SNK/SRC		Current Mode (SRC)		Work Mode		Interruption Control
			0: Yes 1: No	01: Try.SNK 10: Try.SRC 00/11: No Try		00: Default 01: 1.5A 10: 3.0A		00: SNK 01: SRC 10: DRP		1
03H	Interruption	R / Clear	Reserved						Detach/Attach	
									00: No Interruption 01: Attached 10: Detached	
04H	CC Status	R	V <sub>BUS</sub> Detection as SNK	Charging Current Detection as SNK		Plugged Port Status		Plug Orientation		
			0: V <sub>BUS</sub> not detected 1: V <sub>BUS</sub> detected	00: Standby 01: Default 10: 1.5A 11: 3.0A		000: Standby 001: SNK 010: SRC 011: Audio Accessory 100: Debug Accessory		00: Standby 01: CC1 connected 10: CC2 connected 11: CC1 and CC2 connected		

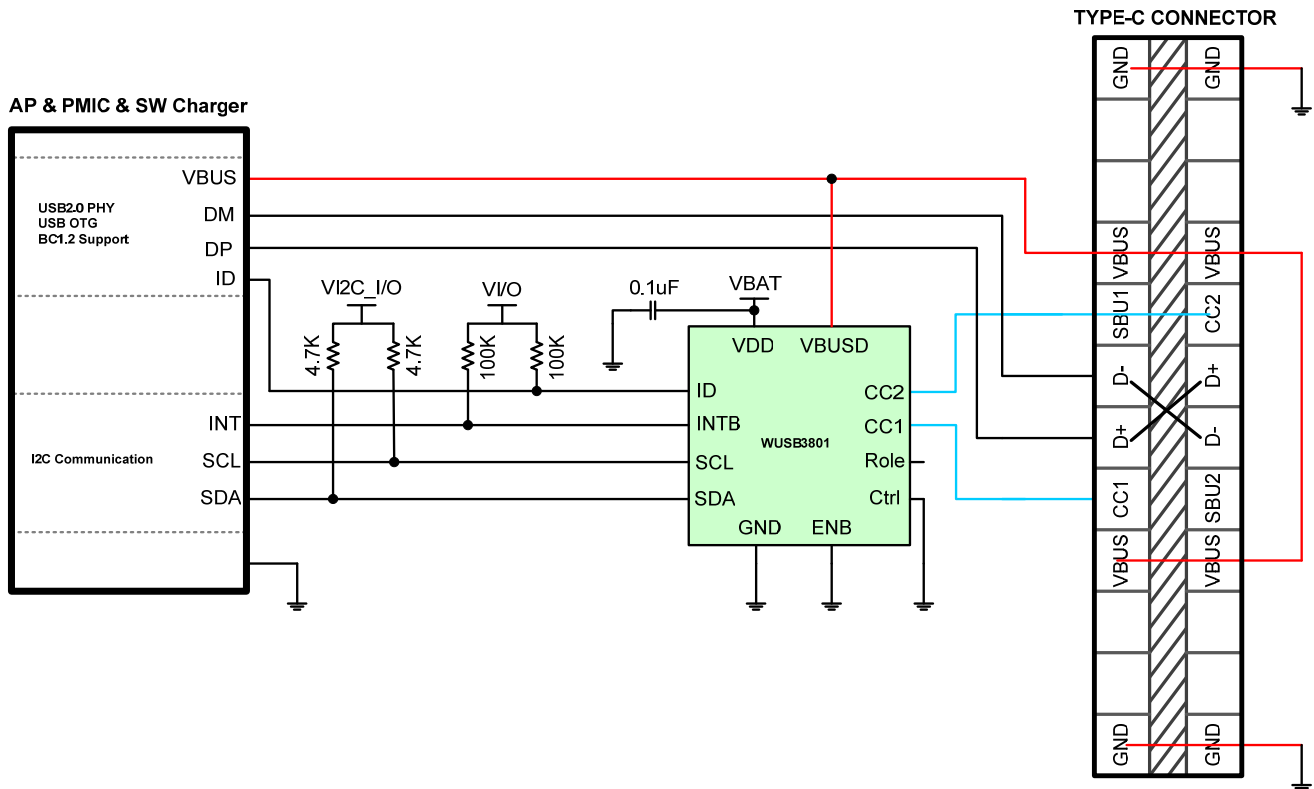
**Function Description**

Registers are used for read/write settings in I2C control mode.

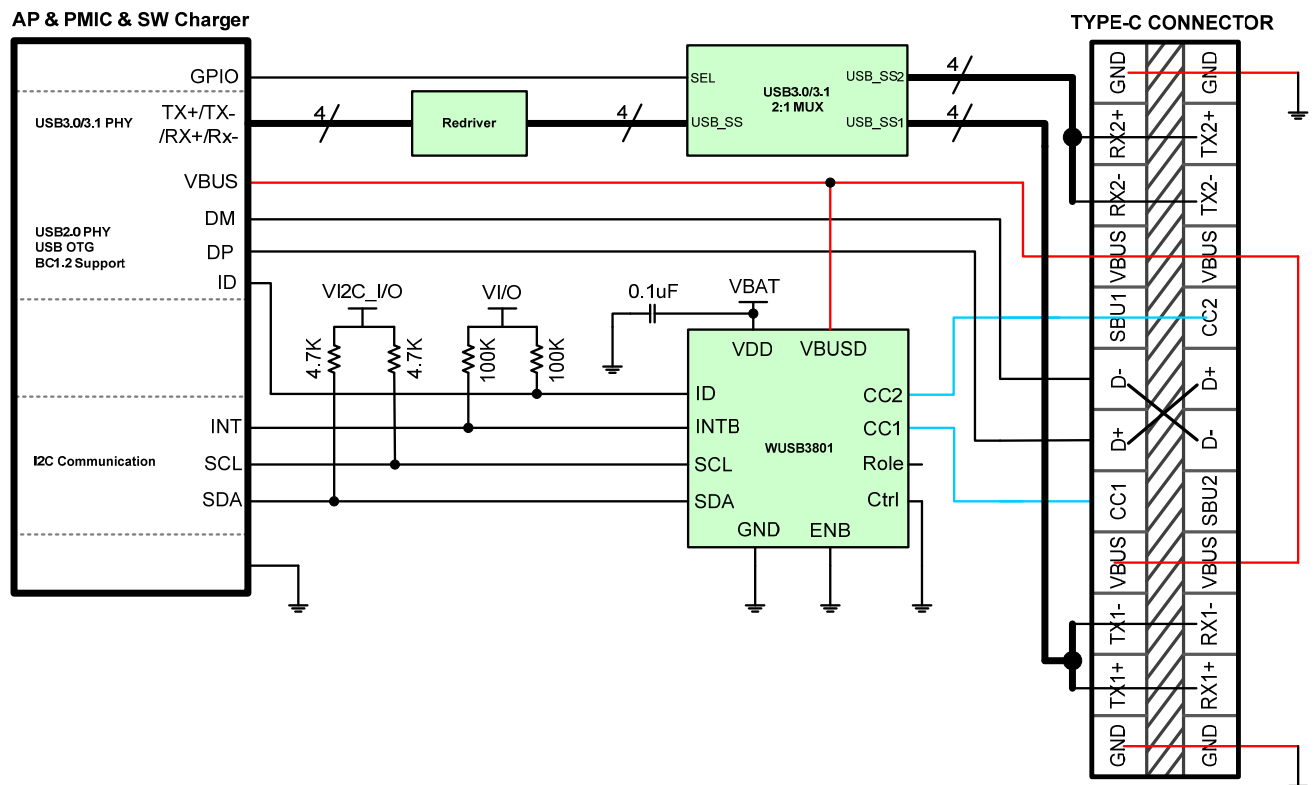
Status of USB Type-C connector is detected and updated in register map automatically by internal state machine. When any update occurs in register map after the last I2C reads, the chip would keep the interruption pin (INTB) at low level. Otherwise, the chip would cancel the interruption signal (INTB=1).

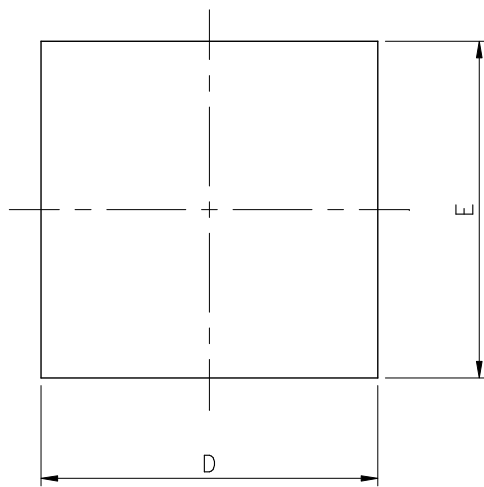
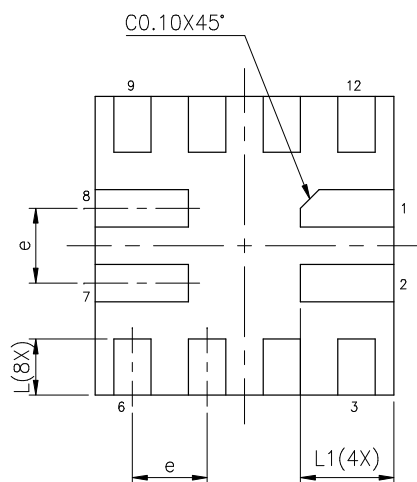
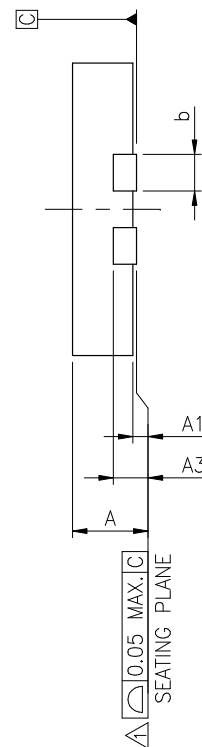
## Typical Application Schematics

### DRP Mode for I<sup>2</sup>C Control with USB2.0

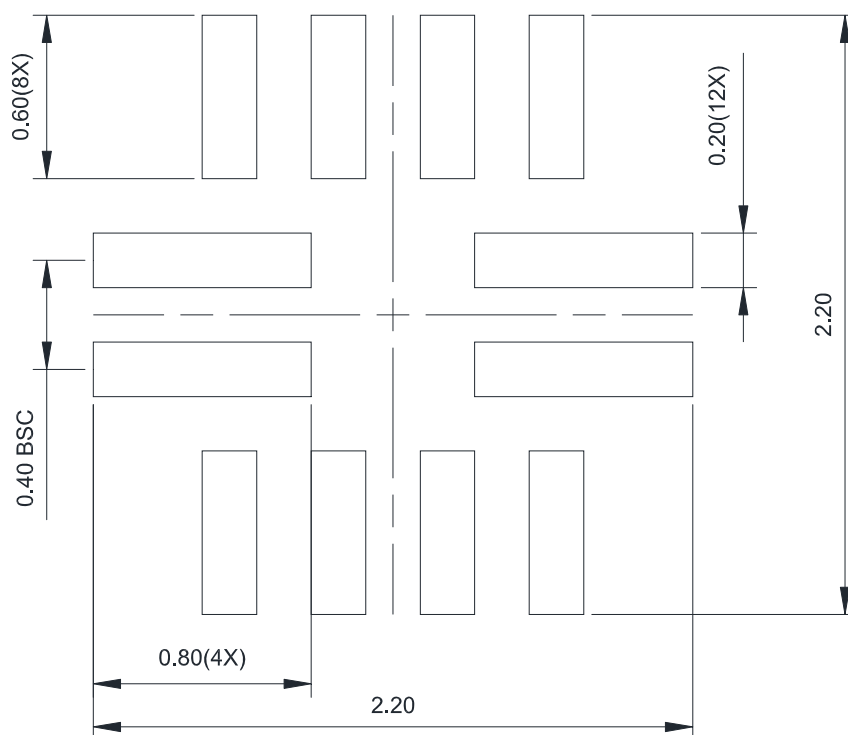


### DRP Mode for I<sup>2</sup>C Control with USB3.0/3.1



**Package Outline Dimensions**
**QFN1616-12L**

**Top View**

**Bottom View**

**Side View**

Symbol	Dimensions in millimeter		
	MIN.	NOM.	MAX.
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
A3	0.127 Ref.		
b	0.15	0.20	0.25
D	1.55	1.60	1.65
E	1.55	1.60	1.65
e	0.40 BSC.		
L	0.25	0.30	0.35
L1	0.45	0.50	0.55

**Recommend Land Pattern**

**RECOMMENDED LAND PATTERN**

**All dimensions are in millimeters**