



偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT7522

POWER SUPPLY PWM SUPERVISOR

Data Sheet

Version 1.10

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GENERAL DESCRIPTION

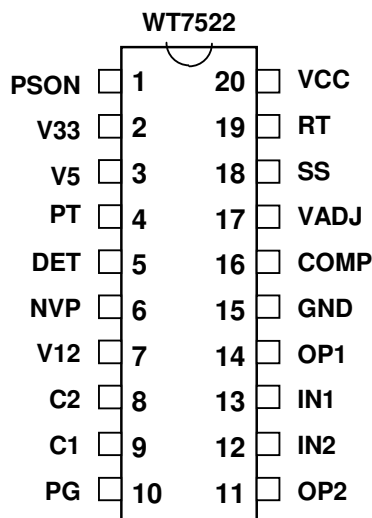
The WT7522 is a pulse-width modulation (PWM) control circuit with complete protection circuits for used in the SMPS (Switched Mode Power Supply). It contains various functions, which are Over Voltage Protection, Under Voltage Protection, Power Good Output (PG), Remote On/Off control, Opamp and etc. It can minimize external components of switching power supply systems in personal computer.

Over Voltage Protection (OVP) monitors 3.3V, 5V, 12V and PT input voltage level. Under Voltage Protection (UVP) monitors 3.3V, 5V, 12V and one negative voltage input voltage level. Power Good Output monitors the voltage level of power supply.

FEATURES

- Complete PWM Control and Protection Circuitry
- Over Voltage Protection for 3.3V / 5V / V12 / PT
- 3.3V / 5V / 12V Under Voltage Warning for PG Low
- Under Voltage Protection for 3.3V / 5V / V12
- Two Opamp loop function
- 300ms PG Time Delay
- Power Good Output is Open Drain Output
- Push-pull PWM Output
- Remote ON/OFF function De-bounce Time
- Soft-Start function built-in
- 20-Pin Dual In-line Package

PIN CONFIGURATION

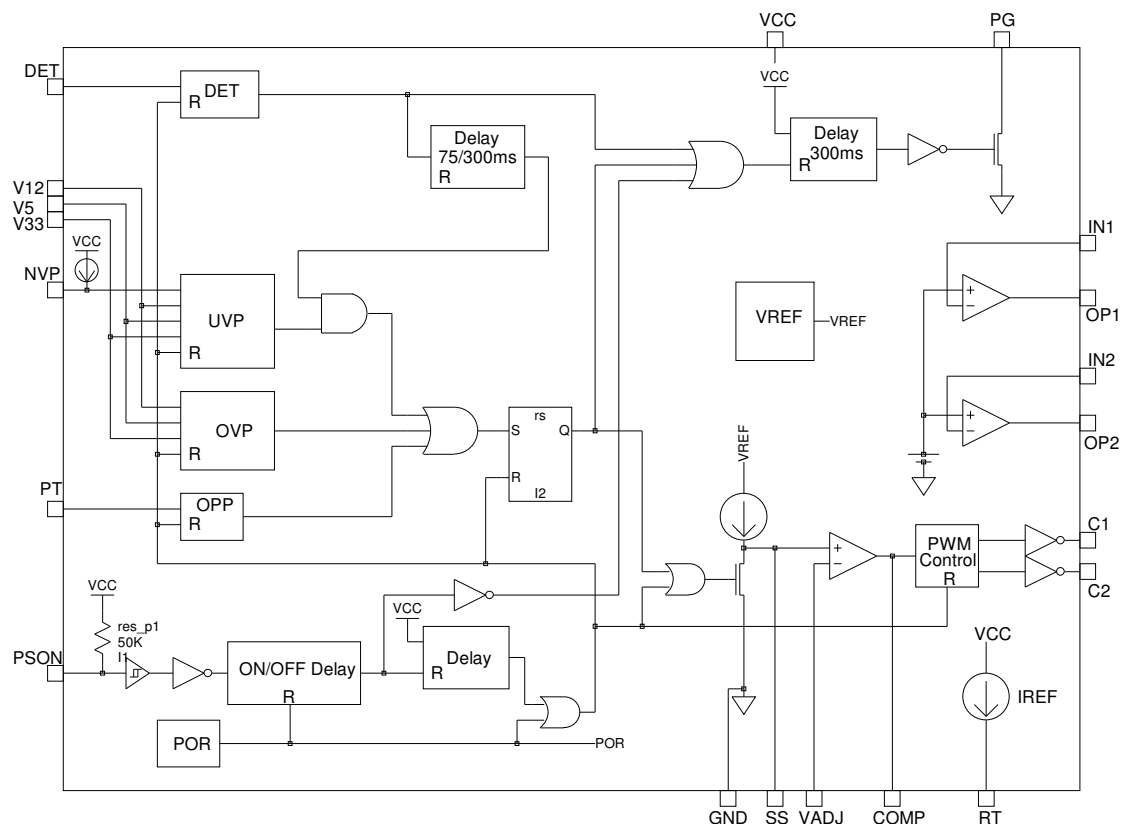


Ordering Number	Package Type
WT7522-NG200WT	Green DIP 20
WT7522-NN200WT	Pb free DIP 20

PIN DESCRIPTION

Pin No.	Pin Name	TYPE	FUNCTION
1	PSON	I	Remote on/off input. PSON="low" that means the main SMPS is turned-on. PSON="high", the main SMPS is turned-off.
2	V33	I	OVP/UVLP sense input FOR 3.3V.
3	V5	I	OVP/UVLP sense input for 5V.
4	PT	I	Over-power sense input.
5	DET	I	Power good detection input.
6	NVP	I	UVP sense input for negative voltage.
7	V12	I	OVP/UVLP sense input for 12V.
8	C2	O	PWM totem-pole output.
9	C1	O	PWM totem-pole output.
10	PG	O	Power good signal. PG= "high" means "power good".
11	OP2	O	Output for second Opamp loop.
12	IN2	I	Input for second Opamp loop.
13	IN1	I	Input for first Opamp loop.
14	OP1	O	Output for first Opamp loop.
15	GND	P	Ground
16	COMP	O	Error amplifier output.
17	VADJ	I	Input of error amplifier.
18	SS	I	The soft-start function set through an external capacitor.
19	RT	I	Reference setting by an external resistor.
20	VCC	P	Supply voltage.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS, VCC=5.5V

CHARACTERISTICS	SYMBOL	VALUE	Unit
Supply voltage	VCC	5.5	V
Power dissipation	Pd	200	mW
Operating temperature	Topr	-25 ~ +85	°C
Storage temperature	Tstg	-55 ~ +150	°C
PIN Voltage	V33,V5	-0.3 ~ (VCC+0.3)	V
	PSON,IN1,IN2,PT,DET, RT,NVP,VADJ,COMP,PG,SS	-0.3 ~ (VCC+0.3)	V
	V12,C1,C2,OP1,OP2	-0.3 ~ 16	V
I _{SINK}	Sink current at OP1,OP2,PG pin	30	mA

ELECTRICAL CHARACTERISTICS, $T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$,

CHARACTERISTICS	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	Unit
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TOTAL DEVICE

STANDBY SUPPLY CURRENT	I_{VCC}	PG=High		5	10	mA
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ERROR AMP SECTION

OPEN LOOP VOLTAGE GAIN				90		dB
UNIT GAIN BANDWIDTH				1		MHz
REFERENCE VOLTAGE			2.46	2.5	2.54	V

PROTECTION SECTION

OVER VOLTAGE PROTECTION (OVP)	V33		3.9	4.1	4.3	V
	V5		5.8	6.1	6.5	V
	V12		13.9	14.5	14.9	V
UNDER VOLTAGE SENSE for PG Low (UVS)	V33		2.5	2.8	3.0	V
	V5		4.0	4.3	4.5	V
	V12		9.4	10.1	10.4	V
UNDER VOLTAGE PROTECTION (UVP)	V33		2.0	2.6	2.8	V
	V5		3.0	3.6	3.9	V
	V12		6.0	7.2	8.0	V
PT Protection with Delay Time	V_{PT}		2.02	2.4	2.66	V
Negative Voltage Protection (NVP)	V_{NVP}	Note 1	2.0	2.1	2.2	V
NVP Source current	I_{NVP}	RT=75K Ω	63	67	71	μA
OVP Debounce Time	T_{OVP}	RT =75K Ω	0.37	0.7	1.35	ms
UVP Debounce Time	T_{UVP}	RT =75K Ω	0.8	2.4	3.75	ms
UVS Debounce Time	T_{UVS}	RT =75K Ω	0.37	1.2	1.88	ms
Debounce Timing of NVP	T_{NVP}	RT =75K Ω	1.65	3.5	5.1	ms
PT Debounce Time	T_{PT}	RT =75K Ω	1.65	3.5	5.1	ms

Note 1 : $V_{NVP} > 2.1$ (TYP) => Protection

REMOTE ON/OFF SECTION

PSON HIGH INPUT VOLTAGE	V_{PSONH}		2.0			V
PSON LOW INPUT VOLTAGE	V_{PSONL}				0.8	V
PSON to ON Debounce TIME	T_{PSON_ON}	RT =75K Ω	30	40	50	ms
PSON to OFF Debounce TIME	T_{PSON_OFF}	RT =75K Ω	7	14	21	ms
PSON to OFF DELAY TIME	T_{OFF}	RT =75K Ω	1.5	2	6.3	ms

POWER GOOD SECTION

DET SENSE VOLTAGE	V_{DET}		0.68	0.7	0.72	V
PG DELAY TIME	T_{PG}	RT =75 K Ω	200	300	400	ms
OUTPUT LOW VOLTAGE	V_{PGL}	$I_{PG}=5\text{mA}$			0.5	V
SINK CURRENT OF PG	I_{PG}				30	mA
Internal UVP Delay Time (RT=75K Ω) (Power On Mode) (Note 3)		$V_{DET} > 0.7\text{V}$	50	75	100	ms
		$V_{DET} < 0.7\text{V}$	200	300	400	ms
UVP disable Voltage (Normal Mode)	V_{DET}	$V_{DET} < 0.7\text{V}$	0.68	0.7	0.72	V

Note 3 : When SS go High will enter Power On Mode at first and then jump to Normal Mode when PG are right



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CHARACTERISTICS	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	Unit
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SOFT START SECTION

CHARGE CURRENT OF SS	I_{SS}	$R_T = 75\text{ K}\Omega$	7	8	9	μA
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OSCILLATION SECTION

OSCILLATION FREQUENCY	F_{OSC}	$R_T = 75\text{ K}\Omega$		65		KHZ
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OPAMP SECTION

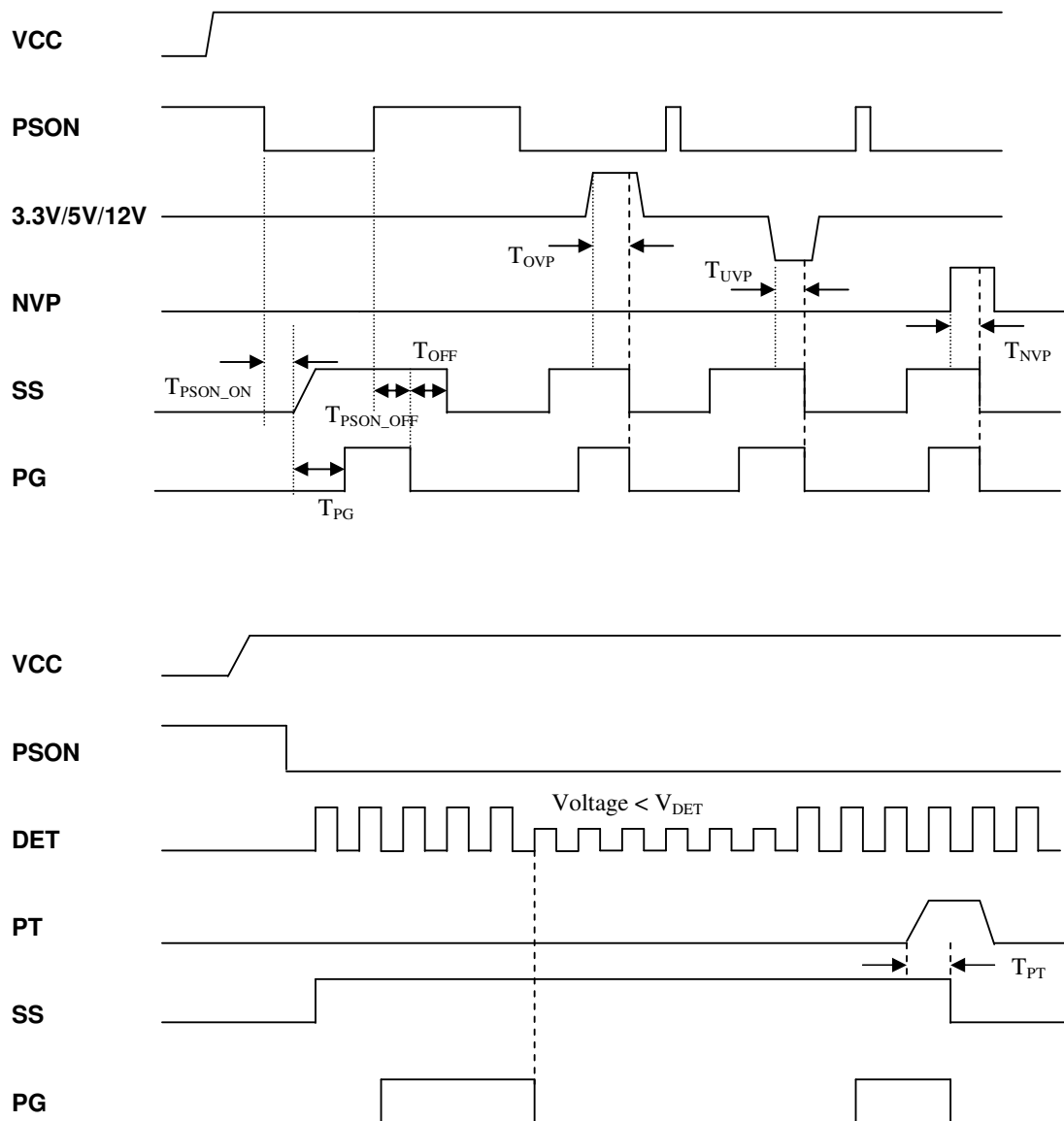
Reference Voltage	V_{REF}		2.475	2.5	2.525	V
SINK CURRENT OF OP	I_{OP}				30	mA

PWM OUTPUT SECTION

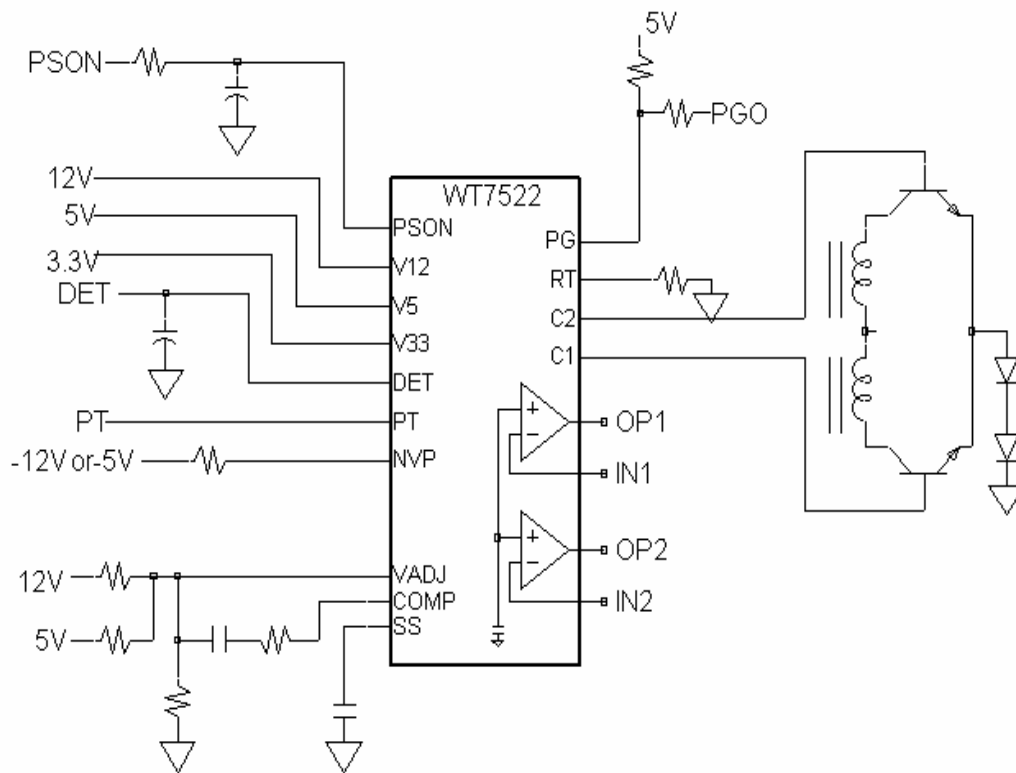
SINK CURRENT OF C1, C2	I_{C1}, I_{C2}				20	mA
Output Voltage Low	V_{OL}	$I_O = 20\text{ mA}$			0.8	V
Output Voltage High	V_{OH}	$V_{I2} = 12\text{ V}$	4			V

TIMING DIAGRAM

1. PSON ON/OFF :

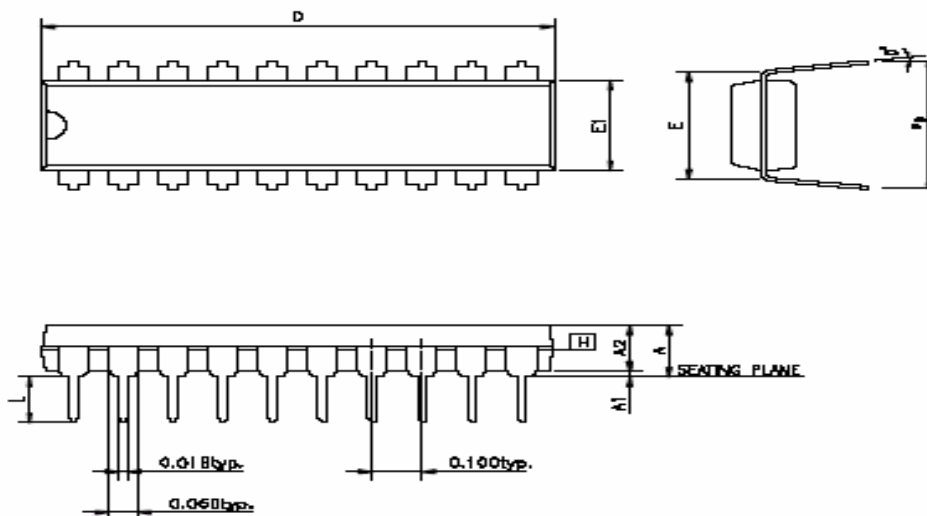


APPLICATION :



MECHANICAL INFORMATION

PLASTIC DUAL-IN-LINE PACKAGE



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	0.98	1.030	1.060
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e _B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 AD
2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. e_B IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

NOTE 1 : All linear dimensions are in inches (millimeters) .

NOTE 2 : This drawing is subject to change without notice.

NOTE 3 : Falls within JEDEC MS-001