

## Description

The WSD30L20DN uses advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application

#### **Features**

- 1,High density cell design for ultra low Rdson
- 2, Fully characterized avalanche voltage and current
- 3,Good stability and uniformity with high EAS
- 4,Excellent package for good heat dissipation

#### **Product Summery**

VDS	RDS(ON)	ID
-30	18.8mΩ	-20A

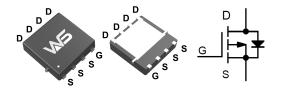
### **Application**

Lithium battery protection

Wireless impact

Mobile phone fast charging

## **DFN3X3-8-EP Pin Configuration**



## Absolute Maximum Ratings (Tc=25°Cunless otherwise noted)

Symbol	Parameter		Rating	Units	
VDS	Drain-Source Voltage		-30	V	
Vgs	Gate-Source Voltage		±20	V	
ID	Continuous Drain Current, Vos @ -10V1	TC=25℃	-20	А	
ID	Continuous Drain Current, Vos @ -10V₁ TC=100°C		-13	А	
Ірм	Pulsed Drain Current <sub>2</sub>		-80	А	
EAS	Single Pulse Avalanche Energy <sub>3</sub>		16	mJ	
las	Avalanche Current		-17	А	
PD	Total Power Dissipation4	TC=25℃	16.6	W	
	Total Power Dissipation4	TA=25℃	1.67	W	
Тѕтс	Storage Temperature Range		-55 to 150	°C	
Tı	Operating Junction Temperature Range		-55 to 150	°C	
Reja	Thermal Resistance Junction-Ambient 1		7.53	°C/W	





# Electrical Characteristics (Tc=25 ℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-30	32		V
△BVDSS/△TJ	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25℃, I <sub>D</sub> =-1mA		-0.022		V/°C
RDS(ON)	Static Drain-Source On-Resistance	Vgs=-10V , Ip=-10A		18.8	25	· mΩ
	Static Dialii-Source Off-Resistance	Vgs=-4.5V , ID=-5A		30.5	40	11122
VGS(th)	Gate Threshold Voltage	Vgs=Vps , Ip =-250uA	-1.2	-1.7	-2.5	V
$\triangle V$ GS(th)	V <sub>GS(th)</sub> Temperature Coefficient	VGS-VDS, ID250UA		4.6		mV/℃
	Drain-Source Leakage Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			-1	- uA
IDSS		V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		8.9		Ω
Qg	Total Gate Charge (-4.5V)			19		nC
Qgs	Gate-Source Charge	V <sub>DS</sub> =-15V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =- 15A		6.3		
Qgd	Gate-Drain Charge			4.5		
Td(on)	Turn-On Delay Time			6		ns
Tr	Rise Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V , R <sub>G</sub> =3.3Ω,		5		
Td(off)	Turn-Off Delay Time	ID=-15A		25		
Tf	Fall Time			7		
Ciss	Input Capacitance			900		pF
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		140		
Crss	Reverse Transfer Capacitance			120		
IS	Continuous Source Current	VV0V Force Correct			-20	Α
ISM	Pulsed Source Current	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-80	Α
VSD	Diode Forward Voltage	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25℃			-1.2	V
trr	Reverse Recovery Time	IF=-15A , dl/dt=100A/μs ,		7		nS
Qrr	Reverse Recovery Charge	TJ=25℃		6.3		nC

### Note:

- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300 \text{us}$  , duty cycle  $\leq 2\%$
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =-24V, $V_{GS}$ =-10V,L=0.1mH, $I_{AS}$ =-17A
- 4.The power dissipation is limited by 150 ℃ junction temperature
- 5. The data is theoretically the same as  $l_D$  and  $l_{DM}$ , in real applications, should be limited by total power dissipation.



## **Typical Characteristics**

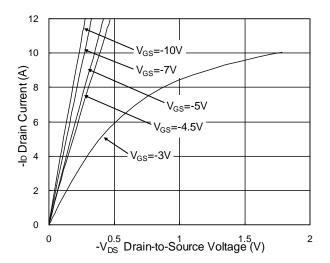


Fig.1 Typical Output Characteristics

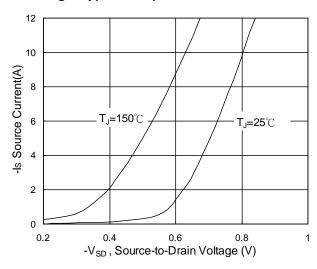


Fig.3 Forward Characteristics of Reverse

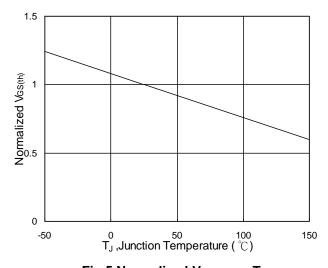


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$ 

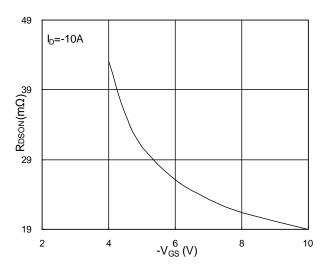


Fig.2 On-Resistance v.s Gate-Source

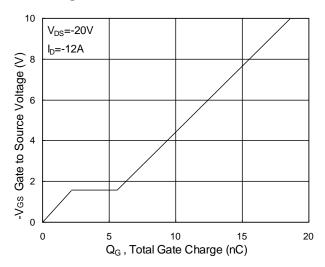


Fig.4 Gate-Charge Characteristics

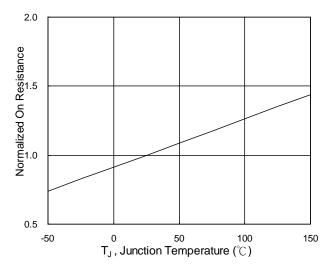
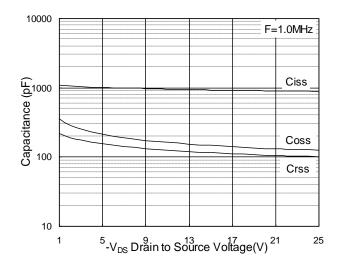


Fig.6 Normalized R<sub>DSON</sub> v.s T<sub>J</sub>





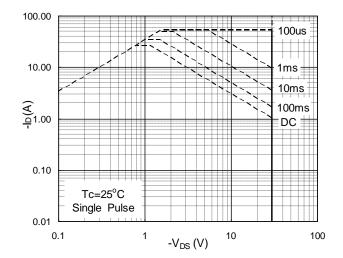


Fig.7 Capacitance

Fig.8 Safe Operating Area

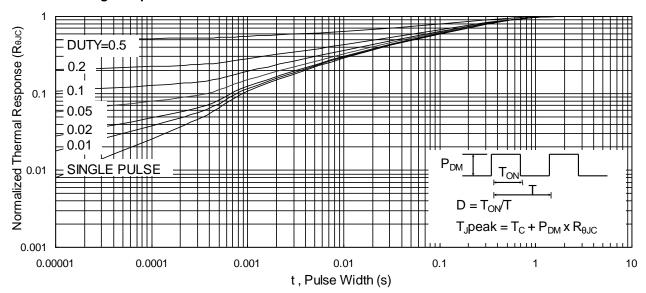


Fig.9 Normalized Maximum Transient Thermal Impedance

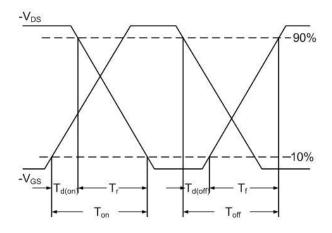


Fig.10 Switching Time Waveform

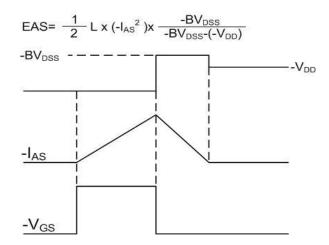


Fig.11 Unclamped Inductive Switching Waveform



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