HIGH SPEED 3.3 VOLT 2K x 8 CMOS PROM/RPROM

KEY FEATURES

- **3.3 Volt ± 0.3 Volt V_{CC}**
- **Fast Access Time**
  - — t_{ACC} = 70 ns
  - — t_{CS} = 20 ns
- **Low Power Consumption**
  - — ≤ 25 mA I_{CC}
- **Available in 300 Mil "Skinny" DIP**
- **Immune to Latch-up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**

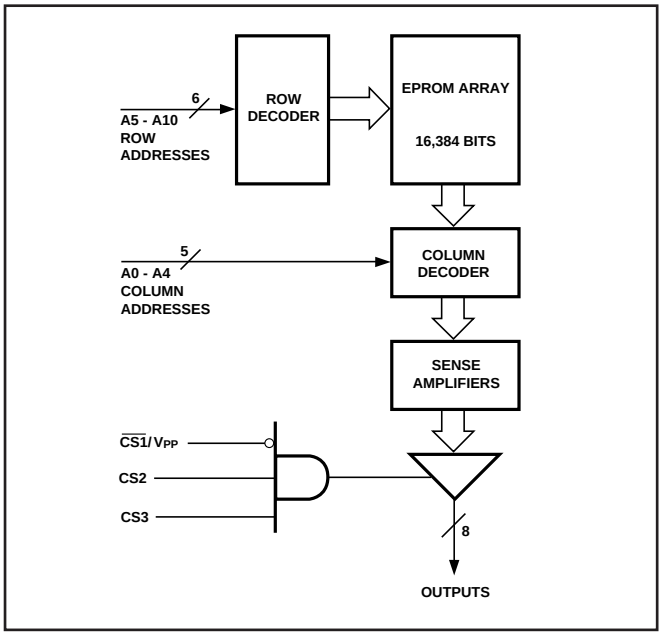
GENERAL DESCRIPTION

The WS57LV291C is a High Performance 2K x 8 UV Erasable Re-Programmable Read Only Memory (RPROM). This RPROM is manufactured using an advanced CMOS EPROM manufacturing process resulting in a very low power die that affords exceptional speed capabilities with a 3.3 volt V_{CC} supply. The WS57LV291C is configured in the standard Bipolar PROM pinouts, the preferred and most common pinout for high speed PROMs of 16K density.

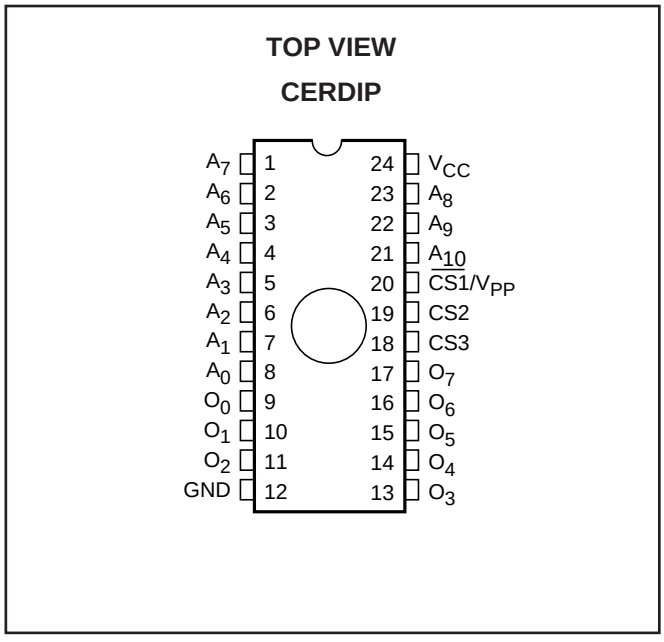
Operating at 3.3 volts, the WS57LV291C dissipates a maximum of 25 mA under worst case conditions at maximum speed (70 ns T_{AA}). Typical I_{CC} at 25°C is less than 20 milliamps.

The WS57LV291C is packaged in a space saving 300 mil windowed, hermetic DIP package.

BLOCK DIAGRAM



PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57LV291C-70	WS57LV291C-90
Address Access Time (Max)	70 ns	90 ns
CS to Output Valid Time (Max)	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....–65° to + 150°C

Voltage on any Pin with
Respect to Ground .....–0.6V to +7V

V_{PP} with Respect to Ground.....–0.6V to + 14V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

MODE SELECTION

PINS / MODE	$\overline{CS1}$/ V_{PP}	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+ 3.3V ± 0.3V

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 3)	–0.1	0.6	V
V_{IH}	Input High Voltage	(Note 3)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4		V
I_{CC}	V_{CC} Active Current (CMOS)	(Notes 1 and 2) I_{CC} at Maximum Frequency Outputs Not Loaded		25	mA
I_{LI}	Input Leakage Current	V_{IN} = 3.6V or Gnd	–10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.6 V or Gnd	–10	10	µA

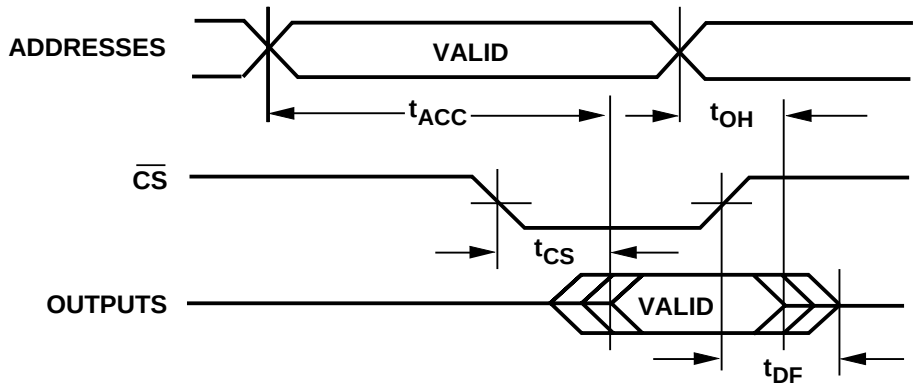
NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. For TTL inputs add 5 mA I_{CC}.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57LV291C-70		WS57LV291C-90		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		70		90	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		30	
Output Disable to Output Float*	t_{DF}		20		30	
Address to Output Hold	t_{OH}	0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

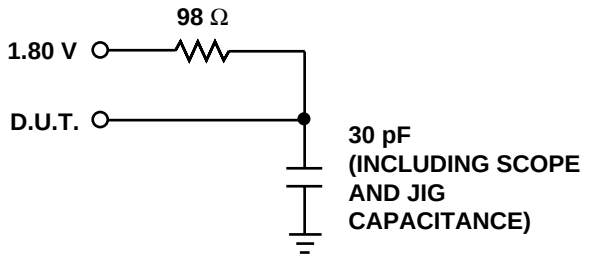


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

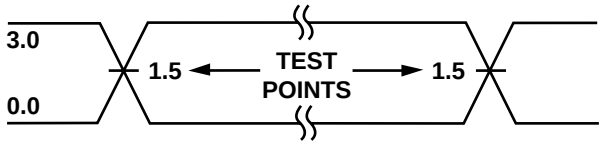
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



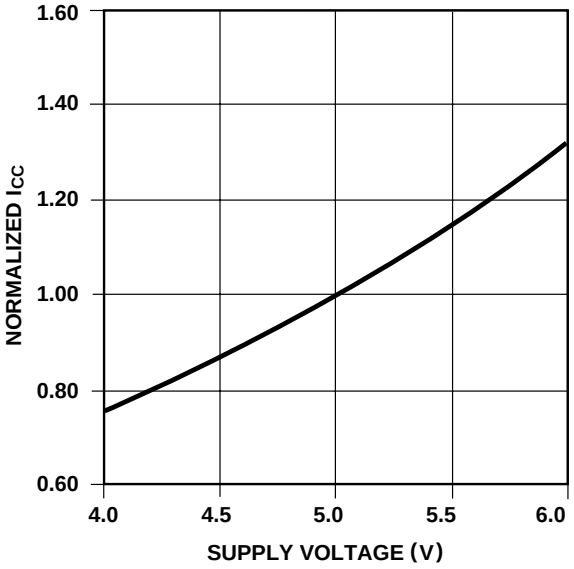
A.C. TESTING INPUT/OUTPUT WAVEFORM



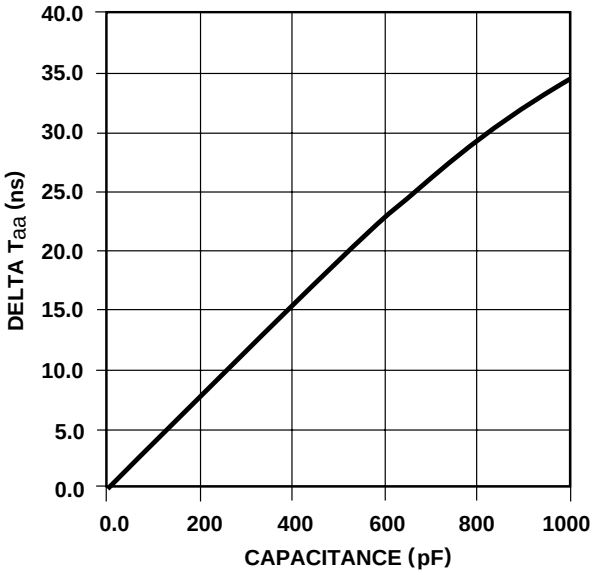
A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

NOTE: 6. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

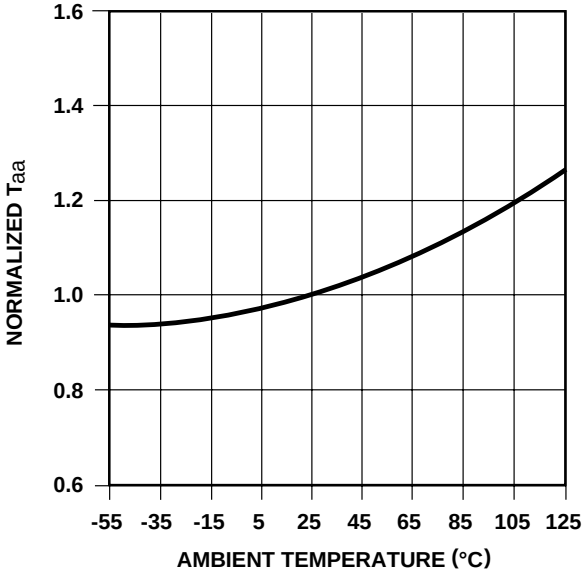
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



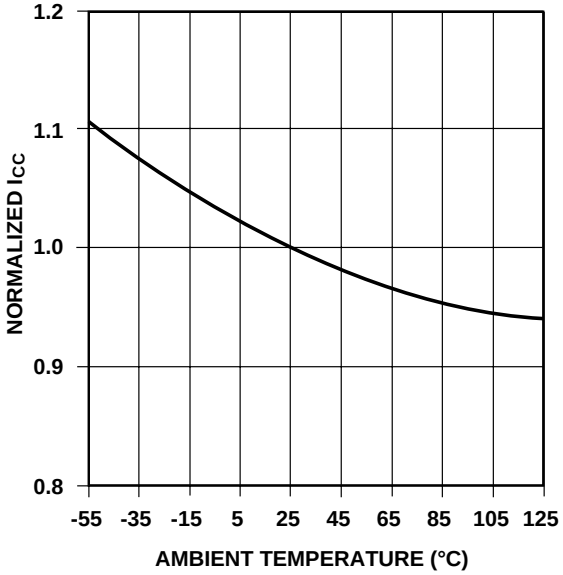
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED T_{aa} vs. AMBIENT TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

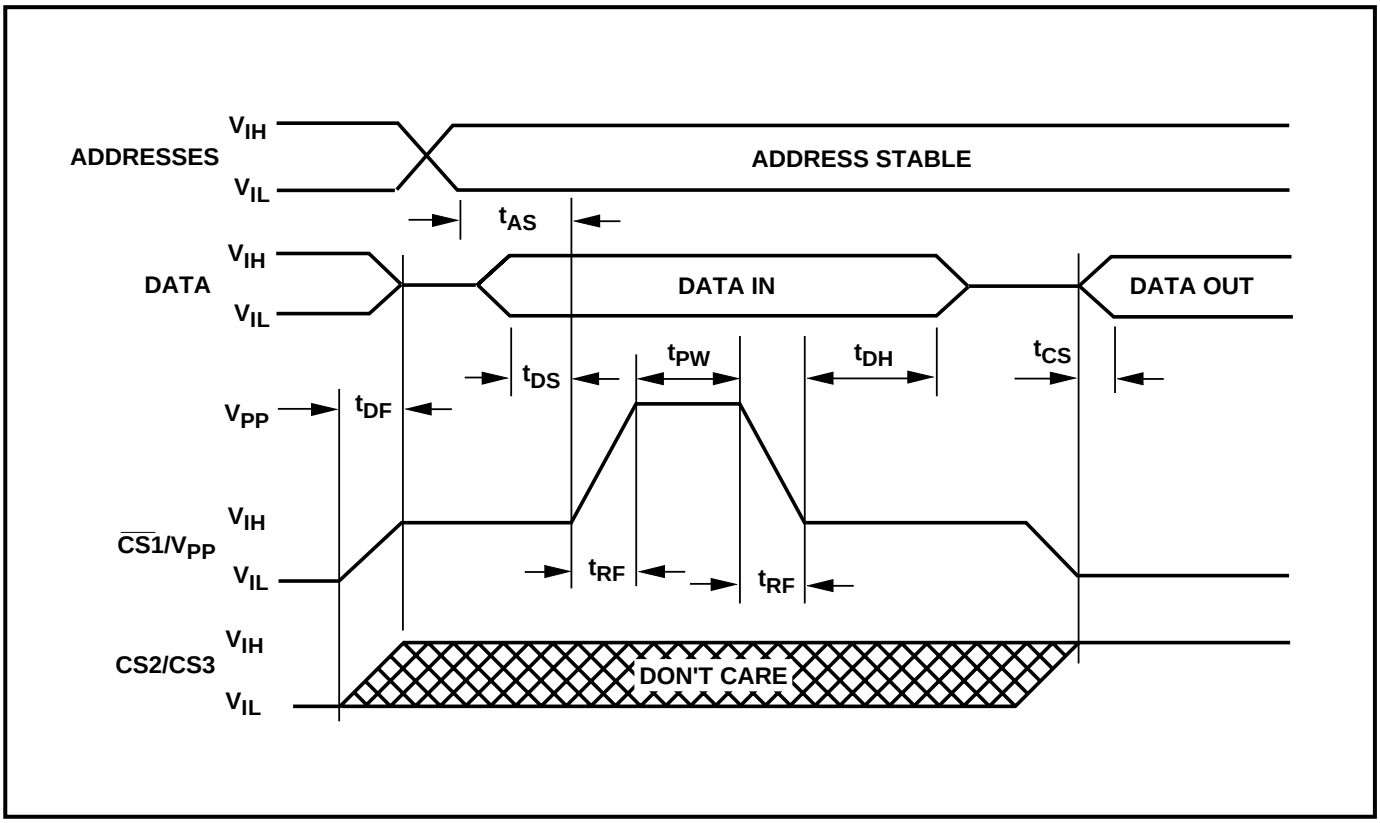
SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = –4 mA)	2.4		V

NOTES: 7. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	100		200	µs
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57LV291C-70T	70	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57LV291C-90T	90	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard

NOTE: 8. The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 5-1

The WS57LV291C is programmed using Algorithm D shown on page 5-9.