WM8200-10/12

40MSPS ADC with PGA

DESCRIPTION

The WM8200 is a CMOS high speed, low power, pipeline analogue-to-digital converter (ADC) with 10 or 12-bit output options. It also has an on-chip programmable gain amplifier (PGA), dc clamp circuit and internal voltage references. Conversion is controlled by a single clock input.

The device has a high bandwidth differential sample and hold input, which gives excellent common-mode noise immunity and low distortion. Alternatively, it can be driven in single ended fashion with an optional voltage clamp for dc restoration that can take its reference from an on-chip 10-bit DAC.

The WM8200 provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. However, it can also accept external references for applications where shared or high-precision references are required.

A 3-wire serial interface is used to control the device and a 10 or 12-bit parallel interface is to read ADC conversion data. ADC data can be output in unsigned binary or two's complement format.

The WM8200 operates with a single 3V supply and is supplied in a 28-lead QFN package.

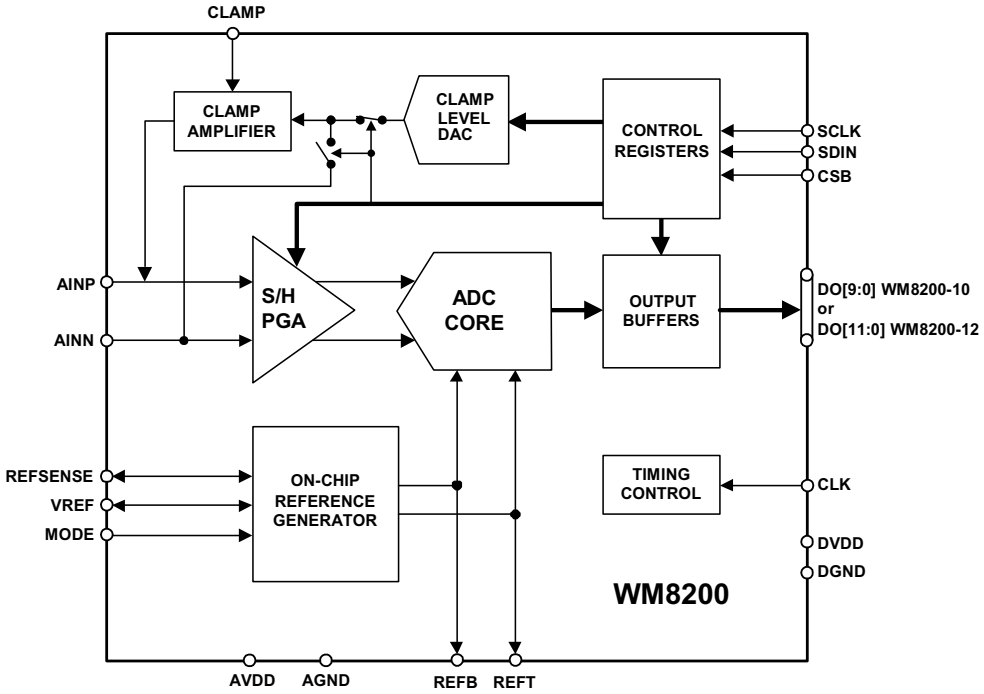
FEATURES

- 10 or 12-bit resolution ADC
- 40MSPS conversion rate
- Programmable Gain Amplifier (PGA)
- Adjustable internal voltage references
- Built in clamp function (dc restore) with 10-bit DAC
- Wide Input Bandwidth - 900MHz
- Unsigned Binary or Two's complement output format
- Programmable via 3-wire serial MPU interface
- Single 3V supply operation
- Low power - 100mW typical at 3.0V supplies
- Powerdown mode to <0.1mW typical
- 28 lead QFN package

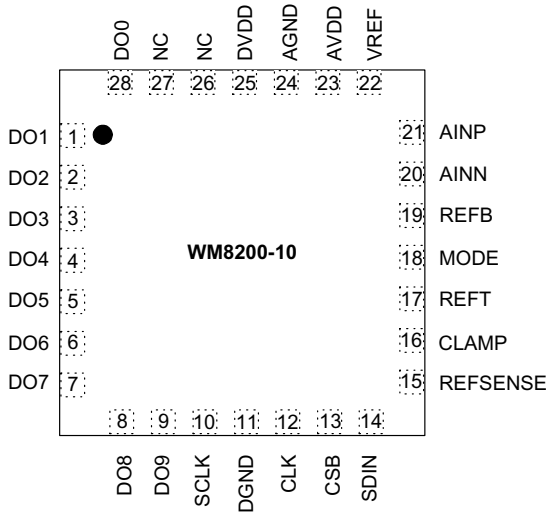
APPLICATIONS

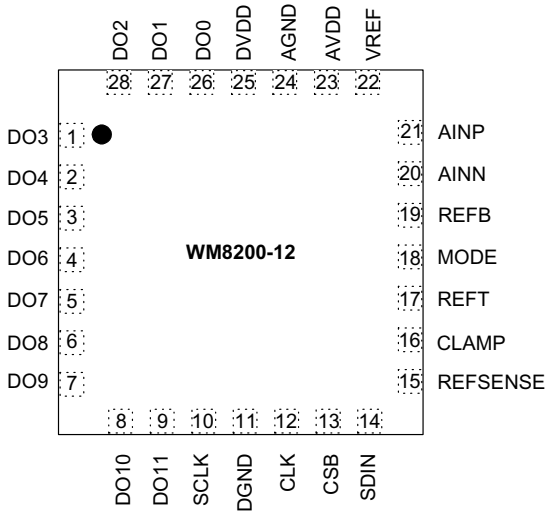
- Digital Still Cameras
- Composite Video Digitisation
- Digital Copiers
- Digital Video Cameras

BLOCK DIAGRAM



PIN CONFIGURATION





ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8200-10IFL	-40 to +85°C	28-lead QFN
WM8200-12IFL	-40 to +85°C	28-lead QFN

PIN DESCRIPTION

PIN	NAME		TYPE	DESCRIPTION
1	DO1	DO3	Digital Output	Digital output bit
2	DO2	DO4	Digital Output	Digital output bit
3	DO3	DO5	Digital Output	Digital output bit
4	DO4	DO6	Digital Output	Digital output bit
5	DO5	DO7	Digital Output	Digital output bit
6	DO6	DO8	Digital Output	Digital output bit
7	DO7	DO9	Digital Output	Digital output bit
8	DO8	DO10	Digital Output	Digital output bit
9	DO9	DO11	Digital Output	Digital output bit (MSB)
10	SCLK		Digital Input	3-Wire Control Interface Clock Input
11	DGND		Ground	Negative Digital Supply
12	CLK		Analogue Input	Clock input
13	CSB		Digital Input	3-Wire Control Interface Chip Select
14	SDIN		Digital Input	3-Wire Control Interface Data Input
15	REFSENSE		Analogue Input	VREF feedback/configuration control
16	CLAMP		Digital Input	High to enable clamp mode, low to disable clamp mode
17	REFT		Analogue Input/Output	Top ADC reference voltage
18	MODE		Analogue Input	High (MODE=AVDD) to enable internal ADC references. Low (MODE=AVSS) to enable use of external ADC references applied to REFT and REFB.
19	REFB		Analogue Input/Output	Bottom ADC reference voltage
20	AINN		Analogue Input	Positive analogue input
21	AINP		Analogue Input	Negative analogue Input
22	VREF		Analogue Input/Output	Internal/external reference voltage
23	AVDD		Supply	Positive Analogue Supply
24	AGND		Ground	Negative Analogue Supply
25	DVDD		Supply	Positive Digital Supply
26	NC	DO0	Digital Output	Not internally connected (10-bit option)/ Digital output bit (LSB for 12-bit option only)
27	NC	DO1	Digital Output	Not internally connected (10-bit option) / Digital output bit (for 12-bit Option Only)
28	DO0	DO2	Digital Output	Digital output bit (LSB for 10-bit Option)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DGND	-0.3V	+3.63V
Analog supply voltage, AVDD to AGND	-0.3V	+3.63V
Maximum voltage difference between AGND and DGND	-0.3V	+0.3V
Voltage range digital input (SCLK, SDIN, CSB, CLAMP)	DGND - 0.3V	DVDD + 0.3V
Voltage range analog inputs	AGND - 0.3V	AVDD + 0.3V
Voltage range CLK, MODE inputs	AGND - 0.3V	AVDD + 0.3V
Operating junction temperature range, T_J	-40°C	+150°C
Storage temperature	-65°C	+150°C
Package Body Temperature (soldering 10 seconds)		+240°C
Package Body Temperature (soldering 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Digital supply range	DVDD		3.0	3.3	3.6	V
Analog supply range	AVDD		3.0	3.3	3.6	V
Ground	DGND, AGND			0		V
Clock frequency	f_{CLK}		5		40	MHz
Clock duty cycle			45	50	55	%
Operating Free Air Temperature	T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 40MHz, 50% duty cycle, MODE = AVDD, VREF=1.0V (REFT = 2.0V, REFB = 1.0V),
PGA gain = 1.0, T_A = T_{MIN} to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
Integral nonlinearity	INL			±1.0		LSB
Differential nonlinearity	DNL			±0.3		LSB
Offset error				0.7		% of FSR
Full scale error				2.2		% of FSR
Missing codes			No missing codes guaranteed			
Analogue Input Signal to AIN pins						
Differential analogue input voltage (AINP-AINN)		PGA=1x gain	-1		1	V
Switched input capacitance				1.2		pF
Conversion Characteristics						
Conversion frequency	f_{CLK}		5		40	MHz
Pipeline delay				4		cycles of CLK
Dynamic Performance (differential input mode)						
Effective number of bits	ENOB	f_{IN} = 4.8MHz		9.6		bits
		f_{IN} = 20MHz		9.5		
Spurious free dynamic range	SFDR	f_{IN} = 4.8MHz		72		dB
		f_{IN} = 20MHz		70		
Total harmonic distortion	THD	f_{IN} = 4.8MHz		-72.5		dB
		f_{IN} = 20MHz		-71.6		
Signal to noise ratio	SNR	f_{IN} = 4.8MHz		60		dB
		f_{IN} = 20MHz		57		
Signal to noise and distortion ratio	SINAD	f_{IN} = 4.8MHz		59.7		dB
		f_{IN} = 20MHz		59.6		
PGA						
Gain range (linear scale)			0.5		4	V/V
Gain step size (linear scale)				0.5		V/V
Clamp						
Clamp DAC resolution				10		bits
Clamp DAC output voltage			REFB		REFT	V
Clamp DAC DNL				±1		LSB
Clamp output voltage error			-40		40	mV
REFB, REFT internal ADC reference voltage outputs (MODE= AVDD)						
Reference voltage top, REFT (AVDD=3V)		VREF = 0.5V		1.75		
		VREF= 1.0V		2		
Reference voltage bottom, REFB (AVDD=3V)		VREF = 0.5V		1.25		
		VREF= 1.0V		1		
VREF Input / Output specifications (ADC Input Range = VREFx2)						
Internal 0.5V reference to VREF		REFSENSE = VREF		0.5		V
Internal 1V reference to VREF		REFSENSE = AGND		1		V
External reference applied to VREF pin		REFSENSE = AVDD	0.5		1	V
Input impedance in internal ADC reference mode		REFSENSE = AVDD, MODE = AVDD		14		kΩ

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 40MHz, 50% duty cycle, MODE = AVDD, VREF=1.0V (REFT = 2.0V, REFB = 1.0V), PGA gain = 1.0, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
Analogue supply current	I_{AVDD}	MODE = AGND		28.5		mA
		MODE = AVDD		31		mA
Digital supply current	I_{DVDD}	C_L = 10pF		5		mA
Standby power consumption (digital and analogue combined)	I_{VDD}(STBY)			75		uW
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}	(Note 1)			0.2 x VDD	V
Input HIGH level	V_{IH}	(Note 1)	0.8 x VDD			V
Output LOW	V_{OL}	I_{OL} = -50µA			0.4	V
Output HIGH	V_{OH}	I_{OH} = 50µA	VDD – 0.4			V

Notes

1. Digital input and output levels refer to the supply used for the input/output buffer on the relevant pin. CLK and MODE refer to the AVDD supply, all other digital input/output refers to the DVDD supply.

CONTROL INTERFACE TIMING

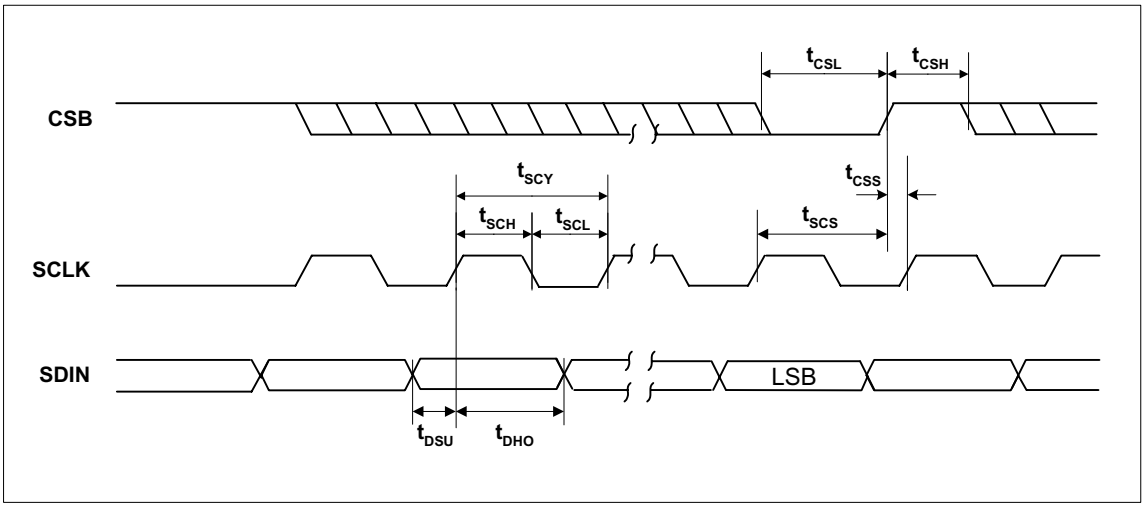


Figure 1: Control Interface Timing

Test Conditions
AVDD = DVDD = 3.0V, AGND = DGND = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		30			ns
SCLK pulse width high	t_{SCH}		30			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

Table 1 Control Interface Timing Information

DEVICE DESCRIPTION

INTRODUCTION

The WM8200 is a high speed analogue to digital converter (ADC) with on-chip analogue pre-processing and reference generation, deisgned for applications such as composite video digitisation digital copiers and high speed data acquisition. The integrated clamp and the coarse offset function mean the device is ideally suited to CCD/CMOS input systems such as colour scanners, digital copiers and digital cameras. A wide input voltage range between REFB and REFT allows the WM8200 to be used in both imaging and communications systems.The chip architecture consists of:

- High bandwidth sample and hold input, which can operate in differential or single-ended mode
- Programmable gain amplifier (PGA)
- Voltage clamp for DC restoration that can take its reference from an on-chip 10-bit DAC or an external source
- Coarse offset function to allow clamping with single ended CCD style inputs
- 10-bit, 40MSPS pipeline analogue-to-digital converter (ADC) core
- On-chip reference generator and reference buffer (external references can also be used for applications where common or high precision references are required)
- 10-bit parallel output for ADC conversion. ADC data can be output in unsigned binary or two's complement format. An out-of-range output pin indicates when the input signal is outside the converter's range
- Serial control interface to configure the operation of the device.

ANALOGUE SIGNAL PATH

The WM8200 analogue signal path consists of a DC clamp with a 10-bit clamp level DAC (discussed under 'DC Clamp', below), a high-bandwidth sample and hold unit followed by a programmable gain amplifier (PGA) and a fast 10-bit pipelined analogue to digital converter (ADC core).

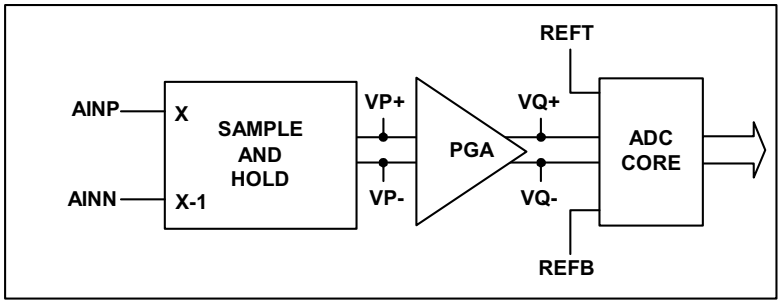


Figure 2 Analogue Input Signal Flow

Figure 2 shows the signal flow through the sample and hold unit and the PGA to the ADC core, where the process of analogue to digital conversion is performed against the ADC reference voltages, REFT and REFB (their generation from internal or external reference sources is described later).

SAMPLE AND HOLD

The differential analogue input signals can be connected directly to the AINN and AINP pins, either DC coupled, AC coupled, or AC coupled with DC restoration using the WM8200 clamp circuit.

The differential sample and hold processes V_{INP} and V_{INN} with respect to the voltages applied to the REFT and REFB pins, and produces a differential output $V_P = V_{P+} - V_{P-}$ given by:

$$V_P = AINP - AINN$$

For single-ended input signals, the signal can be DC or AC coupled to either AINN or AINNP, and a suitable reference voltage must be applied to the other pin. Note of the input signal is applied to AINN this will result in it being inverted during sampling.

PROGRAMMABLE-GAIN AMPLIFIER

V_P is amplified by the PGA and fed into the ADC as a differential voltage $V_Q = V_{Q+} - V_{Q-}$

$$V_Q = Gain \times V_P = Gain \times (V_{INP} - V_{INN})$$

The PGA gain defaults to 1.0 at power-up, but can be programmed from 0.5 to 4.0 in steps of 0.5.

ANALOGUE-TO-DIGITAL CONVERTER

Regardless of the reference configuration, V_Q is digitised against ADC Reference voltages REFT and REFB, full scale values of V_Q being given by:

$$V_{QFS} = \frac{REFT - REFB}{2} \qquad \text{and zero scale by} \quad V_{QZS} = -\left(\frac{REFT - REFB}{2}\right)$$

Attempts to convert V_Q voltages outside the range of V_{QZS} to V_{QFS} are signalled to the application by driving the OVR output pin high when the conversion result is output. If V_Q is less than V_{QZS}, the ADC output code is 0. If V_Q is greater than V_{QFS}, the output code is 1023.

SIGNAL CHAIN SUMMARY

Combining the above equations to find the input voltages [AINP – AINN] that correspond to the limits of the ADCs valid input range gives:

$$\frac{(REFB - REFT)}{(2 \times Gain)} \leq [AINP - AINN] \leq \frac{(REFT - REFB)}{(2 \times Gain)}$$

Therefore the input signal span is given by:

$$AINP - AINN = \frac{REFT - REFB}{Gain}$$

In order to match the ADC input range to the input signal amplitude, REFT and REFB should be set such that:

$$REFT - REFB = (AINP - AINN) \times Gain$$

ADC REFERENCE MODES

The WM8200 references REFT and REFB can be driven from external (off-chip) sources or from the internal reference generation/buffer circuit. The mode of operation is selected by the voltage applied to the MODE pin. These are summarised and explained in Table 2.

Note that the internally generated ADC references are intended solely for WM8200 internal use and REFT and REFB must not be used as voltage references for any other device in the application.

MODE PIN	MODE	FUNCTION	COMMENTS
AGND	Full external	$REFT = external$ $REFB = external$	On-chip reference generator and reference buffer are not used.
AVDD	Top/Bottom	$REFTF = \frac{AVDD + (REFTS - REFBS)}{2}$ $REFBF = \frac{AVDD - (REFTS - REFBS)}{2}$	On-chip reference generator is not used. Reference buffer centers external reference voltages around AVDD/2.

Table 2 WM8200 Reference Generation Modes

DC CLAMP

The WM8200 incorporates a clamp function for restoring the DC reference level of AC coupled input signals. When the clamp input pin is held high the internal clamp amplifier forces the voltage at AINP to equal the clamp reference voltage, setting the DC level at AINP.

The clamp reference voltage comes from the on-chip 10-bit Clamp Level DAC by default, however it can be applied to the AINN pin if the CLPSEL register bit is set high.

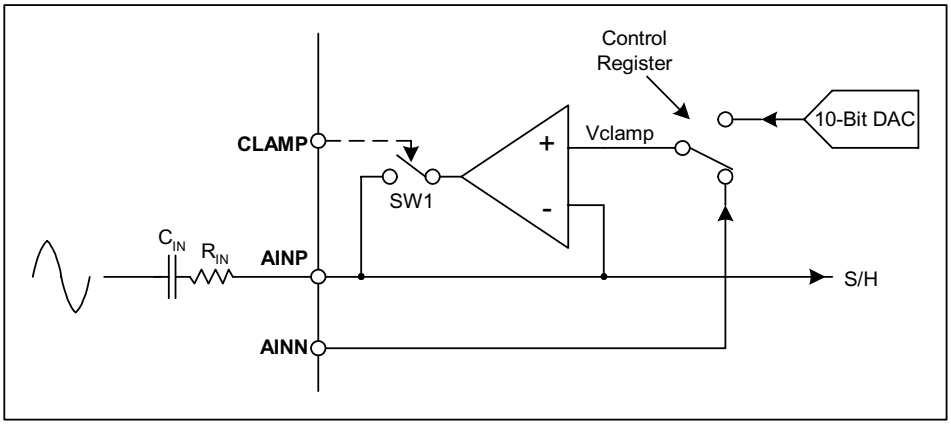


Figure 3 Schematic of Clamp Circuitry

Figure 4 shows an example of using the clamp to restore the black level of a composite video input AC coupled to AINN. While the clamp pin is held high, the clamp amplifier forces the voltage at AINN to equal the clamp reference voltage, setting the DC voltage at AINN for the video black level.

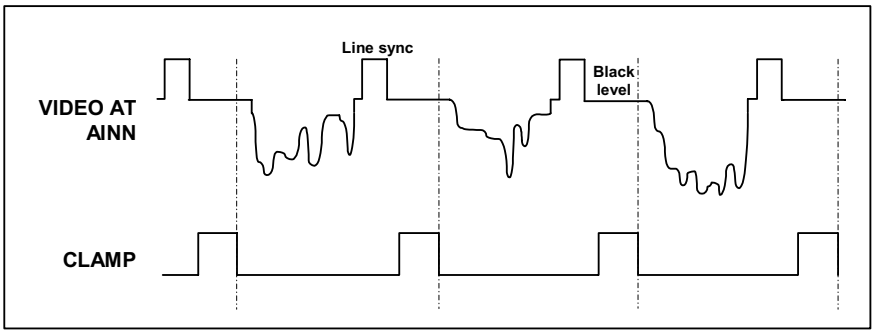


Figure 4 Example Waveforms for Line-Clamping to a Video Input Black Level

If the CLAMP amplifier is not required it can be disabled for power saving purposes by setting the CLPDIS register bit to high.

CLAMP DAC OUTPUT VOLTAGE RANGE AND LIMITS

Important: When using the internal clamp DAC in Top/Bottom or Centre Span Mode, the user must ensure that the desired DC clamp level at AIN lies within the voltage range REFB to REFT. This is because the clamp DAC voltage is constrained to lie within this range REFB to REFT. Specifically:

V_{DAC} = REFB + (REFT – REFB) x (0.006 +0.988 x (DAC_code)/1024)

DAC codes can range from 0 to 1023. Figure 5 shows the clamp DAC output voltage versus the DAC code.

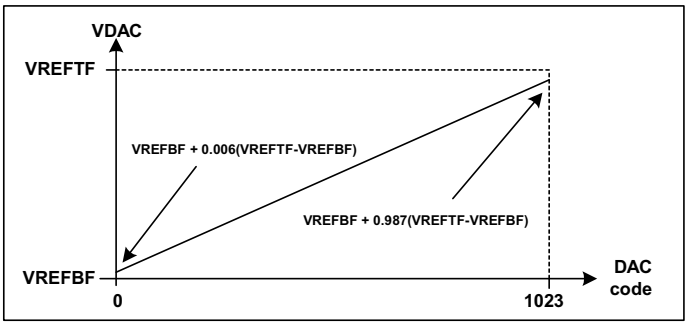


Figure 5 Clamp DAC Output Voltage versus DAC Register Code Value

COARSE OFFSET

The WM8200 features a coarse offset feature which allows it to accommodate both positive-going and negative-going input signals when using the DC clamp. This feature is enabled by setting the PGAOFF register bit to high.

DIAGRAM SHOWING COARSE OFFSET TO BE INSERTED

CONTROL INTERFACE

The internal control registers are programmable via the 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the data and CSB is used to latch in the program data. The 3-wire interface protocol is shown in Figure 6.

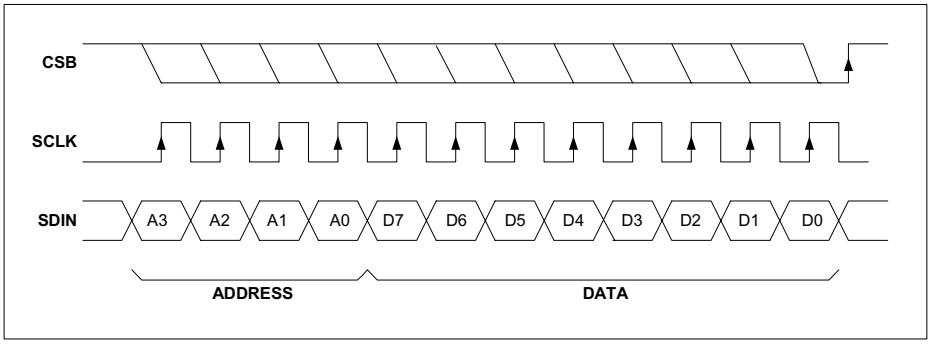


Figure 6: 3-Wire Serial Interface

1. A[3:0] are Control Address Bits
2. D[7:0] are Control Data Bits
3. CSB is edge sensitive – the data is latched on the rising edge of CSB.

REGISTER MAP

Table 3 shows the location of each control bit used to determine the operation of the WM8200. The procedure for programming the register map is described in the CONTROL INTERFACE section.

ADDR	NAME	DEFAULT (HEX)	BIT							
			B7	B6	B5	B4	B3	B2	B1	B0
0000	Clamp Reg 1	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
0001	Clamp Reg 2	00	0	0	0	0	0	0	DAC[9]	DAC[8]
0010	PGA Control	01	0	0	PGASENSE	PGAOFF	0	PGA[2]	PGA[1]	PGA[0]
0011	Control	00	0	0	0	CLPSEL	OEB	TWOSC	CLDIS	PD
0100 - 1111	Reserved	00	Reserved, do not write to these register locations							

Table 3: Register Map

REGISTER MAP DESCRIPTION

REGISTER	BIT	BIT NAMES	DEFAULT	DESCRIPTION
Clamp Register 1	7:0	DAC[7:0]	00000000	Clamp DAC value bits 7 to 0 (Unsigned binary format)
Clamp Register 2	1:0	DAC[9:8]	00	Clamp DAC value bits 9 to 8 (Unsigned binary format)
PGA Control Register	2:0	PGA[2:0]	001	PGA Gain control 000: PGA Gain = 0.5x / 100: PGA Gain = 2.5x 001: PGA Gain = 1.0x / 101: PGA Gain = 3.0x 010: PGA Gain = 1.5x / 110: PGA Gain = 3.5x 011: PGA Gain = 2.0x / 111: PGA Gain = 4.0x
	4	PGAOFF	0	Enables a coarse offset to be added to the output of the PGA. Allows the use of single ended input signals with no loss of ADC dynamic range.
	5	PGASENSE	0	Determines the sense of the coarse offset added to the output of the PGA. This bit only has an effect when PGAOFF=1. 0: PGA output is offset to full-scale positive for zero differential input (suitable for negative going video). 1: PGA output is offset to full-scale negative for zero differential input (suitable for positive going video).
Control Register	0	PD	0	Device power-down 0: Device is powered up 1: Device is powered down.
	1	CLDIS	0	CLAMP amplifier enable (for power saving) 0: Enable 1: Disable
	2	TWOSC	0	Output data format 0: Unsigned binary 1: Twos complement
	3	OEB	0	Output data pin enable 0: DO[9:0]/DO[11:0] enabled 1: DO[9:0]/DO[11:0] disabled (outputs are high impedance).
	4	CLPSEL	0	Clamp source select 0: Clamp to output of Clamp DAC 1: Clamp to voltage on AINN input pin

POWER MANAGEMENT

In power-sensitive applications (such as battery-powered systems) where the WM8200 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the WM8200 into Power Down mode. This is achieved by setting bit 0 (PD) of the control register to 1. In Power Down mode, the device typically consumes less than 3mW of power. Power down mode is exited by resetting control register bit 1 to 0. On power up from long periods of power down, the WM8200 typically requires 5ms of wake up time before valid conversion results are available.

In systems where the ADC must run continuously, but where the clamp is not required, the supply current can be reduced by approximately 1.2mA by setting the control register bit 1 (CLDIS), which disables the clamp circuit. Similarly, when REFSENSE is tied to AVDD, the reference generator is disabled and supply current reduced by approximately 1.2mA.

DATA OUTPUT FORMAT

While the OEB pin is held low, ADC conversion results are output at the data I/O pins DO[0] (LSB) to DO[9] (MSB). The default output data format is unsigned binary (output codes 0 to 1023). This can be switched to two's complement format (output codes -512 to 511) by setting control register bit 2 (TWOSC) to 1.

REFERENCE VOLTAGE GENERATION

The WM8200 incorporates an on-chip 0.5V bandgap voltage reference that can be used to derive a temperature and supply independent voltage on pin VREF. The VREF output can be used for driving external loads or setting the ADC input range. The voltage is programmed via connections made to the REFSENSE pin as shown in Table 4.

REFSENSE	VREF output	Refer to
AGND	1.0V	Figure 7
AVDD	Hi impedance – A1 amplifier disabled If using the ADC reference generator then an external VREF source must be applied to the VREF pin.	Figure 8
Connect to VREF	0.5V	Figure 9
R network to VREF / AGND	Between 0.5 V and 1 V VREF=0.5x(1+Ra/Rb)	Figure 10

Table 4: – VREF output control by REFSENSE connection

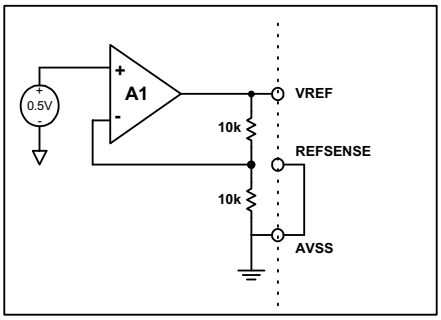


Figure 7: VREF=1V

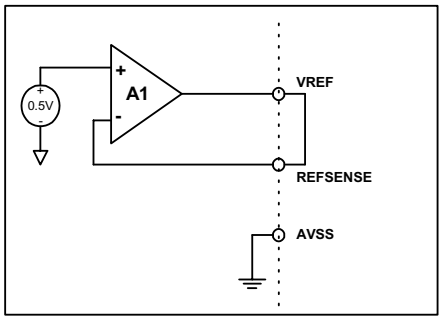


Figure 9: VREF=0.5V

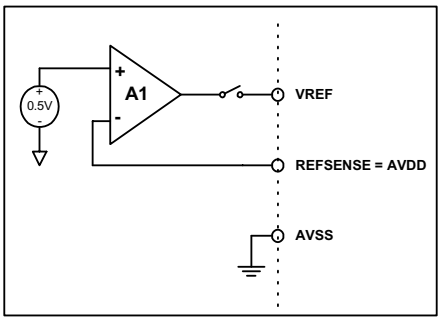


Figure 8: VREF=Hi Impedance

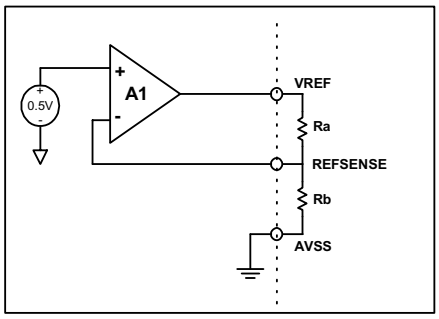


Figure 10: VREF between 0.5 and 1V

When enabled, the on-chip voltage reference should be externally decoupled (see Reference Decoupling Section for details).

In internal ADC references mode (MODE=AVDD), the voltages at REFT and REFB are:

REFT = (AVDD + VREF) / 2

REFB = (AVDD – VREF) / 2

If external ADC references mode (MODE=AVSS), the average value of the external voltages applied to REFT and REFB should be AVDD/2 for correct device operation.

REFERENCE DECOUPLING

VREF, REFT and REFB must be decoupled as shown in Figure 11.

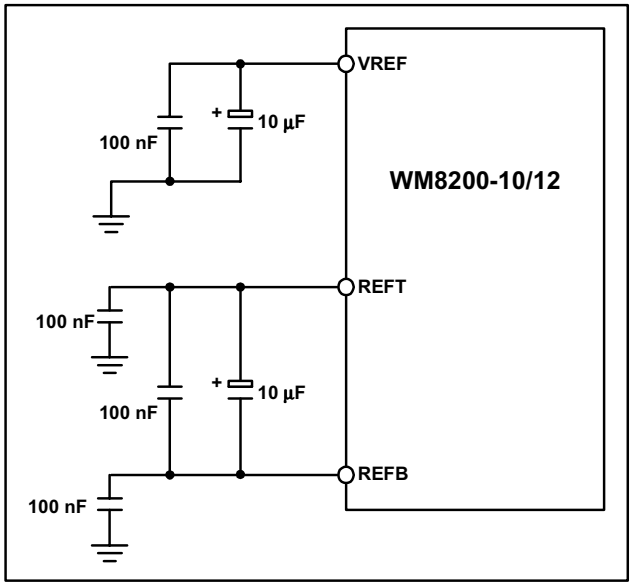
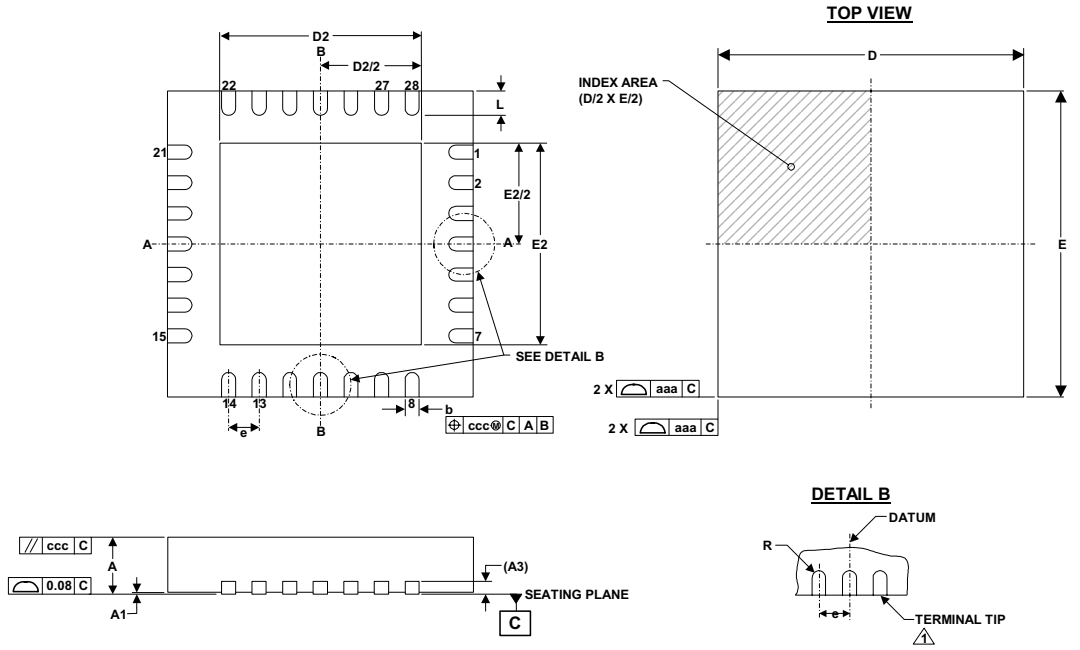


Figure 11: VREF, REFT and REFB decoupling

PACKAGE DIMENSIONS

FL: 28 PIN QFN PLASTIC PACKAGE 5 X 5 X 0.9 mm BODY, 0.50 mm LEAD PITCH **DM023.C**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		2
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
R	b(min)/2			
Tolerances of Form and Position				
aaa		0.15		
ccc		0.10		
REF:	JEDEC.95, MO-220, VARIATION VHHD-1			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC.95, MO-220 WITH THE EXCEPTION OF D2, E2, A3:
   D2,E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
   A3: NOMINAL VALUE LESS THAN JEDEC
3. ALL DIMENSIONS ARE IN MILLIMETRES
4. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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