WM-BAC-CYW-50
WiFi-BT IoT SiP Module
Datasheet

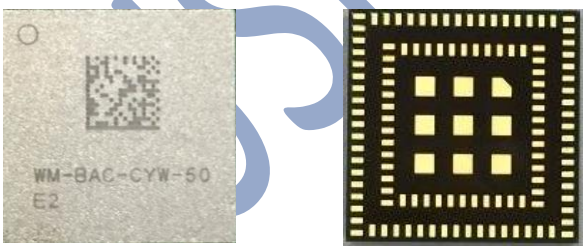
Introduction

The WM-BAC-CYW-50 WiFi-BT SiP module which refers as “module” is a small size module and consists of PSoC6 and CYW43012, authorization chips from Cypress. The WM-BAC-CYW-50 provides the highest-level integration for electronic accessories, featuring integrated full function of IEEE 802.11a/b/g/n, 11ac friendliness and Bluetooth 5.0 in a tiny module via 129 pins LGA Footprint.

The small size & low-profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11a/ac/b/g/n single-band Wi-Fi + Bluetooth features.

For the software and driver development, USI provides extensive technical document and reference software code for the system integration under the agreement of Cypress International Ltd.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.



Features

CYW43012 Wi-Fi/BT

- Full IEEE 802.11a/b/g/n compatibility
- Provide 802.11ac friendliness by supporting 256-QAM for 20 MHz channels.
- Complies with Bluetooth Core Specification version 5.0 with LE 2 Mbps
- Low power operation supporting sleep and standby modes

PSoC6 Microprocessor

- ARM 32-bit Cortex-M4F CPU, frequency up to 150MHz
- 100Mhz Cortex-M0+ CPU
- Embedded 288KB SRAM
- Embedded 1MB+32KB FLASH
- Embedded 128KB ROM
- Up to 38 GPIO interfaces multiplexed with other interfaces

WM-BAC-CYW-50 Module

- Featuring integrated IEEE 802.11 a/b/g/n, 11ac friendliness and BT5.0
- Low power consumption & excellent power management performance extend battery life.
- Small size suitable for low volume system integration.
- Easy for integration into mobile and handheld device with flexible system configuration.
- Lead Free design which supporting Green design requirement, RoHS Compliance.

Module Dimension

- 10.9 x 10.9 x 1.1 (Max.) mm

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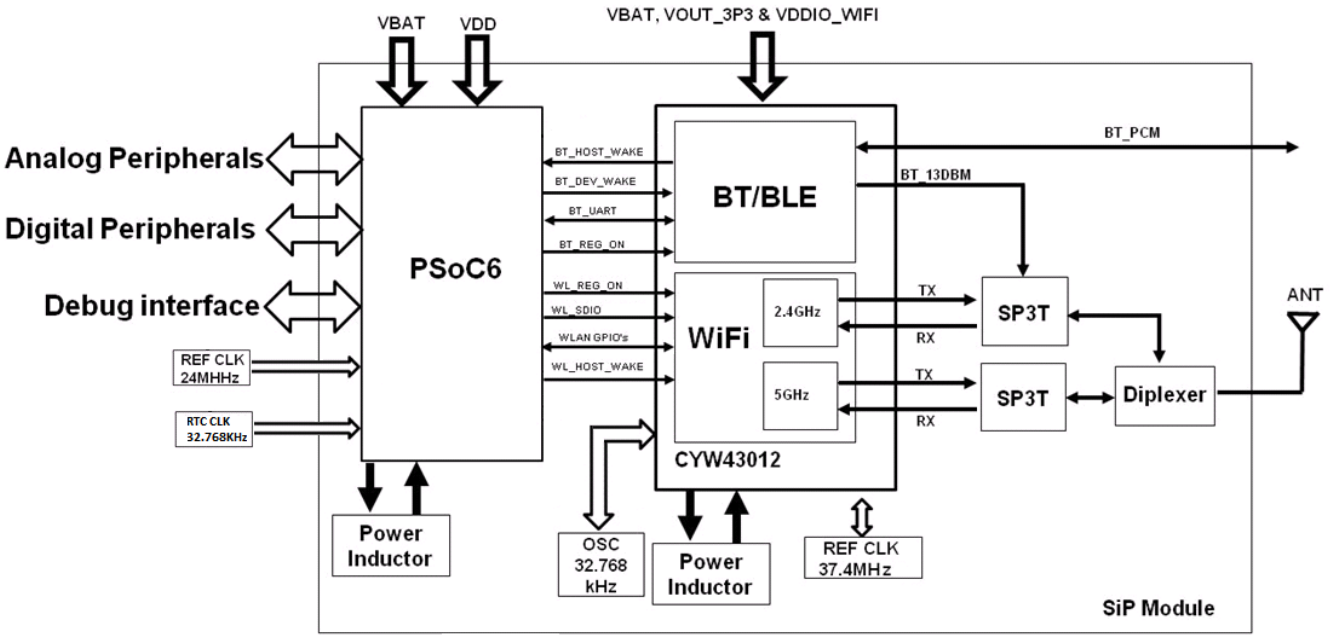
1 BLOCK DIAGRAM

The WM-BAC-CYW-50 MCU host module is designed based on PSoC6+CYW43012 solution. It supports generic UART interface to connect the WLAN and BT to the host processor. A simplified block diagram of the WM-BAC-CYW-50 module is depicted in the Fig. below.



2 TECHNICAL SPECIFICATION

2.1 ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Min	Max	Unit
VBAT	DC supply voltage for VBAT		-0.5	4.8	V
VDDD, VBACKUP, VDD_NS, VDDUSB	DC supply voltage		-0.5	3.6	V
VDDA, VDDIO0, VDDIO1, VDDIO			-0.5	2.2	V
Ts	Storage temperature		-40	85	℃

2.2 RECOMMENDABLE OPERATION CONDITION

2.2.1 TEMPERATURE, HUMIDITY

The WM-BAC-CYW-50 module has to withstand the operational requirements as listed in the table below.

Operating Temperature	-20° to 60° Celsius	
Relative Humidity range	Max 85%	Non condensing , relative humidity

2.2.2 VOLTAGE

Symbol	Parameter	Min	Typ.	Max	Unit	
VBAT	DC supply voltage for 43012_VBAT	3.2	3.6	4.2	V	
VDDIO	VDDIO for 43012	1.7	1.8	1.98	V	
VDDD	Internal regulator and Port 1 GPIO supply	1.7	-	3.6	V	
VDDA	Analog power supply voltage.	1.7	1.8	1.98	V	
VDDIO1	GPIO Supply for Ports 5 to 8	1.7	1.8	1.98	V	VDDIO1 must be ≥ VDDA.
VDDIO0	GPIO Supply for Ports 11 to 13	1.7	1.8	1.98	V	
VDD_NS	Supply input to the Buck	1.7	-	3.6	V	
VBACKUP	Backup Power and GPIO Port 0 supply	1.7	-	3.6	V	Min. is 1.4 V in Backup Mode
VDDUSB	Supply for Port 14 (USB or GPIO)	1.7	3.3	3.6	V	Min supply is 2.85 V for USB

2.3 WIFI PERFORMANCE SPECIFICATIONS

The WM-BAC-CYW-50 module complies with the following features and standards.

Features	Description	
WLAN Standards	IEEE 802 11 a//b/g/n, 802.11ac friendly	
Frequency Band	2.400 GHz – 2.484 GHz 4.900 GHz – 5.845 GHz -	
Number of Sub Channels	CH1 to CH14 CH36 to CH165	
Modulation	DSSS,CCK,OFDM,BPSK,QPSK,16QAM,64QAM,256QAM	
Supported data rates	11b	1, 2, 5.5, 11 (Mbps)
	11a/g	6, 9, 12, 18, 24, 36, 48, 54 (Mbps)
	11n	HT20 MCS0 (6.5Mbps) to MCS7 (65Mbps)
	11ac	HT20 MCS8 (78Mbps)

2.3.1 SPECIFICATIONS OF WIFI'S OUTPUT POWER、 EVM 、SENSITIVITY

The WM-BAC-CYW-50 module WiFi TX power as list in the table below:
(Typical values are at VBAT = 3.6V , VDDIO = 1.8V , VDD = 3.3V and TA = +25C)

Characteristics		TYP.	Tol.	Unit
RF Average Output Power 802.11b CCK Mode	1 Mbps	17	+/- 2	dBm
	11 Mbps	17	+/- 2	dBm
RF Average Output Power 802.11a/g OFDM Mode	6 Mbps	17	+/- 2	dBm
	54 Mbps	15	+/- 2	dBm
RF Average Output Power 802.11n OFDM Mode	MCS0	17	+/- 2	dBm
	MCS7	15	+/- 2	dBm
RF Average Output Power 802.11ac OFDM Mode	MCS8	13	+/- 2	dBm

** Note: The Output Power Level will be updated after samples reliability test

WiFi TX EVM follow the IEEE spec that as list in the table below:
(Typical values are at VBAT = +3.6V , VDDIO = 1.8V , VDD = 3.3V and TA = +25C)

Characteristics		TYP.	IEEE Spec	Unit
RF Average Output EVM (11b)	@1 Mbps	-12	-9.12*	dB
	@11 Mbps	-12	-9.12*	dB
RF Average Output EVM (11a/g)	@6 Mbps	-8	-5*	dB
	@54 Mbps	-28	-25*	dB
RF Average Output EVM (11n)	@ MCS0	-8	-5*	dB
	@ MCS7	-30	-27*	dB
RF Average Output EVM (11ac)	@ MCS8	-32	-30*	dB

The WM-BAC-CYW-50 module WiFi sensitivity as list in the table below:
(Typical values are at VBAT = +3.6V , VDDIO = 1.8V , VDD = 3.3V and TA = +25C)

Receiver Characteristics	TYP.	MAX.	Unit
PER <8%, Rx Sensitivity @ 1 Mbps	-95	-82*	dBm
PER <8%, Rx Sensitivity @ 11 Mbps	-87	-76*	dBm
PER <10%, Rx Sensitivity @ 6 Mbps	-91	-82*	dBm
PER <10%, Rx Sensitivity @ 54 Mbps	-74	-65*	dBm
PER <10%, Rx Sensitivity @ MCS0(HT20)	-91	-82*	dBm
PER <10%, Rx Sensitivity @ MCS7(HT20)	-73	-64*	dBm
PER <10%, Rx Sensitivity @ 11a 6 Mbps	-90	-82*	dBm
PER <10%, Rx Sensitivity @ 11a 54 Mbps	-73	-65*	dBm
PER <10%, Rx Sensitivity @11an MCS0(HT20)	-91	-82*	dBm
PER <10%, Rx Sensitivity @ 11an MCS7(HT20)	-73	-64*	dBm
PER <10%, Rx Sensitivity @ 11ac MCS8(HT20)	-70	-64*	dBm

*Refer to IEEE802.11 specification.

2.4 BLUETOOTH PERFORMANCE SPECIFICATIONS

The Radio specification is compliant with the Bluetooth ™ 5.0 specification

Features	Description
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels
Modulation	FHSS (Frequency Hopping Spread Spectrum) , GFSK, DPSK

(Typical values are at VBAT = 3.6V , VDDIO = 1.8V , VDD = 3.3V and TA = +25C)

2.4.1 SPECIFICATIONS OF BLUETOOTH 'S OUTPUT POWER、SENSITIVITY

The WM-BAC-CYW-50 module BT TX power as list in the table below:

(Typical values are at VBAT = 3.6V , VDDIO = 1.8V , VDD = 3.3V and TA = +25C)

Characteristics	Data Rate	TYP.	Tol.	Unit
BT Output Power	1 Mbps	11	+/- 3	dBm
	2 Mbps	9	+/- 3	dBm
	3 Mbps	9	+/- 3	dBm
	LE	11	+/- 3	dBm

**The Performance will be updated after samples reliability test

The WM-BAC-CYW-50 module BT RX sensitivity as list in the table below:

(Typical values are at VBAT = 3.6V , BT_VBAT = 3.3V , VDDIO = 1.8V , VDD_FEM = 3.3V and TA = +25C)

Characteristics	Data Rate	TYP.	Max.	Unit
BT RX Sensitivity	1 Mbps	-90	-70*	dBm
	2 Mbps	-92	-70*	dBm
	3 Mbps	-85	-70*	dBm
	LE	-92	-70*	dBm

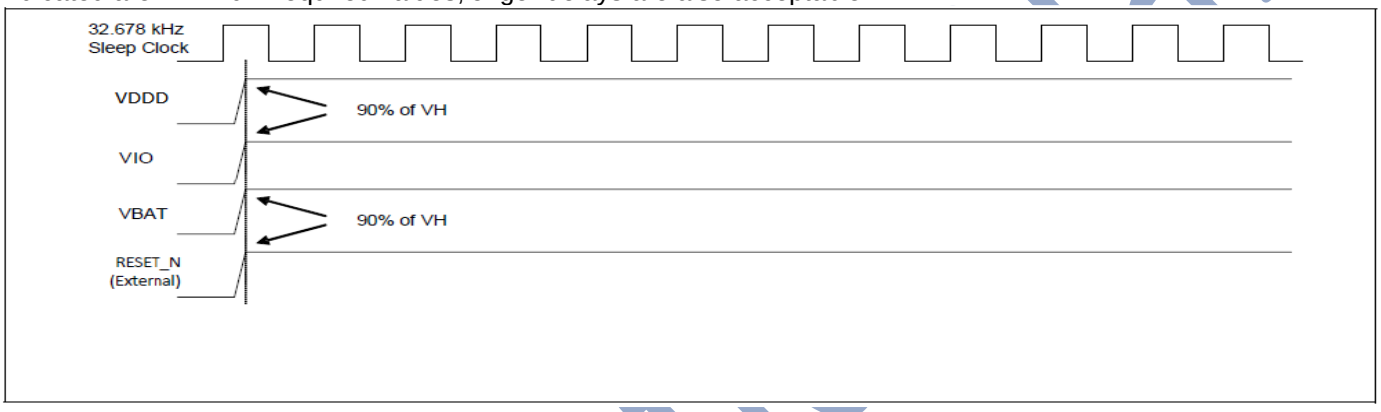
*Refer to Bluetooth specification.

**The Performance will be updated after samples reliability test

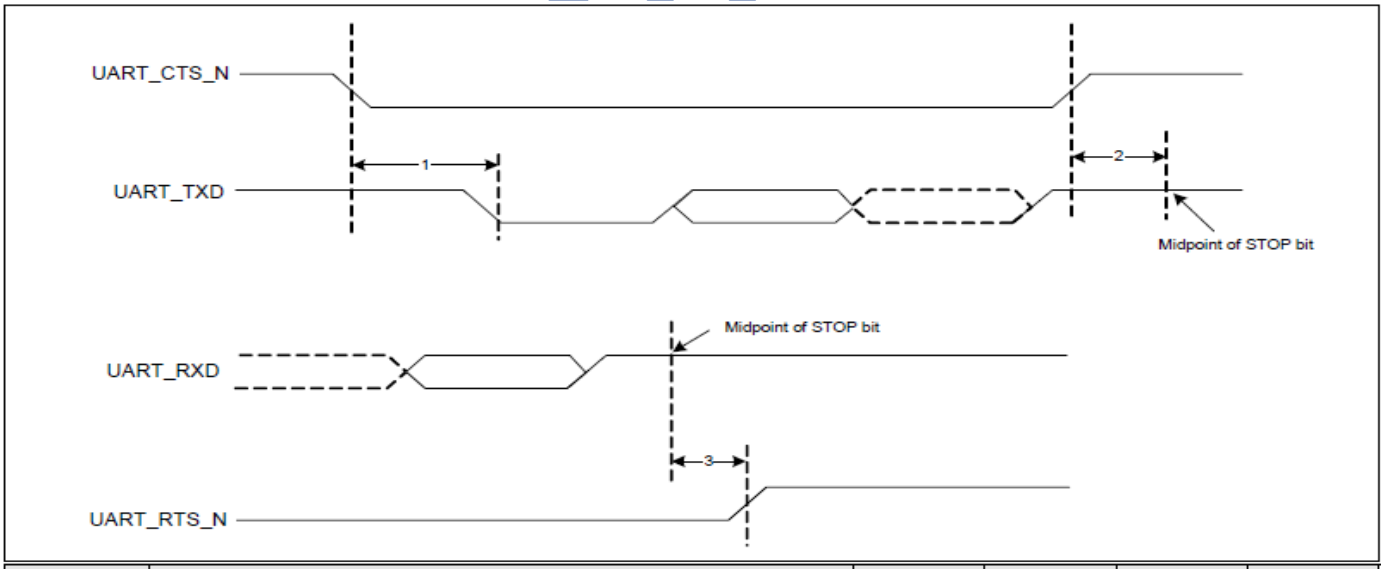
3 TIMING DIAGRAM OF INTERFACE

3.1 POWER-UP SEQUENCE AND TIMING

The WM-BAC-CYW-50 MCU host module has three power signals that allow to control power up by the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see below Figure).The timing values indicated are minimum required values;longer delays are also acceptable.



3.2 UART TIMING

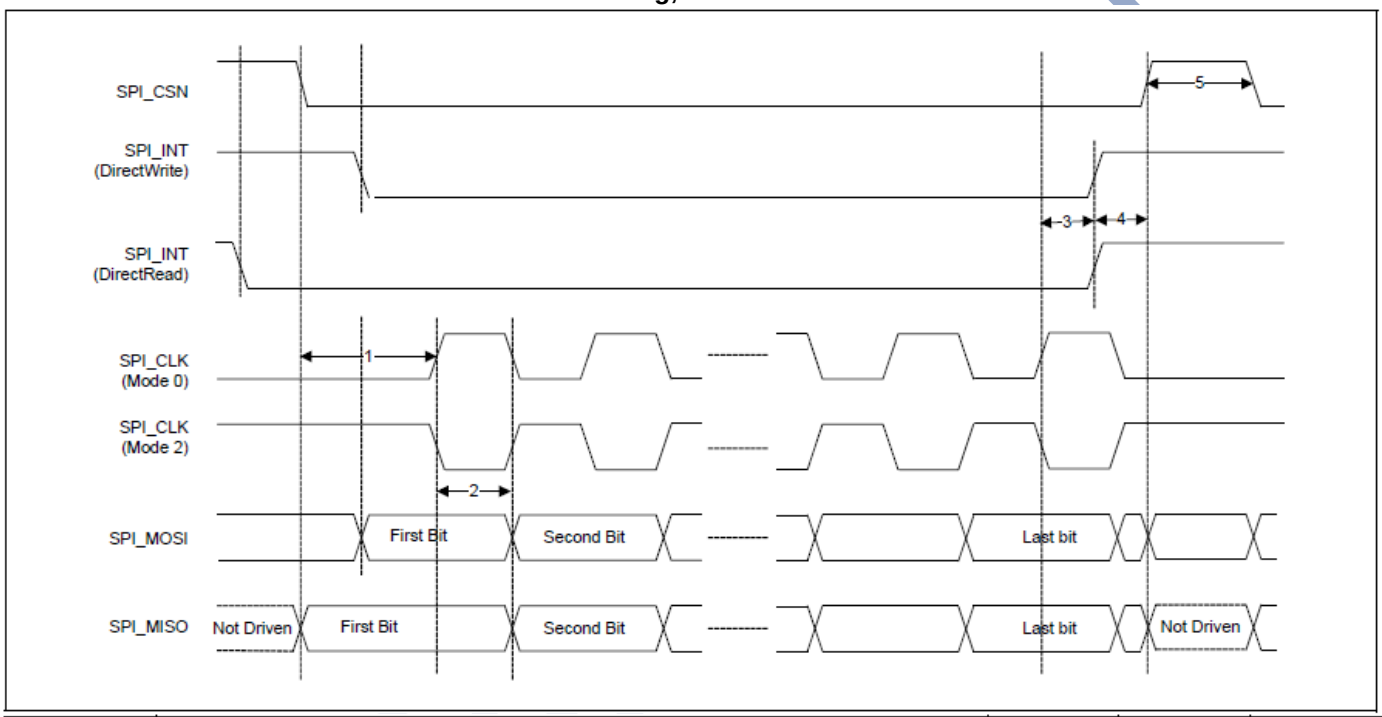


Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

3.3 SPI TIMING

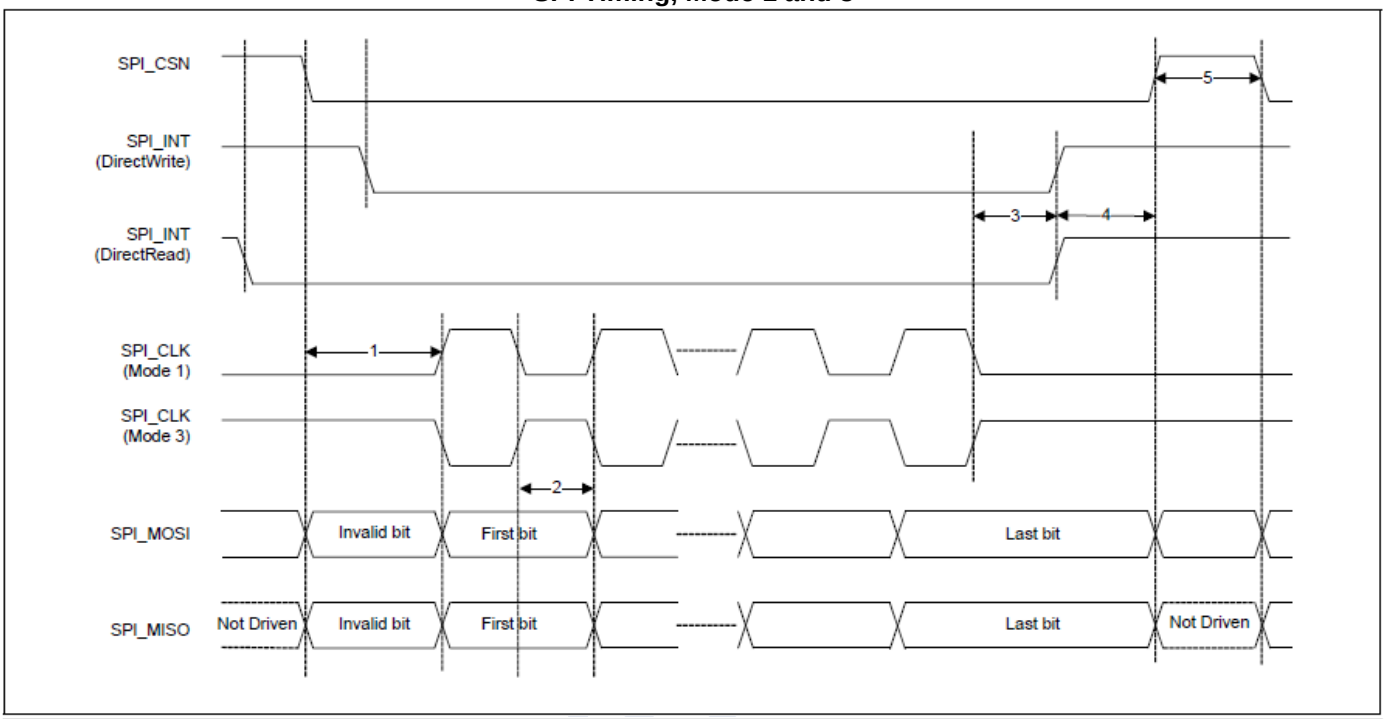
The SPI interface can be clocked up to 24 MHz.

SPI Timing, Mode 0 and 2



Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

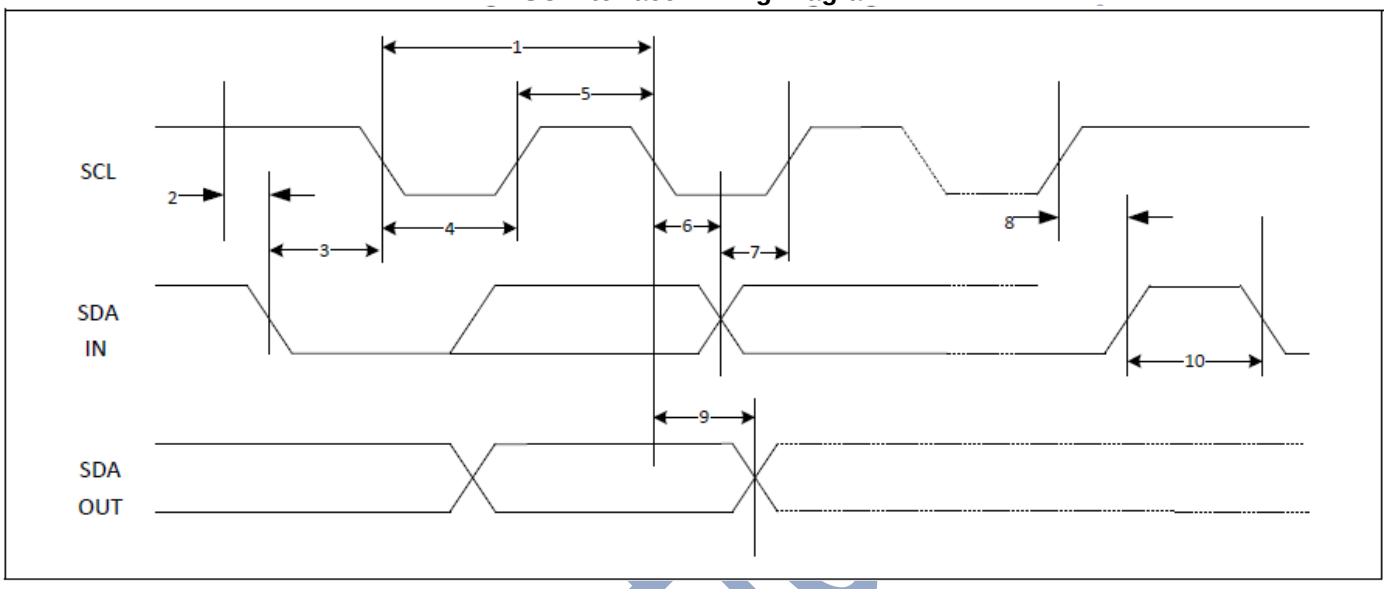
SPI Timing, Mode 1 and 3



Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

3.4 BSC INTERFACE TIMING

BSC Interface Timing Diagram

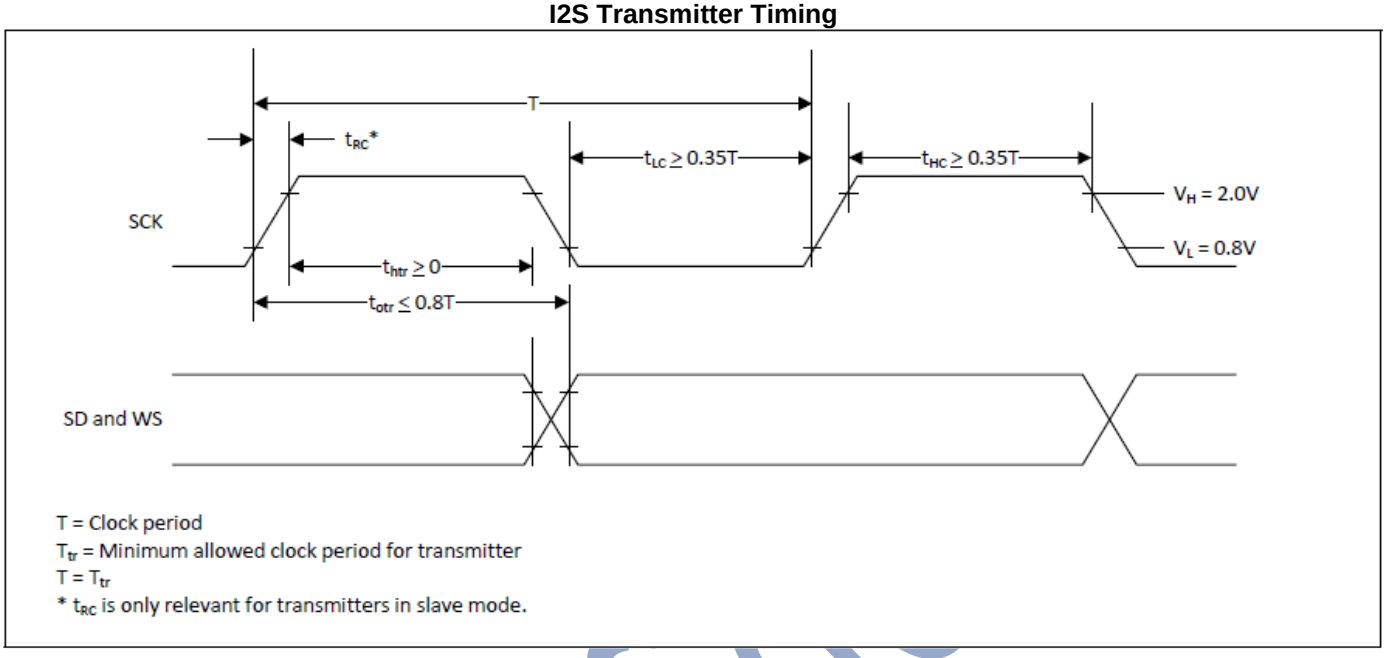


BSC Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[a]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[b]	650	–	ns

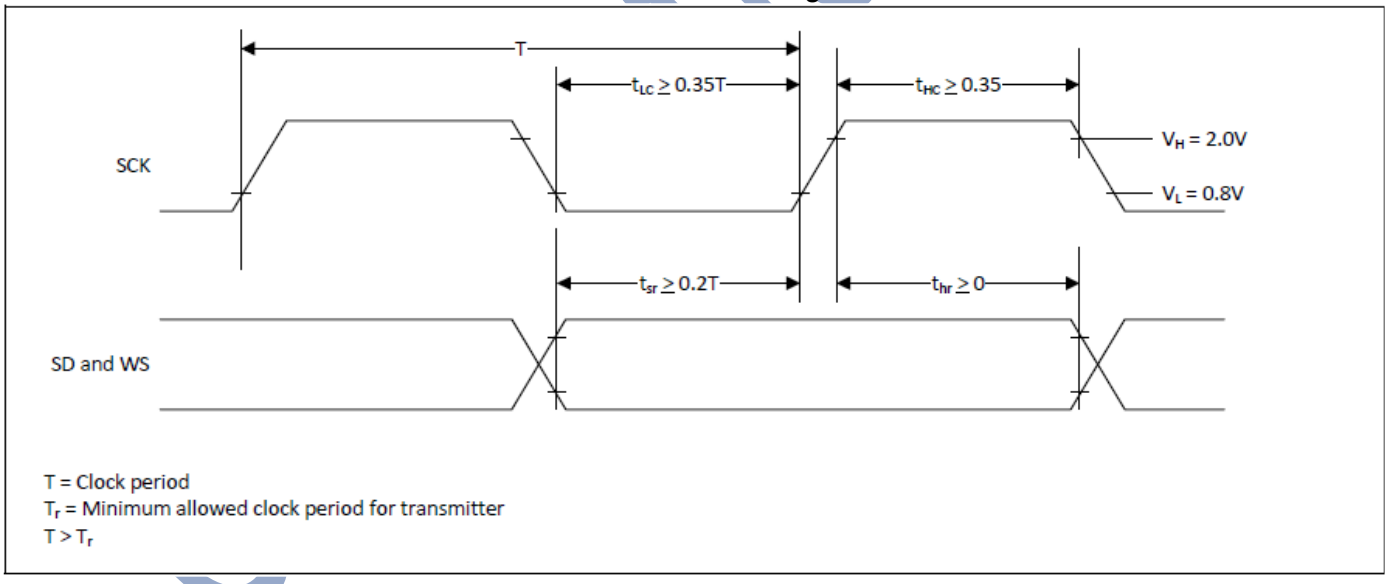
a. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
b. Time that the CBUS must be free before a new transaction can start.

I2S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

I2S Receiver Timing



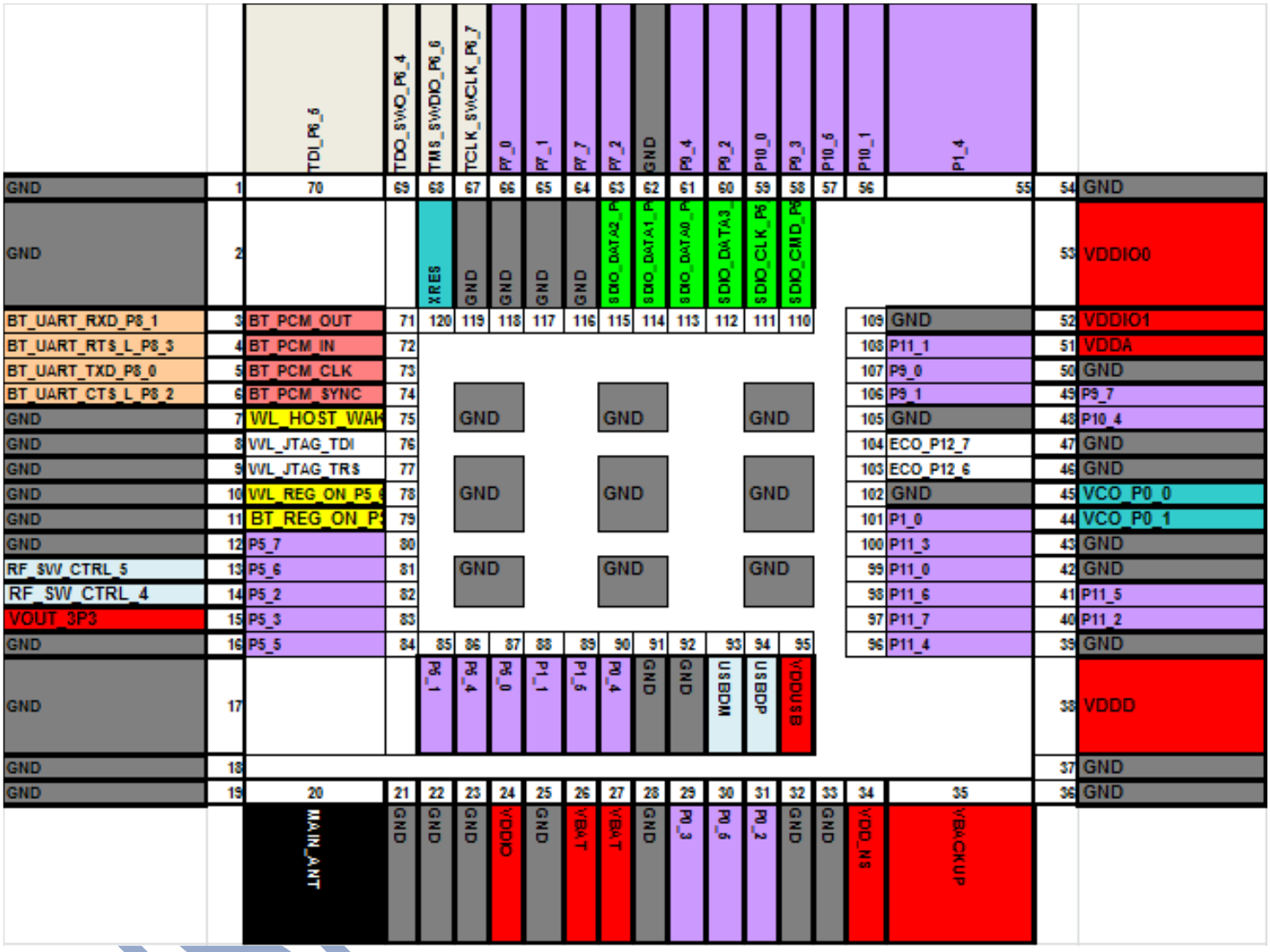
T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Timing for I2S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_{tr}$	–	–	–	f
Hold time t_{hr}	–	–	–	–	$0.2T_{tr}$	–	–	–	f

a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

4 PIN MAP



TOP View

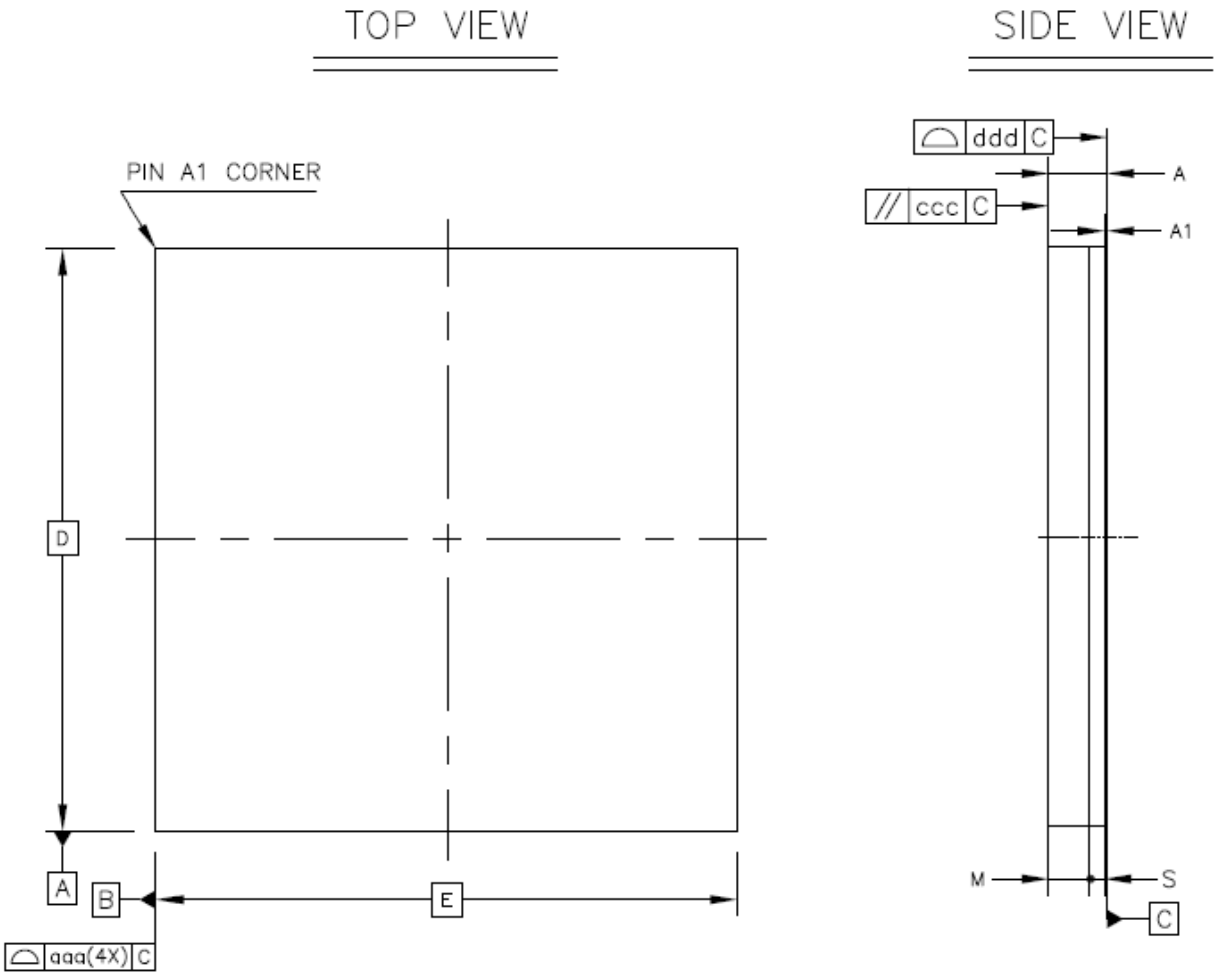
Pin#	Pin Name	Type	Description
1	GND	PWR	GND Pin
2	GND	PWR	GND Pin
3	BT_UART_RXD_P8_1	I/O	Connect to 43012 BT_UART_RXD and PSoC6 P8_1
4	BT_UART_RTS_L_P8_3	I/O	Connect to 43012 BT_UART_RTS and PSoC6 P8_3
5	BT_UART_TXD_P8_0	I/O	Connect to 43012 BT_UART_TXD and PSoC6 P8_0
6	BT_UART_CTS_L_P8_2	I/O	Connect to 43012 BT_UART_CTS and PSoC6 P8_2
7	GND	PWR	GND Pin
8	GND	PWR	GND Pin
9	GND	PWR	GND Pin
10	GND	PWR	GND Pin
11	GND	PWR	GND Pin
12	GND	PWR	GND Pin
13	RF_SW_CTRL_5	I/O	43012 RF_SW_CTRL_5 Pin
14	RF_SW_CTRL_4	I/O	43012 RF_SW_CTRL_4 Pin
15	VOUT_3P3	PWR	43012 VOUT_3P3 Power Pin
16	GND	PWR	GND Pin
17	GND	PWR	GND Pin
18	GND	PWR	GND Pin
19	GND	PWR	GND Pin
20	MAIN_ANT	I/O	RF ANT pin
21	GND	PWR	GND Pin
22	GND	PWR	GND Pin
23	GND	PWR	GND Pin
24	VDDIO	I/O	43012 VDDIO Power Pin
25	GND	PWR	GND Pin
26	VBAT	PWR	43012 VBAT Power Pin
27	VBAT	PWR	43012 VBAT Power Pin
28	GND	PWR	GND Pin
29	P0_3	I/O	PSoC6 P0_3 Pin
30	P0_5	I/O	PSoC6 P0_5 Pin
31	P0_2	I I/O	PSoC6 P0_2 Pin
32	GND	PWR	GND Pin
33	GND	PWR	GND Pin
34	VDD_NS	PWR	PSoC6 VDD_NS Power Pin
35	VBACKUP	PWR	PSoC6 VBACKUP Power Pin

36	GND	PWR	GND Pin
37	GND	PWR	GND Pin
38	VDDD	I/O	PSoC6 VDDD Power Pin
39	GND	PWR	GND Pin
40	P11_2	I/O	PSoC6 P11_2 Pin
41	P11_5	I/O	PSoC6 P11_5 Pin
42	GND	PWR	GND Pin
43	GND	PWR	GND Pin
44	VCO_P0_0	I/O	32.768KHz Clock In
45	VCO_P0_1	I/O	32.768KHz Clock Out
46	GND	PWR	GND Pin
47	GND	PWR	GND Pin
48	P10_4	I/O	PSoC6 P10_4 Pin
49	P9_7	I/O	PSoC6 P9_7 Pin
50	GND	PWR	GND Pin
51	VDDA	PWR	PSoC6 VDDA Power Pin
52	VDDIO1	PWR	PSoC6 VDDIO1 Power Pin
53	VDDIO0	PWR	PSoC6 VDDIO0 Power Pin
54	GND	PWR	GND Pin
55	P1_4	I/O	PSoC6 P1_4Pin
56	P10_1	I/O	PSoC6 P10_1 Pin
57	P10_5	I/O	PSoC6 P10_5 Pin
58	P9_3	I/O	PSoC6 P9_3 Pin
59	P10_0	I/O	PSoC6 P10_0 Pin
60	P9_2	I/O	PSoC6 P9_2 Pin
61	P9_4	I/O	PSoC6 P9_4 Pin
62	GND	PWR	GND Pin
63	P7_2	I/O	PSoC6 P7_2 Pin
64	P7_7	I/O	PSoC6 P7_7 Pin
65	P7_1	I/O	PSoC6 P7_1 Pin
66	P7_0	I/O	PSoC6 P7_0 Pin
67	TCLK_SWCLK_P6_7	I/O	Connect to PSoC6 P6_7
68	TMS_SWDIO_P6_6	I/O	Connect to PSoC6 P6_6
69	TDO_SWO_P6_4	I/O	Connect to PSoC6 P6_4
70	TDI_P6_5	I/O	Connect to PSoC6 P6_5
71	BT_PCM_OUT	I/O	Connect to 43012 PCM_OUT
72	BT_PCM_IN	I/O	Connect to 43012 PCM_IN

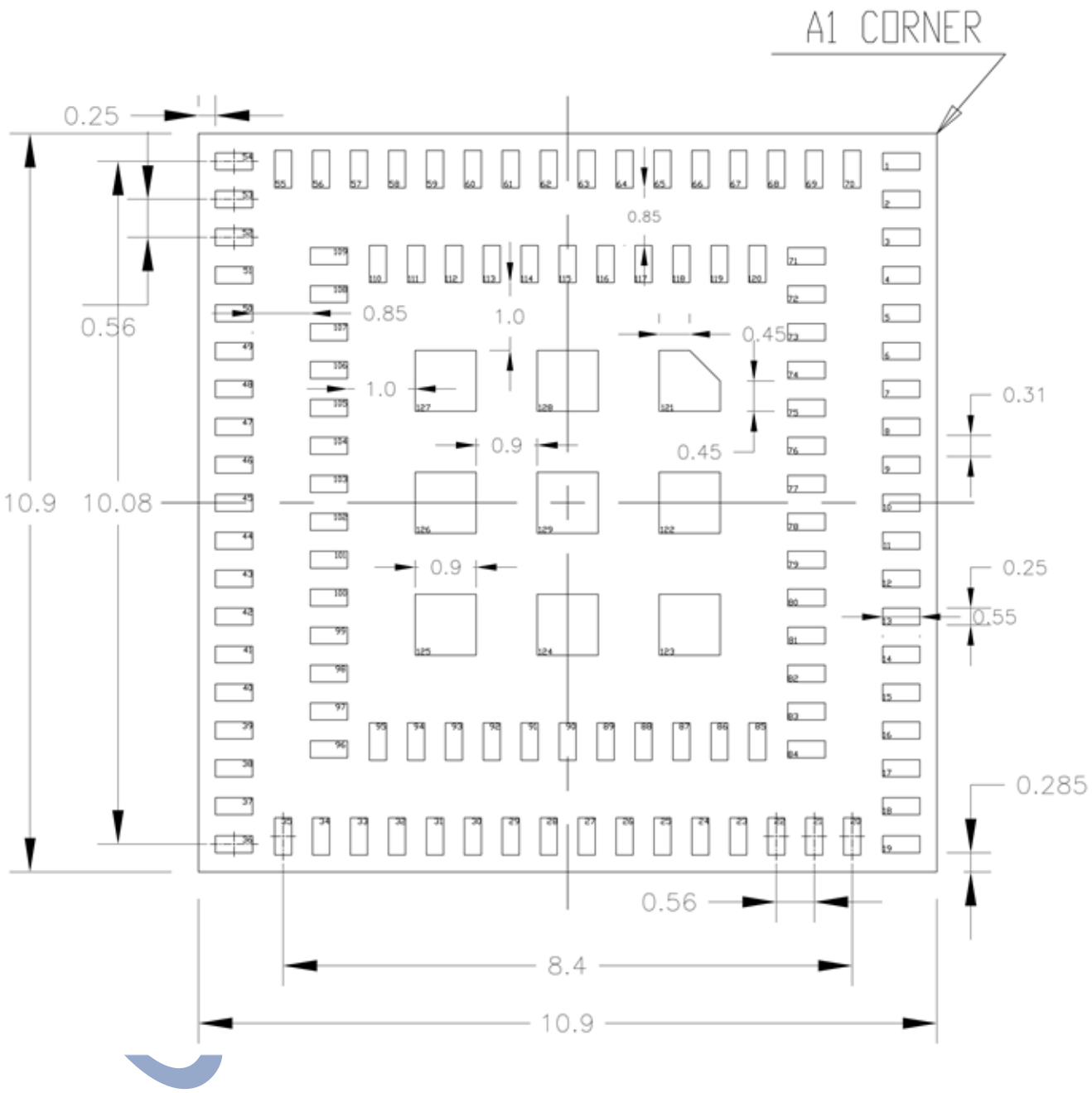
73	BT_PCM_CLK	I/O	Connect to 43012 PCM_CLK
74	BT_PCM_SYNC	I/O	Connect to 43012 PCM_SYNC
75	WL_HOST_WAKE_P6_0	I/O	Connect to 43012 WL_HOST_WAKE and PSoC6 P6_0
76	WL_JTAG_TDI	I/O	Connect to 43012 WL_JTAG_TDI
77	WL_JTAG_TRS	I/O	Connect to 43012 WL_JTAG_TRS
78	WL_REG_ON_P6_2	I/O	Connect to 43012 WL_REG_ON and PSoC6 P6_2
79	BT_REG_ON_P6_3	I/O	Connect to 43012 BT_REG_ON and PSoC6 P6_3
80	P5_7	I/O	PSoC6 P5_7 Pin
81	P5_6	I/O	PSoC6 P5_6 Pin
82	P5_2	I/O	PSoC6 P5_2 Pin
83	P5_3	I/O	PSoC6 P5_3 Pin
84	P5_5	I/O	PSoC6 P5_5 Pin
85	P5_1	I/O	PSoC6 P5_1 Pin
86	P5_4	I/O	PSoC6 P5_4 Pin
87	P5_0	I/O	PSoC6 P5_0 Pin
88	P1_1	I/O	PSoC6 P1_1 Pin
89	P1_5	I/O	PSoC6 P1_5 Pin
90	P0_4	I/O	PSoC6 P0_4 Pin
91	GND	PWR	GND Pin
92	GND	PWR	GND Pin
93	USBDM	I/O	PSoC6 USBDM Pin
94	USBDP	I/O	PSoC6 USBDP Pin
95	VDDUSB	PWR	PSoC6 VDDUSB Power Pin
96	P11_4	I/O	PSoC6 P11_4 Pin
97	P11_7	I/O	PSoC6 P11_7 Pin
98	P11_6	I/O	PSoC6 P11_6 Pin
99	P11_0	I/O	PSoC6 P11_0 Pin
100	P11_3	I/O	PSoC6 P11_3 Pin
101	P1_0	I/O	PSoC6 P1_0 Pin
102	GND	PWR	GND Pin
103	ECO_P12_7	I/O	ECO Clock Out
104	ECO_P12_6	I/O	ECO Clock In
105	GND	PWR	GND Pin
106	P9_1	I/O	PSoC6 P9_1 Pin
107	P9_0	I/O	PSoC6 P9_0 Pin
108	P11_1	I/O	PSoC6 P11_1 Pin
109	GND	PWR	GND Pin

110	SIDO_CMD_P12_5	I/O	Connect to 43012 SIDO_CMD and PSoC6 P12_5
111	SDIO_CLK_P12_0	I/O	Connect to 43012 SDIO_CLK and PSoC6 P12_0
112	SIDO_DATA_3_P12_4	I/O	Connect to 43012 SIDO_DATA_3 and PSoC6 P12_4
113	SIDO_DATA_0_P12_1	I/O	Connect to 43012 SIDO_DATA_0 and PSoC6 P12_1
114	SIDO_DATA_1_P12_2	I/O	Connect to 43012 SIDO_DATA_1 and PSoC6 P12_2
115	SIDO_DATA_2_P12_3	I/O	Connect to 43012 SIDO_DATA_2 and PSoC6 P12_3
116	GND	PWR	GND Pin
117	GND	PWR	GND Pin
118	GND	PWR	GND Pin
119	GND	PWR	GND Pin
120	XRES	I/O	System Reset
121	GND	PWR	GND Pin
122	GND	PWR	GND Pin
123	GND	PWR	GND Pin
124	GND	PWR	GND Pin
125	GND	PWR	GND Pin
126	GND	PWR	GND Pin
127	GND	PWR	GND Pin
128	GND	PWR	GND Pin
129	GND	PWR	GND Pin

5 PHYSICAL SPECIFICATIONS



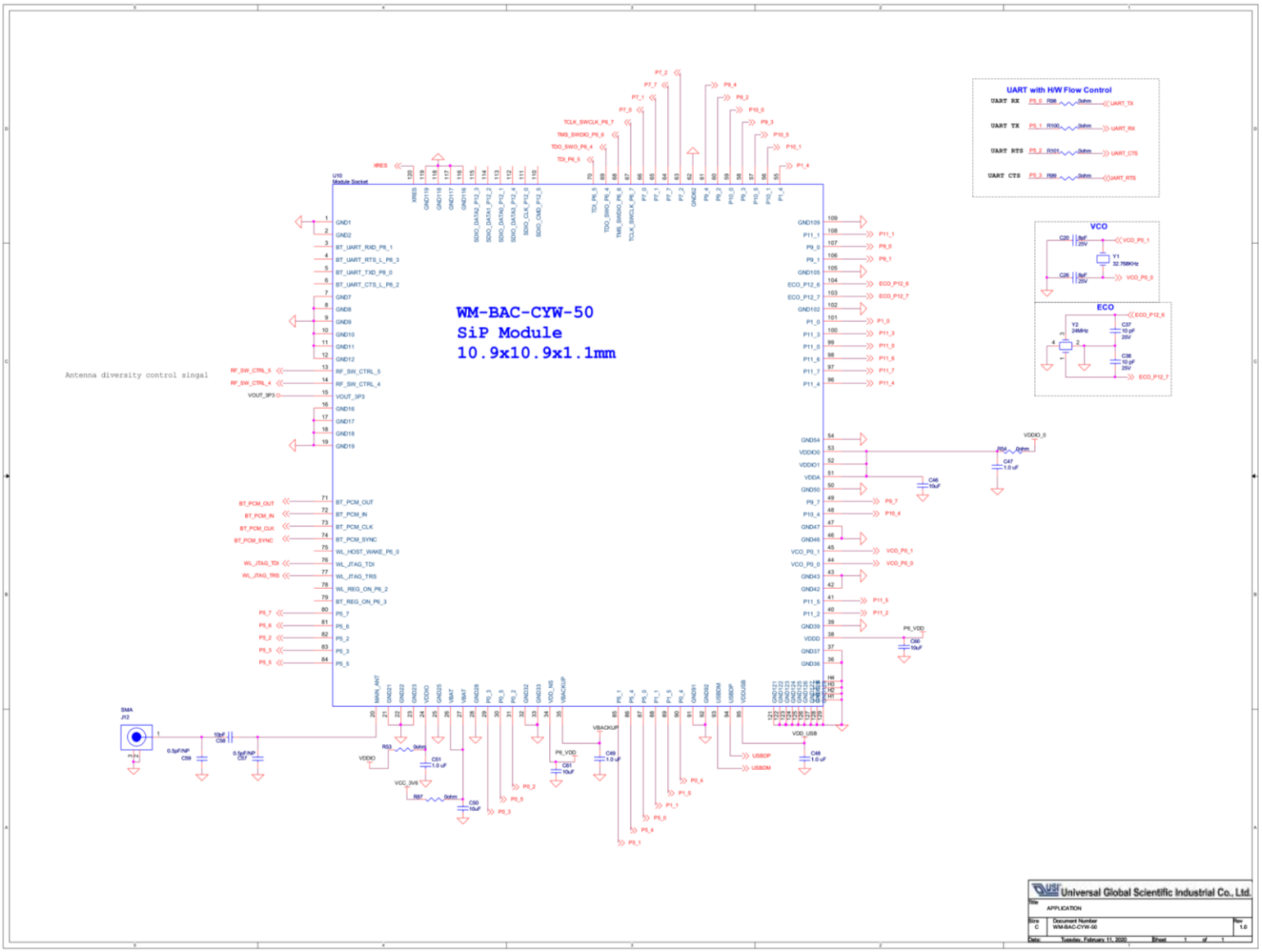
		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			PIM		
Body Size:	X	E	10.900		
	Y	D	10.900		
Total Thickness :		A	–	–	1.100
Mold Thickness :		M	0.750 Ref.		
Substrate Thickness :		S	0.300 Ref.		
Lead Thickness:		A1	–	–	0.050
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		ccc	0.100		
Coplanarity:		ddd	0.080		



Bottom View

*all dimension tolerance ±0.1mm

6 APPLICATION REFERENCE DESIGN

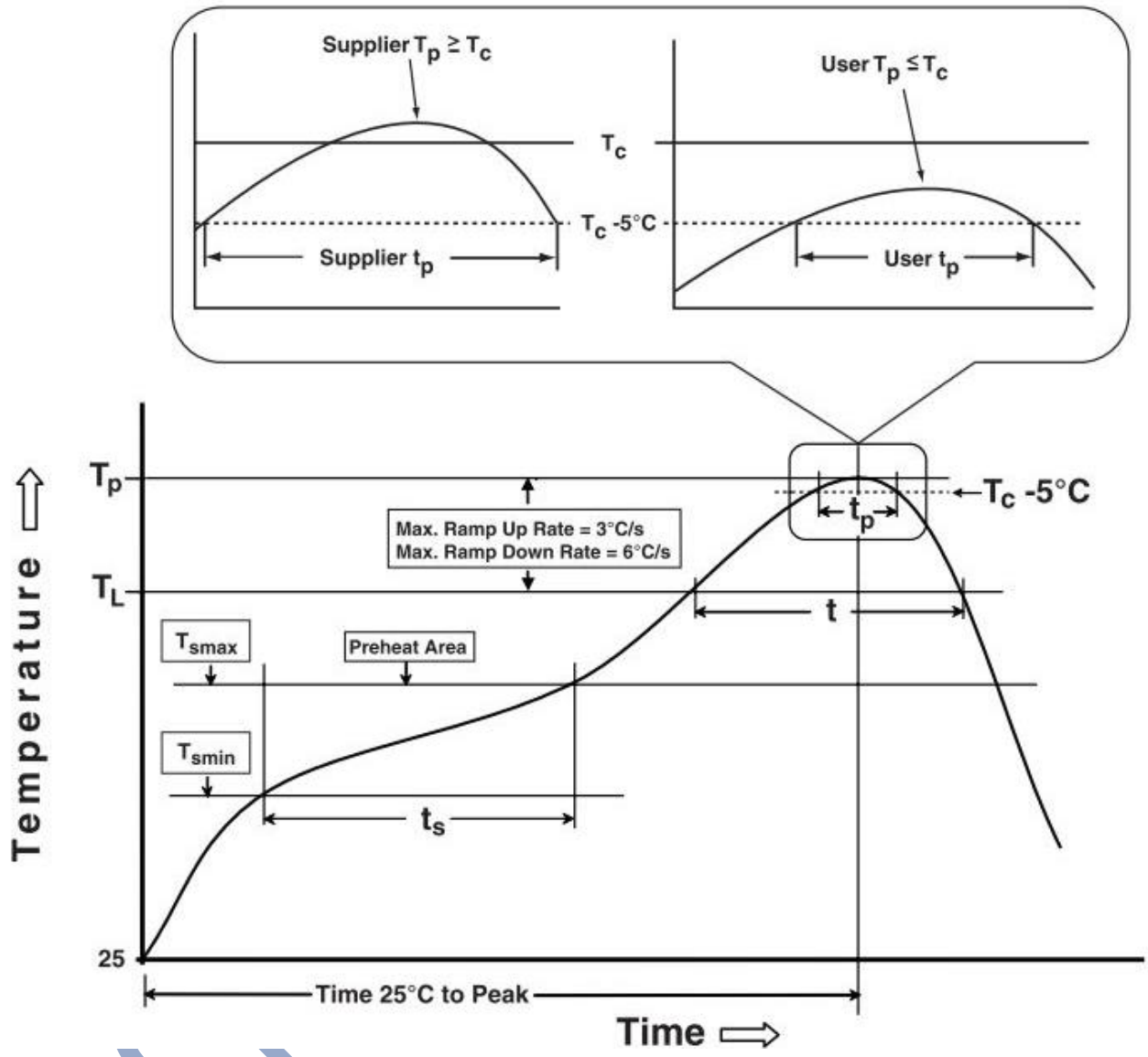


7 RECOMMENDED REFLOW PROFILE

The module is compliant with JEDEC-020D standard that can guarantee the module to endure the peak 260 degree C reflow profile without any problem.

Reflow profiles

Critical Profiles Parameters	Pb-Free assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	260ºC ± 2ºC
Time (tp)* within 5 °C of the specified classification temperature (Tc), see Figure 5-1.	30* seconds
Ramp-down rate (Tp to TL)	6°C/second max.
Time 25 °C to peak temperature	8 minutes max.



8 PACKAGE AND STORAGE CONDITION

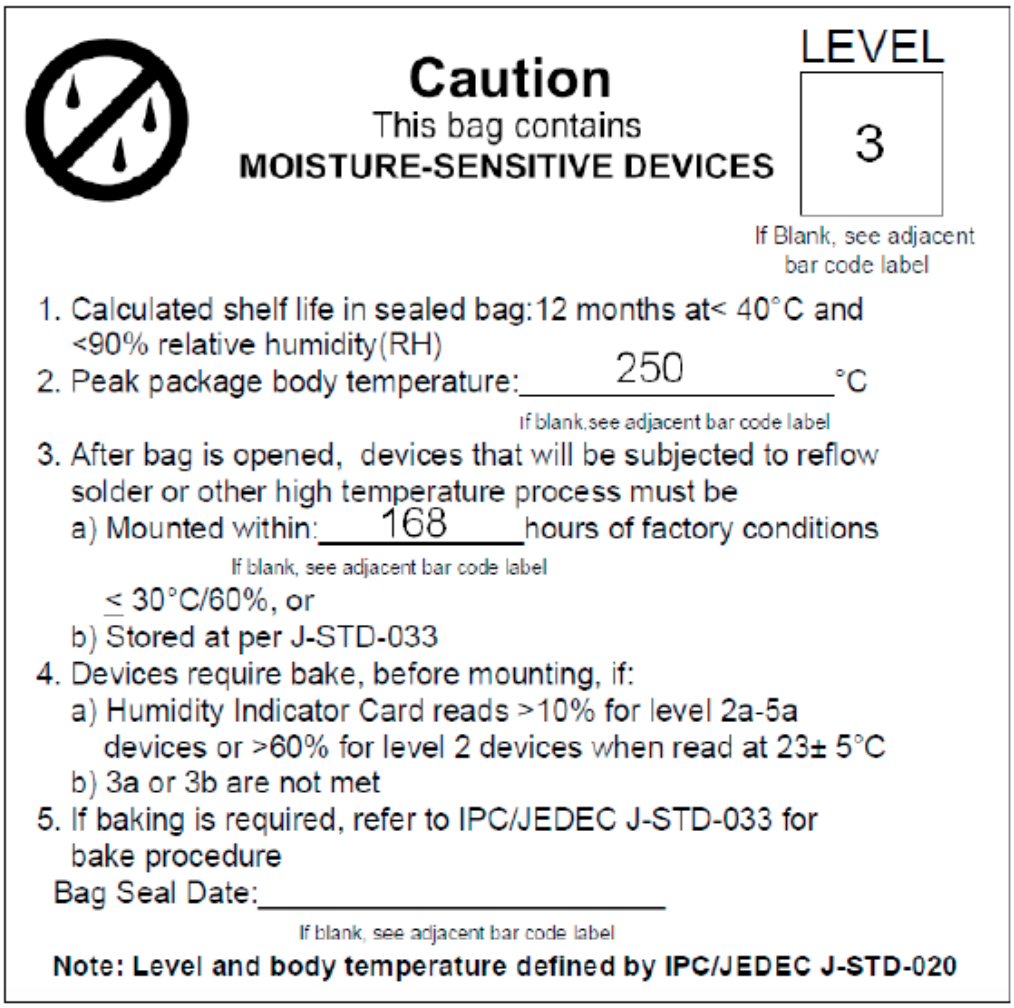
8.1 PACKAGE DIMENSION (TBD)

8.2 ESD LEVEL (TBD)

According to FCC and CE standard

1. Surface Resistively:
   Interior:10^9~10^{11}Ω/SQUARE
   EXTERIOR:10^8~10^{12}Ω/SQUARE
2. Dimension:TBD
3. Tolerance:+5,0mm
4. Color:
   Background : Gray
   Text : Red

8.3 MOISTURE SENSITIVE LABEL



Half-Sine Shock
Sustained for Mechanical Shock under 2000G

Product Warranty: 1 year