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SPECIFICATION

CUSTOMER :

MODULE NO.:

WF320240C-TXI#

APPROVED BY:		
(FOR CUSTOMER USE ONLY)		
	PCB VERSION:	DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

	Winstar Display Co., LTD MODLE NO :							
	凌光電股份有限 ORDS OF REV		DOC. FIRST ISSUE					
	1							
VERSION	DATE	PAGE NO.	SUMMARY					
0	2006-06-06		First issue					
A	2006.12.04	14	Add contour drawing.					
В	2007.02.01	6	Modify Vcc=3.3V					

Winstar reserves the right to change products and specifications without notice at any time.

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- **10. software (Register Initiate code)**

1. Module Classification Information

This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of WWTFT3.5AI-0#

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	77.5 x 64.4 x 3.2	mm
Active area	70.08 x 52.56	mm
Dot pitch	0.073 x 0.219	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED,Normally White	

*Epose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.



2.Block Diagram



3.Electrical Characteristics

Item	Symbol	Condition	Min	Тур	Max	Unit
Supply Voltage For Logic	VCC		3.0	3.3	3.6	V
Input High Volt.	V _{IH}	—	0.7 V _{CC}	_	V _{CC}	V
Input Low Volt.	V _{IL}	_	0	_	0.3Vcc	V
Power Supply Voltage	V_{GH}	Ta=25°℃	_	15.0		V
i ower suppry voluge	V _{GL}	Ta=25°℃		-10		V
Supply Current	I _{cc}	V _{CC} =5		250	280	mA (*NOTE1)

*NOTE1:MIN. and MAX. Voltage is specified ac the voltage within the condition

Temperature rang -0°C ~70°C

Typ. Voltage is specified as module driving condition : Ta=25°C, Vop at Optimum Contrast

4.Absolute Maximum Ratings

Item	Symbol	Min	Тур	Max	Unit
Operating Temperature	T _{OP}	0		+70	°C
Storage Temperature	T _{ST}	0		+80	°C
	V _{GH}	-0.3		18	V
Power Supply Voltage	V _{GL}	-15		+70 +80	V
11 7 1 100	VCC	-0.3			V

5.Interface Pin Function

P/N	Symbol	Function	P/N	Symbol	Function
1	Vcc	Power Supply : +5V	26	GND	Ground for logic circuit
2	BL_C	Backlight control signal	27	NC	No Connection
3	DB0		28	GND	Ground for logic circuit
4	DB1		29	AD0	System address bus bits
5	DB2		30	GND	Ground for logic circuit
6	DB3		31	AD1	System address bus bits
7	DB4		32	GND	Ground for logic circuit
8	DB5		33	AD2	System address bus bits
9	DB6		34	GND	Ground for logic circuit
10	DB7	Input data from the system data	35	AD3	System address bus bits
11	DB8	bus.	36	GND	Ground for logic circuit
12	DB9		37	AD4	
13	DB10		38	AD5	
14	DB11		39	AD6	
15	DB12		40	AD7	
16	DB13		41	AD8	
17	DB14		42	AD9	
18	DB15		43	AD10	
19	CS	Chip select input.	44	AD11	System address bus bits
20	MR	See Note(1)	45	AD12	System address bus bits
21	RD	this pin inputs the read command	46	AD13	
22	WR	write enable signal	47	AD14	
23	BHE	This pin inputs the byte enable	48	AD15	
		signal for the high data byte			
24	REST	Active low input to set all internal	49	AD16	
		registers to the default state			
25	WAIT	This pin outputs the wait signal	50	AD17	

5-1 Pins Connection To Control Board

Note(1): This input pin is used to select between the display buffer and register address spaces of the S1D13A04. M/R# is set high to access the display buffer and low to access the registers.

6.<u>Timing Characteristics</u>



6-1.Interface Timing

Symbol	Parameter	Min	Max	Unit
f _{BUSCLK}	Bus clock frequency		50	MHz
T _{BUSCLK}	Bus clock period	1/f _{BUSCLK}		ns
t1	A[16:0], M/R#, BHE# setup to first BUSCLK rising edge where CS# = 0 and either RD# = 0 or WE# = 0	9		ns
t2	CS# setup to BUSCLK rising edge	9		ns
t3	RD#, WE# setup to BUSCLK rising edge	1		ns
t4	RD# or WE# state change to WAIT# driven low	1	10	ns
t5	RD# falling edge to D[15:0] driven (read cycle)	2	10	ns
t6	D[15:0] setup to 4th rising BUSCLK edge after CS#=0 and WE#=0	1		T _{BUSCLK}
t7	A[16:0], M/R#, BHE# and CS# hold from RD#, WE# rising edge	0		ns
t8	CS# deasserted to reasserted	0		ns
t9	WAIT# rising edge to RD#, WE# rising edge	0		ns
t10	WE#, RD# deasserted to reasserted	1		TBUSCLK
t11	Rising edge of either RD# or WE# to WAIT# high impedance		0.5	T _{BUSCLK}
t12	D[15:0] hold from WE# rising edge (write cycle)	2		ns
t13	D[15:0] hold from RD# rising edge (read cycle)	1		ns
t14	Cycle Length	6		TBUSCLK

WE#	RD#	BHE#	A0	D[15:8]	D[7:0]	Comments		
0	1	0	0	valid	valid	16-bit write		
0	1	1	0	-	valid	8-bit write at even address		
0	1	0	1	valid	-	8-bit write at odd address		
1	0	0	0	valid	valid	16-bit read		
1	0	1	0	-	valid	8-bit read at even address		
1	0	0	1	valid	-	8-bit read at odd address		

6-2. Interface Truth Table for Little Endian

7.Optical Characteristics

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
	θ∟	Φ=180°(9 o'clock)	55	65	-		
Viewing angle	θ _R	Φ=0°(3 o'clock)	55	65	-	degree	Note 1
(CR≥10)	θτ	Φ=90°(12 o'clock)	35	45	-		Note 1
	θ _B	Φ=270°(6 o'clock)	55	65	-		
Pospopso Timo	T _{ON}		-	15	30	msec	Note 3
Response Time	T _{OFF}		-	20	50	msec	Note 3
Contrast ratio	CR		200	300	-	-	Note 4
Color obromoticity	Wx	Normal θ=Φ=0°	-	(0.33)	-	-	Note 5
Color chromaticity	W _Y		-	(0.36)	-	-	Note 6
Luminance	L		150	200	-	cd/m ²	Note 6
Luminance uniformity	YU		70	75	-	%	Note 7

Test Conditions:

- 1. V_{CC}=3.3V, AV_{DD}=5.0V, I_L=20mA (Backlight current), the ambient temperature is 25° C. 2. The test systems refer to Note 2.

7.1 Definition of optical characteristics



Fig. 5-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)



Fig. 5-2 Optical measurement system setup The copyright belongs to InnoLux. Any unauthorized use is prohibited. Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Fig. 5-3 Definition of response time

Note 4: Definition of contrast ratio

Contrast ratio (CR) = <u>Luminance measured when LCD is on the "White" state</u> <u>Luminance measured when LCD is on the "Black" state</u>

- Note 5: Definition of color chromaticity (CIE1931) Color coordinates measured at center point of LCD.
- Note 6: All input terminals LCD panel must be ground when measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity

To test for uniformity, the tested area, which is inside the active area, is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each box.

Luminance Uniformity (Yu) =
$$\frac{B_{min}}{B_{max}}$$

L-----Active area length

W----- Active area width





B_{max}: The measured maximum luminance of all measurement position. **B**_{min}: The measured minimum luminance of all measurement position.







9. Inspection specification

NO	Item	Criterion	AQL			
01	Electrical Testing	 1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character , dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect. 				
02	Black or white spots on LCD (display only)	 2.1 White and black spots on display ≤0.25mm, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm 				
03	LCD black spots, white spots,	3.1 Round type : As following drawing $\Phi = (x + y) / 2$ SIZEAcceptable Q TYXImage: Colspan="3"> $\Phi \le 0.10$ XImage: Colspan="3"> $\Phi \le 0.20$ XImage: Colspan="3"> $\Phi \le 0.20$ XImage: Colspan="3"> $\Phi \le 0.20$ YImage: Colspan="3"> $0.20 < \Phi \le 0.25$ Image: Colspan="3"> $0.25 < \Phi$ Image: Colspan="3"> $0.25 < \Phi$	2.5			
contamina (non-disp	(non-display)	3.2 Line type : (As following drawing) \mathbf{W} LengthWidthAcceptable Q TY \mathbf{W} \mathbf{W} $\mathbf{W} \leq 0.02$ Accept no dense $\mathbf{L} \leq 3.0$ $0.02 < W \leq 0.03$ 2 $\mathbf{L} \leq 2.5$ $0.03 < W \leq 0.05$ 2 $\mathbf{U} \leq 2.5$ $0.05 < W$ As round type	2.5			
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.Size Φ Acceptable Q TY $\Phi \leq 0.20$ Accept no dense $0.20 < \Phi \leq 0.50$ 3 $0.50 < \Phi \leq 1.00$ 2 $1.00 < \Phi$ 0Total Q TY3	2.5			

05ScratchesFollow NO.3 LCD black spots, white spots, contaminationSymbols Define: x: Chip length k: Seal width t: Glass thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length: 6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:6.1 Chipped glass106Chipped glass107107108109109109109100101101102102103104105105106107107108109109109100100101102103104104105105106107107108109 <t< th=""><th>NO</th><th>Item</th><th></th><th>Criterion</th><th></th><th>AQL</th></t<>	NO	Item		Criterion		AQL
$06 \begin{array}{c} \text{Chipped} \\ \text{glass} \end{array} \left[\begin{array}{c} \text{x: Chip length} & \text{y: Chip width} & \text{z: Chip thickness} \\ \text{x: Seal width} & \text{t: Glass thickness} & \text{a: LCD side length} \\ \text{L: Electrode pad length:} \\ \hline 6.1 \text{ General glass chip :} \\ \hline 6.1.1 \text{ Chip on panel surface and crack between panels:} \\ \hline & \hline$	05	Scratches				
z: Chip thicknessy: Chip widthx: Chip length $Z \le 1/2t$ Not over viewing area $x \le 1/8a$ $1/2t < z \le 2t$ Not exceed $1/3k$ $x \le 1/8a$		Chipped	Symbols Define: x: Chip length k: Seal width t: Glass L: Electrode pad length:6.1 General glass chip : 6.1.1 Chip on panel surface a $\boxed{1.1 Chip on panel surface a}$ $\boxed{2 \le 1/2t}$ $\boxed{2 \le 1/2t}$ $\boxed{1/2t < z \le 2t}$ $\boxed{1.2 Corner crack:}$ $\boxed{2 \le 1/2t}$	width z: Chip t s thickness a: LCD s and crack between par with the set of th	thickness side length nels: $x \ge 1/8a$ $x \le 1/8a$ ch chip. $x \ge 1/8a$	2.5



NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	 8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong. 	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination.9.2 Bezel must comply with job specifications.	2.5 0.65
10	РСВ、СОВ	 10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	 11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB. 	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	 12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet. 	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

10. software (Register Initiate code)

struct easy code S1D_REGS[]=

{
ι.

{ 0x14,	0x00000000 },	/* Power Save Configuration Register	*/ \
{ 0x64,	0x28D70000 },	/* GPIO Status and Control Register	*/ \
{ 0x04,	$0x00000000$ },	/* Memory Clock Configuration Register	*/ \
{ 0x08,	0x00000032 },	/* Pixel Clock Configuration Register	*/ \
{ 0x0C,	0x00000061 },	/* Panel Type and MOD Rate Register	*/ \
$\{ 0x10, $	0x00000010 },	/* Display Settings Register	*/ \
{ 0x20,	0x00000037 },	/* Horizontal Total Register	*/ \
{ 0x24,	0x00000027 },	/* Horizontal Display Period Register	*/ \
{ 0x28,	0x0000000F },	/* Horizontal Display Period Start Position Register	*/ \
{ 0x2C,	0x00870156 },	/* FPLINE Register	*/ \
{ 0x30,	0x00000105 },	/* Vertical Total Register	*/ \
{ 0x34,	0x000000EF },	/* Vertical Display Period Register	*/ \
{ 0x38,	0x000000D },	/* Vertical Display Period Start Position Register	*/ \
{ 0x3C,	0x00800000 },	/* FPFRAME Register	*/ \
{ 0x40,	0x00000000 },	/* Main Window Display Start Address Register	*/ \
{ 0x44,	0x000000A0 },	/* Main Window Line Address Offset Register	*/ \
{ 0x50,	0x00000000 },	/* PIP+ Window Display Start Address Register	*/ \
{ 0x54,	0x00000A0 },	/* PIP+ Window Line Address Offset Register	*/ \
{ 0x58,	0x00000000 },	/* PIP+ Window X Positions Register	*/ \
{ 0x5C,	0x00000000 },	/* PIP+ Window Y Positions Register	*/ \
{ 0x60,	0x00000000 },	/* Special Purpose Register	*/ \
{ 0x70,	0x00000000 },	/* PWM Clock Configuration Register	*/ \
{ 0x74,	$0x00000000$ },	/* PWMOUT Duty Cycle Register	*/ \
{ 0x80,	$0x00000000$ },	/* Scratch Pad A Register	*/ \
{ 0x84,	$0x00000000$ },	/* Scratch Pad B Register	*/ \
{ 0x88,	0x00000000 },	/* Scratch Pad C Register	*/ \
{ S1D_REGE			*/ \
{ 0x64,	0x28D70001 },	/* GPIO Status and Control Register	*/ \
{ 0x14,	0x00000000 }	/* Power Save Configuration Register	*/ \
};	,		

Number:			Page: 1
Panel Specification :			1 4901 1
Panel Type :	Pass	NG,	
View Direction :	Pass		
Numbers of Dots :	Pass		
View Area:	Pass		
Active Area :	Pass		
Operating Temperature :	Pass		
Storage Temperature :	Pass		
Others :			
Mechanical Specification :			
PCB Size :	Pass	🗌 NG ,	
Frame Size :	Pass		
Material of Frame :	Pass		
Connector Position :	Pass		
Fix Hole Position :	Pass		
Backlight Position :	Pass		
Thickness of PCB :	Pass		
Height of Frame to PCB:	Pass		
Height of Module :	Pass		
). Others :	Pass		
Relative Hole Size :			
Pitch of Connector :	Pass	🗌 NG ,	
Hole size of Connector :	Pass		
Mounting Hole size :	Pass		
Mounting Hole Type :	Pass		
Others :	Pass		
Backlight Specification			
B/L Type :	Pass	□ NG ,	
B/L Color :	Pass	□ NG ,	
B/L Driving Voltage (Refere	nce for LED 7		
B/L Driving Current :	Pass	□ NG ,	
Brightness of B/L:	Pass	□ NG ,	
B/L Solder Method :	Pass	□ NG ,	
Others :	Pass	🗌 NG ,	

winstar

Module Number :

5、 <u>Electronic Characteristics of Module</u>:

- 1. Input Voltage :Pass2. Supply Current :Pass
- 3. Driving Voltage for LCD :
 Pass

Pass

Pass

Pass

- 8. LCD Uniformity :
- 9. ESD test :
- 10. Others :

6 <u>Summary</u> :

Page: 2

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Sales signature : _____

Customer Signature : _____

Date : / /