WESTERN DIGITAL CORP 54E D 9718228 0015716 936 WDC

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# *WD61C40A*

# *Peripheral Cache Manager Device*



WESTERN DIGITAL

30-0

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# 1.0 INTRODUCTION

## 1.1 FEATURES

- High-speed host bus transfers
  10.0 MTransfers per second in 16-bit mode (20 MBytes/s)
- Parallel disk interface - 80 Mbits NRZ in parallel mode (10 MBytes maximum, 5 MBytes nominal)
- Reed Solomon ECC data field
  - — Degree 6 with 3-way interleave with or without 4 CRC bytes
  - — Single burst on-the-fly correction
  - — Maximum of three bursts/interleave/sector correction with microprocessor intervention
  - — Maximum guaranteed single burst correction of 17 bits for on-the-fly operation
- Four byte ID CRC
- Data sector defect skipping support - programmable defect skip size
- Enhanced buffer management
  - — Memory segmentation
  - — Shared host/disk buffer count
- Embedded servo support
- Four port buffer management (host, disk, microprocessor, and buffer)
- Configurable buffer support
  - — With or without parity
  - — Programmable memory speed
- Disk Longitudinal Redundancy Checking (LRC) on write operations over logical blocks
- Pipelined buffer address/data counters for host and disk (2 levels)
- RAM-based writable disk control store
- Pass-through parity, checked on inputs of the host/disk FIFOs
- Minimum microprocessor intervention required
- Single +5V supply with low power mode
- 132-pin PQFP package with complete functionality
- Dedicated 8-bit port for high-speed microprocessor
- 25 MHz 80186 microprocessor support

## 1.2 GENERAL DESCRIPTION

The WD61C40A is a high-performance CMOS VLSI device that controls data transfers between the host port and the disk port through the local data buffer. It is primarily intended as a companion device to the WD33C96 Small Computer System Interface (SCSI) Controller.

The WD61C40A joins the basic functions of the WD10C01 and WD60C40A into a single package. It also provides additional functions:

- Reed Solomon on-the-fly ECC
- Parallel disk data bus
- Sector defect skipping
- Buffer memory segmentation
- Host-disk buffer count
- Enhanced control store functionality
- Wider host and buffer buses for improved bus bandwidth
- Minimal microprocessor intervention
- Skip mask support

There are two areas of major performance improvements. The first area is data transfer rate. The WD61C40A can maintain 20 Mbyte host port transfers and 5 Mbyte disk port transfers at a system clock of 47 MHz. This type of performance is achieved through the usage of a 16-bit host bus, a 16-bit buffer bus and an 8-bit disk bus. The disk port can also achieve a maximum transfer rate of 10 Mbytes.

The second area of improvement is key system functions. For example, the disk controller has on-chip Reed Solomon ECC generation, detection and correction logic. Defect skipping (the ability to write and read data around flaws on the disk) maximizes disk capacity while minimizing sector reallocation. The buffer manager also reduces microprocessor support. The buffer segmentation

and skip mask modes reduce interrupts to the microprocessor. Block mode operation also reduces interrupts.

The WD61C40A is flexible in a variety of ways. Three ports (host, disk, and buffer) support multiple pin configurations. The port data widths are 16 bits for host and 8 bits for the disk. Each port supports parity or no parity checking. The Disk Controller is based upon a writeable control store. The user can define the disk format of choice rather than using a fixed track format. The defect skipping option permits the dynamic variation of sector format during a read or write operation. This option operates equally well with embedded or dedicated servos.

The WD61C40A also includes several features to improve testability of the device:

- All register files contain internal Built-in Self-test (BIST) logic.
- Most microprocessor registers are readable.
- Provides test modes for the large transfer counter, address pointers and major internal logic blocks.
- The I/O pins include the I/O Mapping Test feature for printed circuit board testing.
- The Writeable Control Store RAM is read-writeable by the microprocessor.

## 2.0 ARCHITECTURE

The WD61C40A is divided into four major sections. These sections are the disk control logic, the buffer management control, microprocessor interface and the host port logic.

The Disk Port contains a 64 x 32 writeable control store, the ID field control logic with defect skipping control, a 32 byte data FIFO, and the ECC checking/generation/correction logic.

The host port contains the host control logic and a 32 byte FIFO.

The microprocessor interface contains logic which supports a microprocessor with a multiplexed data/address bus and wait state capabilities. This includes Intel's family of 80196 and 80186 devices.

The buffer interface contains the buffer arbitration control and the DMA address pointers (refresh, host port, disk controller port, ECC correction, microprocessor access).

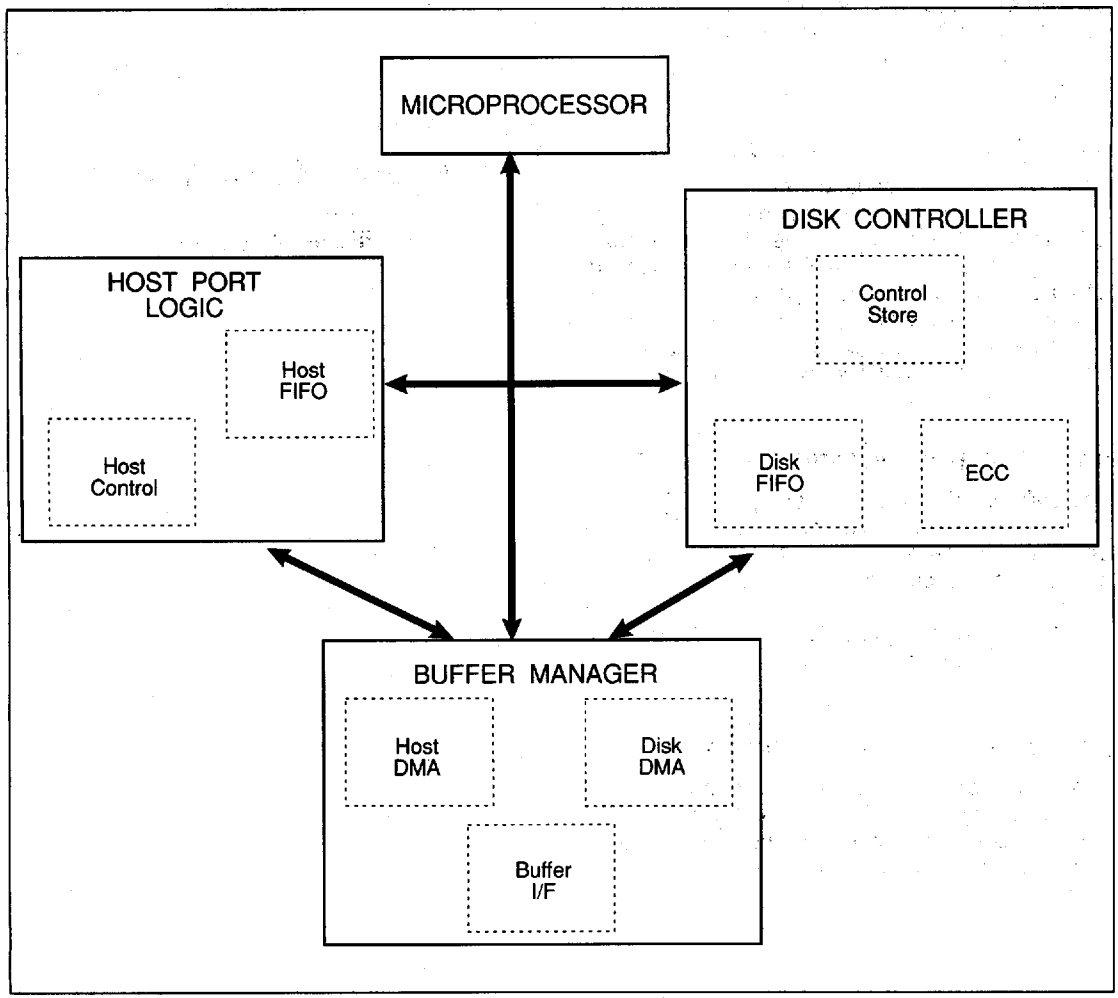


**FIGURE 2-1. BLOCK DIAGRAM OF THE WD61C40A**

# 3.0 INTERFACES

## 3.1 MICROPROCESSOR INTERFACE

The WD61C40A supports 8-bit microprocessors with multiplexed address/data busses. All the internal registers are accessible through this bus. The microprocessor accesses these registers using the following control signals: WEB, REB, ALE, CSB and RDYB. The device must be externally mapped into a 256-byte space. A chip select, CSB, must be presented to this device for any read or write access. The WD61C40A sends a ready signal, RDYB, to the microprocessor whenever an extended read or write strobe is required. This is done when the microprocessor wishes to access the buffer memory.

## 3.2 HOST PORT INTERFACE

The host port is a generic DMA data port. Data transfer speeds are programmable. The data can be transferred in a 16-bit mode. The maximum transfer speed is 10 MTransfers per second. The host port DMA logic is programmable. Both master and slave DMA operations are supported. The polarity of the DREQ and DACK signals are programmable to be active high or low.

## 3.3 DISK PORT INTERFACE

The disk port is constructed around a WD10C01-like architecture. The disk port is controlled by a 64 x 32-bit writeable control store. The disk port now supports a parallel data path. This path can support up to a 10 MByte transfer rate. All of the WD10C01 control signals and most of the general port bits are supported.

## 3.4 BUFFER PORT INTERFACE

The buffer port is designed to support 16-bit DRAM configurations up to 4 MWords. The memory size, parity option and bus timing are all programmable features.

# 4.0 SIGNAL DESCRIPTION

## 4.1 SIGNAL TO PIN LOCATION

Figure 4-1 is a pin diagram of the 132-pin WD61C40A. Table 4-1 lists the pin assignments.

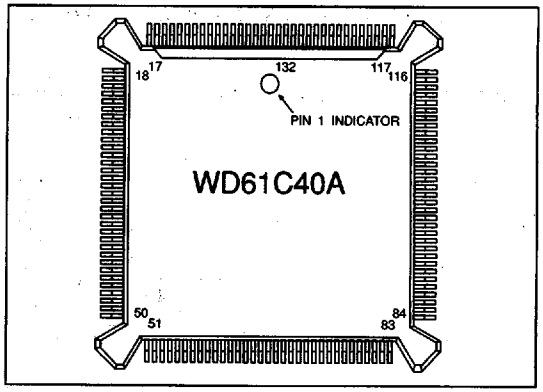


**FIGURE 4-1. 132-PIN PQFP**

## 4.2 DETAILED SIGNAL DESCRIPTION

Table 4-2 provides signal descriptions.

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|---|---|---|---|---|---|---|---|
| 1 | VCC | 34 | BF11 | 67 | RESETB | 100 | GPX0 |
| 2 | N/C | 35 | BF12 | 68 | VCC | 101 | VCC |
| 3 | GND | 36 | GND | 69 | GPY3 | 102 | DATA7 |
| 4 | A10 | 37 | BF13 | 70 | TSTB | 103 | GND |
| 5 | A9 | 38 | BF14 | 71 | N/C | 104 | DATA6 |
| 6 | A8 | 39 | BF15 | 72 | BDPH | 105 | GPX2 |
| 7 | A7 | 40 | BFPH | 73 | BD15 | 106 | DATA5 |
| 8 | A6 | 41 | GND | 74 | BD14 | 107 | GPX3 |
| 9 | GND | 42 | ESP | 75 | BD13 | 108 | DATA4 |
| 10 | A5 | 43 | INT2 | 76 | BD12 | 109 | GND |
| 11 | A4 | 44 | INT | 77 | GND | 110 | DATA3 |
| 12 | A3 | 45 | RDY | 78 | BD11 | 111 | GPX5 |
| 13 | A2 | 46 | ALE | 79 | BD10 | 112 | DATA2 |
| 14 | A1 | 47 | WEB | 80 | BD9 | 113 | DATA1 |
| 15 | A0 | 48 | CSB | 81 | BD8 | 114 | DATA0 |
| 16 | CASB | 49 | REB | 82 | BDPL | 115 | DATAP |
| 17 | GND | 50 | VCC | 83 | GND | 116 | GND |
| 18 | MEMWB | 51 | GND | 84 | BD7 | 117 | RRCLK |
| 19 | RASB | 52 | AD7 | 85 | BD6 | 118 | WRTCLK |
| 20 | BF0 | 53 | AD6 | 86 | BD5 | 119 | GND |
| 21 | BF1 | 54 | AD5 | 87 | BD4 | 120 | AMENA |
| 22 | BF2 | 55 | AD4 | 88 | GND | 121 | RDGATE |
| 23 | GND | 56 | GND | 89 | BD3 | 122 | WRTGATE |
| 24 | BF3 | 57 | AD3 | 90 | BD2 | 123 | SEQOUT |
| 25 | BF4 | 58 | AD2 | 91 | BD1 | 124 | GPX6 |
| 26 | BF5 | 59 | AD1 | 92 | BD0 | 125 | GPX7 |
| 27 | BF6 | 60 | AD0 | 93 | GND | 126 | AMDET |
| 28 | BF7 | 61 | GND | 94 | DRQ | 127 | SMDET |
| 29 | GND | 62 | GPY0 | 95 | DACK | 128 | IDXDET |
| 30 | BFPL | 63 | GPY1 | 96 | PREB | 129 | COMPLT |
| 31 | BF8 | 64 | GPY2 | 97 | PWEB | 130 | DRVFLT |
| 32 | BF9 | 65 | N/C | 98 | GPX4 | 131 | WRAP |
| 33 | BF10 | 66 | X1 | 99 | GPX1 | 132 | N/C |

**TABLE 4-1. WD61C40A PIN ASSIGNMENTS**

| PIN | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *MICROPROCESSOR INTERFACE* |
| 43 | INT2 | O | **Secondary Interrupt Request** This active-high output signal is asserted when any unmasked interrupt is active. |
| 44 | INT | O | **Interrupt Request** This active-high output signal is asserted when any unmasked interrupt is active. |
| 45 | RDYB | O | **Ready** This open-drain output controls the microprocessor's wait logic. (Active low) |
| 46 | ALE | I | **Address Latch Enable** This signal is used to load the address of the desired register. |
| 47 | WEB | I | **Write Enable** This signal is used with the CSB signal to write to the registers. (Active low) |
| 48 | CSB | I | **Chip Select** This signal qualifies REB and WEB signals when the microprocessor is accessing a register. (Active low) |
| 49 | REB | I | **Read Enable** This signal is used with the CSB signal to read the registers. (Active low) |
| 52-55<br>57-60 | AD7-AD0 | I/O | **Microprocessor Data/Address Bus** |

**TABLE 4-2. SIGNAL DESCRIPTION**

| PIN | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *HOST INTERFACE* |
| 72 | BDPH | I/O | **Parity of the Upper DMA Bus**<br>Odd parity for BD15 through BD8. |
| 82 | BDPL | I/O | **Parity of the Lower DMA Bus**<br>Odd parity ofr BD7 through BD0. |
| 81-78<br>76-73 | BD[8:15] | I/O | **Host DMA Bus**<br>Upper 8 bits of host DMA bus. |
| 92-89<br>87-84 | BD[0:7] | I/O | **Host DMA Bus**<br>Lower 8 bits of host DMA bus. |
| 94 | DREQ | I/O | **DMA Request**<br>Programmable DMA request. |
| 95 | DACK | I/O | **DMA Acknowledge**<br>Programmable DMA Acknowledge. |
| 96 | DREB | I/O | **DMA Read Enable** (Active low) |
| 97 | DWEB | I/O | **DMA Write Enable** (Active low) |

**TABLE 4-2. SIGNAL DESCRIPTION (Continued)**

| PIN | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *DISK INTERFACE* |
| 42 | ESP | | **ESPEND**<br>This bit reflects the internal status of the ESPEND bit. ESPEND is the primary control line from the Disk Controller to the buffer manager. |
| 62-64, 69 | GPY[0:3] | I/O | **General Purpose Port**<br>These pins can be configured as a generic input or output pins. |
| 100,99, 105,107, 98, 111, 124, 125 | GPX[0:7] | I/O | **General Purpose Port**<br>These pins can be configured as a generic input or output pins. |
| 114, 113 112, 110 108, 106 104, 102 | DATA[0:7] | I/O | **Disk Drive Parallel Data Bus** |
| 115 | DATAP | I/O | **Disk Drive Parallel Data Bus Parity** |
| 117 | RRCLK | I | **Read Reference Clock**<br>This clock is generated by the Disk Read Channel. All WD61C40A disk control and data signals are synchronized to this clock. |
| 118 | WRTCLK | O | **Write Clock**<br>This signal is the inversion of RRCLK. |
| 120 | AMENA | O | **Address Mark Enable**<br>In write mode, this signal indicates to the write channel that an address mark byte is being sent on the DATA[0:7] lines. In read mode, this signal flags the read channel as to the type of sync bytes to be detected. When RDGATE and WRTGATE are inactive, this signal indicates a search for an ID Address mark. (This signal is not tristated under reset conditions.) |
| 121 | RDGATE | O | **Read Gate**<br>This signal is controlled by the Control Store (This signal is not tristated under reset conditions.) |
| 122 | WRTGATE | I | **Write Gate**<br>This signal is controlled by the Control Store. (This signal is not tristated under reset conditions.) |
| 123 | SEQOUT | O | **Sequence Out**<br>This is a general purpose control signal that is directed by Control Store. |

**TABLE 4-2. SIGNAL DESCRIPTION (Continued)**

| PIN | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *DISK INTERFACE (Continued)* |
| 126 | AMDET | I | **Address Mark Detect**<br>The Read Channel generates this signal when an ID address mark (or optional sync byte) is detected. |
| 127 | SMDET | I | **Sector Mark Detect**<br>This signal is generated by the read/write logic when a sector mark is found. |
| 128 | IDXDET | O | **Index Detect**<br>This signal is generated by the read/write logic when an index mark is detected. |
| 129 | CMPLT | I | **Seek Complete**<br>This is a general purpose flag from the drive electronics. When this signal is active an interrupt can be generated by the WD61C40A. |
| 130 | DRVFLT | I | **Drive Fault**<br>This is a general purpose flag from the drive electronics. This is typically an indication of a drive failure. When this signal is active, an interrupt is generated by the WD61C40A. As an option, the Control Store can respond to this error condition and jump to the error routine. |
| 131 | WRAP | I | **WRAP Check**<br>This pin is used to verify that the REGATE, WRTGATE, and AMENA signals are properly connected to the drive electronics. An interrupt is also generated when an error is detected. |
| | | | *BUFFER PORT INTERFACE* |
| 15-10<br>8-4 | A[0:10] | O | **Buffer Address Pins** |
| 16 | CASB | O | **Primary Column Address Strobe** (Active Low) |
| 18 | MEMWB | O | **Memory Write** (Active Low) |
| 19 | RASB | O | **Row Address Strobe** (Active Low) |
| 20-22,<br>24-28 | BF[0:7] | I/O | **Buffer Data Bus (LSB)** |
| 30 | BFPL | I/O | **Buffer Data Parity Bit (LSB)**, odd parity. |
| 31-35<br>37-39 | BF[8:15] | I/O | **Buffer Data Bus (MSB)** |
| 40 | BFPH | I/O | **Buffer Data Parity (MSB)**, odd parity. |

**TABLE 4-2. SIGNAL DESCRIPTION (Continued)**

| PIN | MNEMONIC | I/O | DESCRIPTION |
|---|---|---|---|
| | | | *MISCELLANEOUS* |
| 66 | X1 | I | **Clock** - maximum 47 MHz. |
| 67 | RESETB | I | **Hard Reset**<br>This active-low input sets the WD61C40A in power-on-reset condition. All the drivers are set into inactive state. (Active low) |
| 70 | TSTB | I | **I/O Test Enable**<br>When active low, the WD61C40A is in I/O Map Test. |
| 1, 101, 68, 50 | VCC | I | **+5V Power Supply** |
| 119, 116, 109, 93, 88,83, 77, 61, 56, 51, 41, 36, 29, 23, 17, 9, 3 | GND | I | **Ground** |

**TABLE 4-2. SIGNAL DESCRIPTION (Continued)**