WD4200/WD4210 Single-Chip N-Channel Microcontrollers

FEATURES

- Low cost
- Powerful instruction set
- 1K x 8 ROM, 64 x 4 RAM
- 23 I/O lines (WD4200)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0 μs instruction time
- Single supply operation (4.5V to 6.3V)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS™ compatible
- Software/hardware compatible with other members of WD4200 family
- Extended temperature range device available (-40°C to +85°C)

GENERAL DESCRIPTION

The WD4200 and WD4210 Single-Chip N-Channel Microcontrollers are members of the Control Oriented Processor family, fabricated using N-channel, silicon gate MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The WD4210 is identical to the WD4200, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented Processor at a low end-product cost.

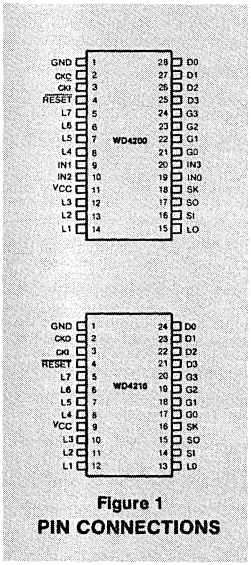


Figure 1
PIN CONNECTIONS

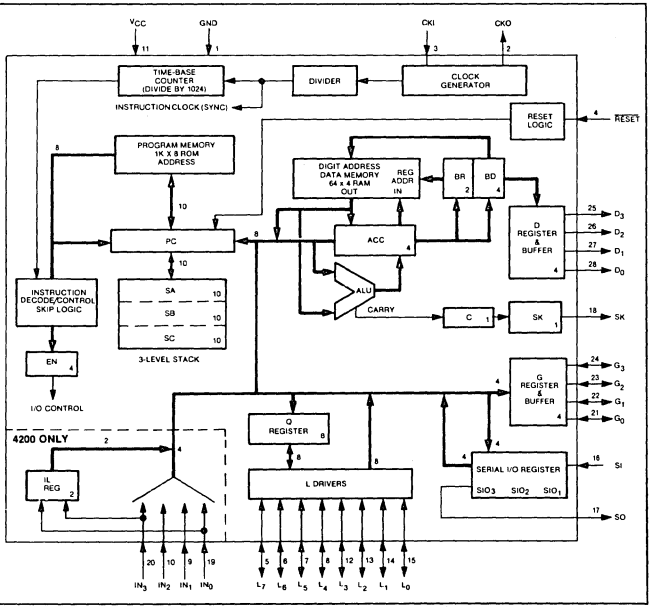


Figure 2 WD4200/4210 BLOCK DIAGRAM

SECTION 4

PIN DESCRIPTION	
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs (WD4200 only)
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
CKI	System oscillator input
CKO	System Oscillator output (or general purpose input or RAM power supply)
$\overline{\text{RESET}}$	System reset input
V_{CC}	Power supply
GND	Ground

FUNCTIONAL DESCRIPTION

A block diagram of the WD4200 is given on page 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

Program Memory

Program Memory consists of a **1,024-byte ROM.** As can be seen by an examination of WD4200/4210 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a **10-bit PC register.** Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the **10-bit subroutine save registers, SA, SB and SC,** providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

Data Memory

Data Memory consists of a **256-bit RAM,** organized as four data registers of 16 4-bit digits. RAM addressing is implemented by a **6-bit B** register whose upper two bits (Br) select one of four data registers and lower 4 bits (Bd) select one of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected **RAM digit (M)** is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

Internal Logic

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input four bits of the 8-bit Q latch data, to input four bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A **4-bit adder** performs the arithmetic and logic functions of the WD4200/4210, storing its results in A. It also outputs a carry bit to the 1-bit **C register,** most often employed to indicate arithmetic overflow. The C register, in conjunction with XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time (see XAS instruction and EN register description below).

Four **general-purpose inputs,** IN_3-IN_0, are provided; IN_1, IN_2 and IN_3 may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS™ applications.

The **D register** provides four general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to four general-purpose bidirectional I/O ports. G_0 may be mask-programmed as an output for MICROBUS™ applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS™ option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The **eight L drivers,** when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS™ option allows L I/O port data to be latched into the Q register. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with

Q data being outputted to the Sa-Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register (see EN register description below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/serial-out shift registers. For example of additional parallel output capacity, see Application No. 2.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selectes the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of C upon execution of XAS and remains the same until the execution of another XAS instruction. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time (see 4 below). The SK output becomes a logic-controlled clock, providing a SYNC signal each instruction time. It will start outputting a SYNC pulse upon the execution of an XAS instruction with C = 1, stopping upon the execution of a subsequent XAS with C = 0.
2. With EN_1 set the IN_1 input is enabled as an interrupt input. Immediately following an interrupt, EN_1 is reset to disable further interrupts.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state. If the MICROBUS™ option is being used, EN_2 does not affect the L drivers.
4. EN3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output: data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides a summary of the modes associated with EN_3 and EN_0.

Interrupt

The following features are associated with the IN_1 interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1)onto the stack, pushing in turn the contents of the other subroutine-save register to the next lower level (PC+1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met:
   1) EN_1 has been set.
   2) A low-going pulse ("1" to "0") of at least two instruction cycles wide occurs on the IN_1 input.
   3) A currently executing instruction has been completed.

ENABLE REGISTER MODES — BITS EN_3 AND EN_0

EN3	EN0	SIO	SI	SO	SK AFTER XAS
0	0	Shift Register	Input to Shift Register	0	If C = 1, SK = SYNC If C = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If C = 1, SK = SYNC If C = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If C = 1, SK = 1 If C = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If C = 1, SK = 1 If C = 0, SK = 0

4) All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon the execution of a subsequent RET instruction. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the *end* of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. *At this time*, the skip logic is enabled and skips this instruction because of the previous ASC carry. Since, as explained above, it is the RET instruction which enables the previously saved status of the skip logic, subroutines should not be nested within the interrupt servicing routine since their RET instruction will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.

e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

MICROBUS™ Interface

The WD4200 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN_1, IN_2, and IN_3 general purpose inputs become MICROBUS™ compatible read-strobe, chip-select, and write-strobe lines, respectively. **IN_1 becomes $\overline{RD}$** — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. **IN_3 becomes $\overline{CS}$** — a logic "0" on this line selects the WD4200 as the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several periopheral components. **IN_3 becomes $\overline{WR}$** — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the WD4200. **G_0 becomes INTR** a "ready" output, reset by a write pulse from the μP on the WR line, providing the "hand-shaking" capability necessary for asynchronous data transfer between the host CPU and the WD4200.

This option has been designed for compatibility with National's MICROBUS™ — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS™, National Publication.) The functioning and timing relationships between the WD4200 signal lines affected by this option are as specified for the MICROBUS™ interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figures 11 and 12). Connection of the WD4200 to the MICROBUS™ is shown in MICROBUS™ Option interconnect illustration.

Initialization

The Reset Logic, internal to the WD4200/4210 will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μs. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the $\overline{RESET}$ pin as shown below. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least two instruction cycle times.

Upon initialization, the **PC register is cleared** to 0 (ROM address 0) and the **A, B, C, D, EN, and G registers are cleared.** The **SK output is enabled as a SYNC output,** providing a pulse each instruction cycle time. *Data Memory (RAM) must be cleared by the user's program.* The first instruction at address 0 must be a CLRA.

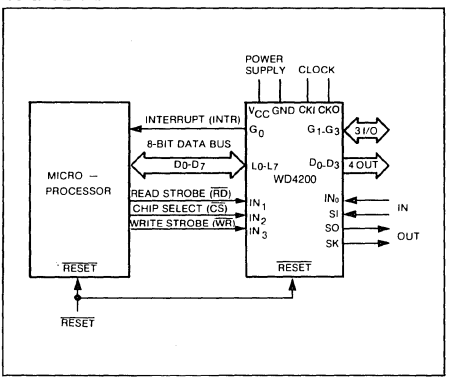


Figure 3 MICROBUS™ OPTION INTERCONNECT

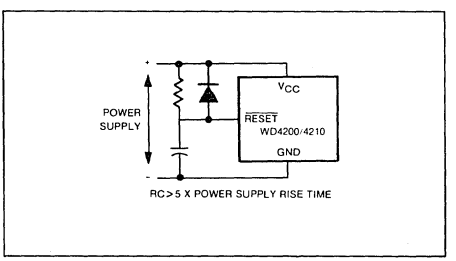


Figure 4 POWER-UP CLEAR CIRCUITS

Oscillator

There are four basic clock oscillator configurations available as shown below.

a. **Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).

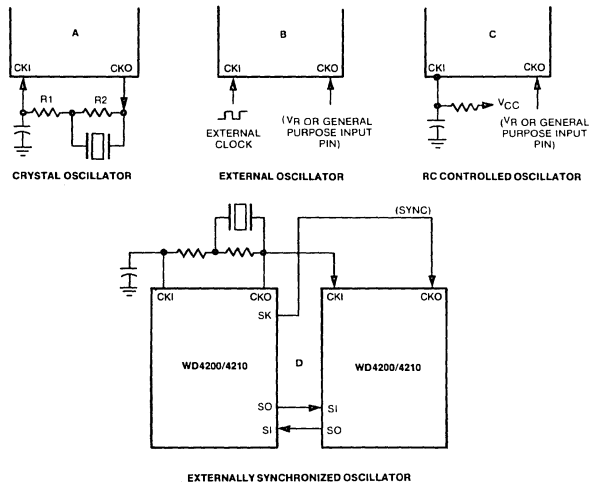
b. **External Oscillator.** CKI is configured as a TTL compatible input accepting an external clock signal. The external frequency is divided by 16 (optional by 8 or 4) to give the instruction cycle time. CKO is now available to be used as the RAM power supply (V_R) or as a general purpose input.

c. **RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.

d. **Externally Synchronized Oscillator.** Intended for use in multi-WD systems, CKO is programmed to function as an input connected to the SK output of another WD4200/4210 with CKI connected as shown. In this configuration, the SK output connected to CKO must provide a SYNC (instruction cycle) signal to CKO, thereby allowing synchronous data transfer between the WDs using only the SI and SO serial I/O pins in conjunction with the XAS instruction. Note that on power-up SK is automatically enabled as a SYNC output (see Functional Description, Initialization, above).

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an **output to the crystal network.** As an option CKO can be a **general purpose input,** read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a **RAM power supply** pin (V_R), allowing its connection to be a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the WD4200/4210 system timing configuration does not require use of the CKO pin.



Crystal Oscillator

Crystal Value	Component Values		
	R1	R2	C
4 MHz	1K	1M	27 pF
3.58 MHz	1K	1M	27 pF
2.09 MHz	1K	1M	56 pF

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time in μs
12	100	5± 20%
6.8	220	5.3 ± 23%
8.2	300	8 ± 29%
22	100	8.6 ± 16%

Figure 5 WD4200/4210 OSCILLATOR

I/O Options

WD4200/4210 outputs have the following optional configurations, illustrated below.

a. **Standard.** An enhancement-mode device to ground in conjunction with a depletion-mode device to V_{CC} compatible with TLL and CMOS input requirements.

b. **Open-Drain.** An enhancement-mode device to ground only, allowing external pull-up as required by the user's application.

c. **Push-Pull.** An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.

d. **LED Direct Drive.** An enhancement-mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.

e. **TRI-STATE® Push-Pull.** An enhancement-mode device to ground and V_{CC} intended to meet the requirements associated with the MICROBUS™ option. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

WD4200/4210 inputs have the following optional configurations:

f. An on-chip depletion **load device to V_{CC}.**

g. **A Hi-Z input** which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given on figure 7 for each of these devices to allow the designer to effectively use these I/O configurations in designing a WD4200/4210 system.

The SO, SK outputs can be configured as shown in A, B, or C. The D and G outputs can be configured as shown in A or B. Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as A, B, D, or E.

An important point to remember if using configuration A or D with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current.

WD4210

If the WD4200 is bonded as a 24-pin device, it becomes the WD4210, illustrated in figure 1, WD4200/4210 Connection Diagrams. Note that the WD4210 does not contain the four general purpose IN inputs (IN_3-IN_0). Use of this option precludes, of course use of the IN options, interrupt feature, and the MICROBUS™ option which uses IN_1-IN_3. All other options are available for the WD4210.

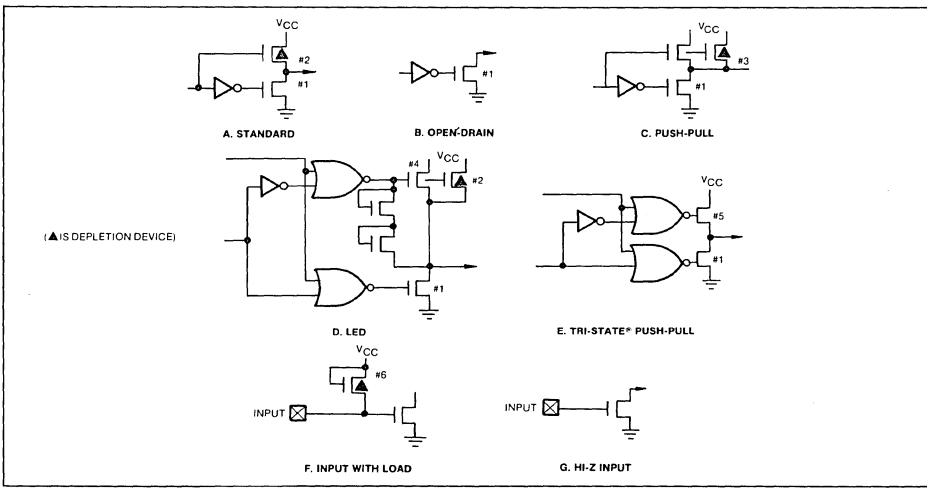
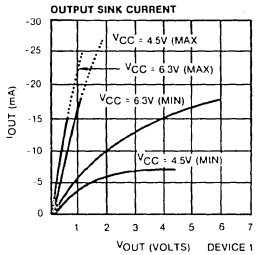
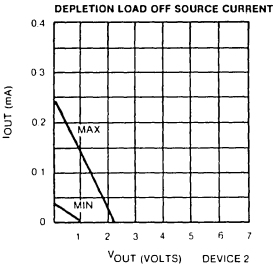
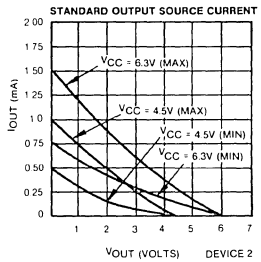
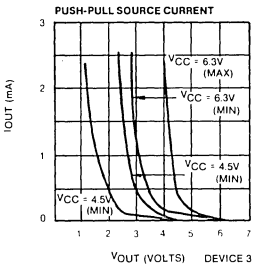


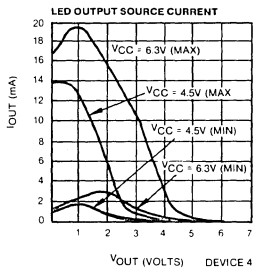
Figure 6 OUTPUT CONFIGURATIONS

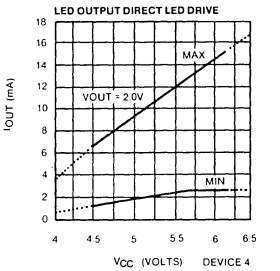


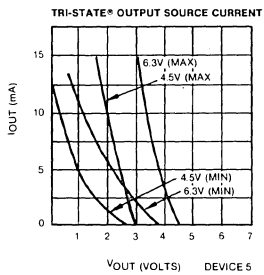












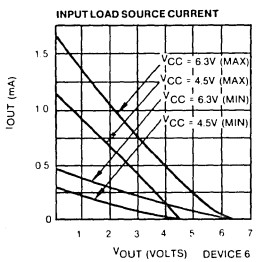


Figure 7 OUTPUT CHARACTERISTICS

WD4200/4210 INSTRUCTION SET

Table 1 is a symbol table providing internal architecture, instruction operand, and operational symbols used in the instruction set table.

Table 2 provides the mnemonic, operand, machine code, data flow, skip conditions, and description associated with each instruction in the WD4200/4210 instruction set.

TABLE 1. WD4200/4210 INSTRUCTION SET TABLE SYMBOLS

Symbol	Definition	Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS		**INSTRUCTION OPERAND SYMBOLS**	
A	4-bit Accumulator	d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
B	6-bit RAM Address Register	r	2-bit Operand Field, 0-3 binary (RAM Register Select)
Br	Upper 2 bits of B (register address)	a	10-bit Operand Field, 0-1023 binary (ROM Address)
Bd	Lower 4 bits of B (digit address)	y	4-bit Operand Field, 0-15 binary (Immediate Data)
C	1-bit Carry Register	RAM(s)	Content and RAM location addressed by s
D	4-bit Data Output Port	ROM(t)	Content and ROM location addressed by t
EN	4-bit Enable Register		
G	4-bit Register to latch data for G I/O Port	**OPERATIONAL SYMBOLS**	
IL	Two 1-bit Latches associated with the IN_3 or IN0 Inputs	+	Plus
IN	4-bit Input Port	-	Minus
L	8-bit TRI-STATE® I/O Port	→	Replaces
M	4-bit contents of RAM Memory Pointed to by B Register	↔	Is exchanged with
PC	10-bit ROM Address Register (program counter)	=	Is equal to
Q	8-bit Register to latch data for L I/O Port	$\overline{A}$	The ones complement of A
SA	10-bit Subroutine Save Register A	⊕	Exclusive-OR
SB	10-bit Subroutine Save Register B	:	Range of values
SC	10-bit Subroutine Save Register C		
SIO	4-bit Shift Register and Counter		
SK	Logic-Controlled Clock Output		

TABLE 2. WD4200/4210 INSTRUCTION SET TABLE (Note 1)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0 0 1 1 0 0 0 0	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0 0 1 1 0 0 0 1	A + RAM(B) → A	None	Add A to RAM
ADT		4A	0 1 0 0 1 0 1 0	A + 10_{10} → A	None	Add Ten to A
AISC	y	5-	0 1 0 1 | y |	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CASC		10	0 0 0 1 0 0 0 0	$\overline{A}$ + RAM(B) + C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	0 0 0 0 0 0 0 0	0 → A	None	Clear A
COMP		40	0 1 0 0 0 0 0 0	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	0 1 0 0 0 1 0 0	None	None	No Operation
RC		32	0 0 1 1 0 0 1 0	"0" → C	None	Reset C
SC		22	0 0 1 0 0 0 1 0	"1" → C	None	Set C
XOR		02	0 0 0 0 0 0 1 0	A ⊕ RAM(B) → A	None	Exclusive-OR A with RAM

SECTION 4

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1 1 1 1 | 1 1 1 1	ROM (PC9:8, A, M) → $PC_{7:0}$	None	Jump Indirect (Note 3)
JMP	a	6_	0 1 1 0 | 0 0 $a_{9:8}$	a → PC	None	Jump
		--	$a_{7:0}$			
JP	a	--	1 | $a_{6:0}$	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			(Pages 2, 3 only) or			
		--	1 1 | $a_{5:0}$	a → $PC_{5:0}$		
			(all other pages)			
JSRP	a	--	1 0 | $a_{5:0}$	PC + 1 → SA → SB → SC 0010 → $PC_{9:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6_	0 1 1 0 | 1 0 $a_{9:8}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
		--	$a_{7:0}$			
RET		48	0 1 0 0 | 1 0 0 0	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0 1 0 0 | 1 0 0 1	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	0 0 1 1 | 0 0 1 1	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	0 0 1 1 | 1 1 0 0	RAM(B) → $Q_{3:0}$		
CQMA		33	0 1 1 0 | 0 1 1 1	$Q_{7:4}$ → RAM(B)	None	Copy Q to RAM, A
		2C	0 0 1 0 | 1 1 0 0	$Q_{3:0}$ → A		
LD	r	_5	0 0 | r | 0 1 0 1	RAM(B) → A BR[9] r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r, d	23	0 0 1 0 | 0 0 1 1	RAM(r,d) → A	None	Load A with RAM pointed to directly by r, d
		--	0 0 | r | d			
LQID		BF	1 0 1 1 | 1 1 1 1	ROM($PC_{9:8}$, A, M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	0 1 0 0 | 1 1 0 0	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	0 1 0 0 | 0 1 0 1	0 → $RAM(B)_1$		
	2	42	0 1 0 0 | 0 0 1 0	0 → $RAM(B)_2$		
	3	43	0 1 0 0 | 0 0 1 1	0 → $RAM(B)_3$		
SMB	0	4D	0 1 0 0 | 1 1 0 1	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	0 1 0 0 | 0 1 1 1	1 → $RAM(B)_1$		
	2	46	0 1 0 0 | 0 1 1 0	1 → $RAM(B)_2$		
	3	4B	0 1 0 0 | 1 0 1 1	1 → $RAM(B)_3$		

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7_	0 1 1 1 | y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	_6	0 0 | r | 0 1 1 0	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive OR Br with r
XAD	r, d	23	0 0 1 0 | 0 0 1 1	RAM(r,d) ↔ A	None	Exchange A with RAM pointed to directly by r, d
		- -	1 0 | r | d			
XDS	r	_7	0 0 | r | 0 1 1 1	RAM(B) ↔ A Bc - 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR br with r
XIS	r	_4	0 0 | r | 0 1 0 0	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0 1 0 1 | 0 0 0 0	A → Bd	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	BD → A	None	Copy Bd to A
LBI	r, d	- -	0 0 | r | (d (d = 0, 9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r, d (Note 6)
			or			
		33	0 0 1 1 | 0 0 1 1			
		- -	1 0 | r | d (any d)			
LEI	y	33	0 0 1 1 | 0 0 1 1	y → EN	None	Load EN Immediate (Note 7)
		6_	0 1 1 0 | y			
XABR		12	0 0 0 1 | 0 0 1 0	A ↔ Br (0, 0 → A_3, A_2)	None	Exchange A with Br
TEST INSTRUCTIONS						
SKC		20	0 0 1 0 | 0 0 0 0		C = "1"	Skip if C is True
SKE		21	0 0 1 0 | 0 0 0 1		A = (RAM(B)	Skip if A Equals RAM
SKGZ		33	0 0 1 1 | 0 0 1 1		$G_{3:0}$ =0	Skip if G is Zero (all 4 bits)
		21	0 0 1 0 | 0 0 0 1			
SKGBZ		33	0 0 1 1 | 0 0 1 1	1st byte		Skip if G Bit is Zero
	0	01	0 0 0 0 | 0 0 0 1	2nd byte	G_0 = 0	
	1	11	0 0 0 1 | 0 0 0 1		G_1 = 0	
	2	03	0 0 0 0 | 0 0 1 1		G_2 = 0	
	3	13	0 0 0 1 | 0 0 1 1		G_3 = 0	
SKMBZ	0	01	0 0 0 0 | 0 0 0 1		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0 0 0 1 | 0 0 0 1		$RAM(B)_1$ = 0	
	2	03	0 0 0 0 | 0 0 1 1		$RAM(B)_2$ = 0	
	3	13	0 0 0 1 | 0 0 1 1		$RAM(B)_3$ =0	
SKT		41	0 1 0 0 | 0 0 0 1		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0 0 1 1 0 0 1 1	G → A	None	Input G ports to A
		2A	0 0 1 0 1 0 1 0			
ININ		33	0 0 1 1 0 0 1 1	IN → A	None	Input IN inputs to A
		28	0 0 1 0 1 0 0 0			(Note 2)
INIL		33	0 0 1 1 0 0 1 1	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Notes 2 and 3)
		29	0 0 1 0 1 0 0 1			
INL		33	0 0 1 1 0 0 1 1	$L_{7:4}$ → RAM(B)	None	Input L Ports to RAM, A
		2E	0 0 1 0 1 1 1 0	$L_{3:0}$ → A		
OBD		33	0 0 1 1 0 0 1 1	Bd → D	None	Output Bd to D Outputs
		3E	0 0 1 1 1 1 1 0			
OGI	y	33	0 0 1 1 0 0 1 1	y → G	None	Output to G Ports Immediate
		5-	0 1 0 1 | y			
OMG		33	0 1 1 0 0 1 1 1	RAM(B) → G	None	Output RAM to G Ports
		3A	0 0 1 1 1 0 1 0			
XAS		4F	0 1 0 0 1 1 1 1	A ↔ SIO, C → SK	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined) Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ and INIL instructions are not available on the 24-pin WD4210 since this device does not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of page 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary view of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal B (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 5 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection of deselection of a particular function associated with each bit (see Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing WD4200/4210 programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output, providing a logic controlled clock if SIO is selected as a shift register or C → SK if SIO is selected as a binary counter. (See Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data system.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 10-bit word, $PC_{9:8}$, A, M. PC_9 and PC_8 are not affected by this instruction.

Note that JID requires two instruction cycles.

INIL Instruction

INIL (Input IL Latches to A) inputs two latches, IL_3 and IL_0 (see figure 8) and CKO into A. The IL_3 and IL_0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN_3 and IN_0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A_2. If CKO has not been so programmed, a "1" will be placed in A_2. A "0" is always placed in A_1 upon the execution of an INIL. The general purpose inputs IN_3—IN_0 are input to A upon the execution of an ININ instruction (see table 2, ININ Instruction). INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word PC_9, PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of PC as follows: A → $PC_{7:4}$, RAM(B) → $PC_{3:0}$, leaving PC_9 and PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the contents of SB are placed in SC (SB → SC). Note that LQID takes two instruction cycle times to execute.

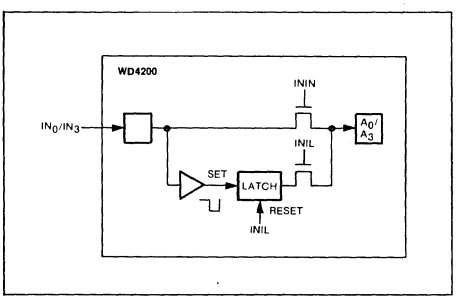


Figure 8 **INIL HARDWARE IMPLEMENTATION**

SKT Instruction

The SKT (Skip on Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the WD4200/4210 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency ÷ 16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

Instruction Set Notes

a. The first word of a WD4200/4210 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed.

c. The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP location in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of pages 2, 7, 11, or 15 will access data in the next group of four pages.

OPTION LIST

The WD4200/4210 mask-programmable options are assigned numbers which correspond with the WD4200 pins.

TABLE 3 is a list of WD4200 options. When specifying a WD4210 chip, Options 9, 10, 19, 20, and 29 must all be set to zero. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

TABLE 3 WD4200 MASK OPTIONS

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal
- = 1: pin is RAM power supply (V_R input)
- = 2: general purpose input, load device to V_{CC}
- = 3: multi-COP SYNC input
- = 4: general purpose input, Hi-Z input

Option 3: CKI Input
- = 0: crystal input divided by 16
- = 1: crystal input divided by 8
- = 2: TTL external clock input divided by 16
- = 3: TTL external clock input divided by 8
- = 4: single-pin RC controlled oscillator

Option 4: $\overline{\text{RESET}}$ Pin
- = 0: load devices to V_{CC}
- = 1: Hi-Z input

Option 5: L_7 Driver
- = 0: Standard output (Figure 6A)
- = 1: Open-Drain output (Figure 6B)
- = 2: LED direct drive output (Figure 6D)
- = 3: TRI-STATE®push-pull output (Figure 6E)

Option 6: L_6 Driver
Same as Option 5

Option 7: L_5 Driver
Same as Option 5

Option 8: L_4 Driver
Same as Option 5

Option 9: IN_1 Input
- = 0: load device to V_{CC} (Figure 6F)
- = 1: Hi-Z input

Option 10: IN_2 Input
Same as Option 9

Option 11 = 0: V_{CC} Pin — no options available

Option 12: L_3 Driver
Same as Option 5

Option 13: L_2 Driver
Same as Option 5

Option 14: L_1 Driver
Same as Option 5

Option 15: L_0 Driver
Same as Option 5

Option 16: SI Input
Same as Option 9

Option 17: SO Driver
- = 0: Standard output (Figure 6A)
- = 1: Open-Drain output (Figure 6B)
- = 2: Push-Pull output (Figure 6C)

Option 18: SK Driver
Same as Option 17

Option 19: IN_0 Input
Same as Option 9

Option 20: IN_3 Input
Same as Option 9

Option 21: G_0 I/O Port
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 22: G_1 I/O Port
Same as Option 21

Option 23: G_2 I/O Port
Same as Option 21

Option 24: G_3 I/O Port
Same as Option 21

Option 25: D_3 Output
- = 0: Standard output (A)
- = 1: Open-Drain output (B)

Option 26: D_2 Output
Same as Option 25

Option 27: D_1 Output
Same as Option 25

Option 28: D_0 Output
Same as Option 25

Option 29: COP Function
- = 0: normal operation
- = 1: MICROBUS™ option

Option 30: COP Bonding
- = 0: WD4200 (28-pin device)
- = 1: WD4210 (24-pin device)

TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed WD4200. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

APPLICATION NO. 1: WD4200 General Controller

The diagram below shows an interconnect diagram for a WD4200 used as a general controller. Operation of the system is as follows:

1. The L_7-L_0 outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.
2. The D_3-D_0 outputs are buffered by transistors to drive the digits of the multiplexed display and to scan the columns of the 4x4 keyboard matrix rows.
3. The IN_3-IN_0 inputs are used to input the four drives of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
4. CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single pin RC network. CKO is therefore available for use as a VR RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down.
5. SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK may be used as general purpose outputs.
6. The four bidirectional G I/O ports (G_3-G_0) are available for use as required by the user's application.

APPLICATION NO. 2

Provides an interconnect diagram for a versatile application of the WD4200 as a keyboard/display interface to a microprocessor (μP). Generally, operation of the WD4200 in this configuration is as follows:

1. The MICROBUS™ option has been selected.
2. System timing is provided by an external crystal. The time base for the real-time (counter and clock) modes is provided by the internal time-base counter, tested by the SKT instruction.
3. The SIO register is used as a serial-in/serial-out shift register. In this configuration, however, SI is shifted into SIO to be tested as one of the four row lines tied to the keyboard matrix. SO is used to output display segment data (loaded into SIO with an XAS instruction) to the cascaded 74C164s (8-bit parallel out serial shift registers). SK functions as a logic-controlled clock, sending a SYNC signal to clock serial data into the 74C164s.
4. The 16 bits of data shifted into the 74C164s are buffered through the DS8867s (8-segment LED drivers) to the 16 segments of the alpha-numeric LED displays.
5. The D_0-D_1 outputs are decoded by the DS8664 (14-digit decoder/driver) and used to select one of the 14 digits of the multiplexed display as well as to scan the 13 columns of the keyboard matrix and the strap switch scan line (D14).

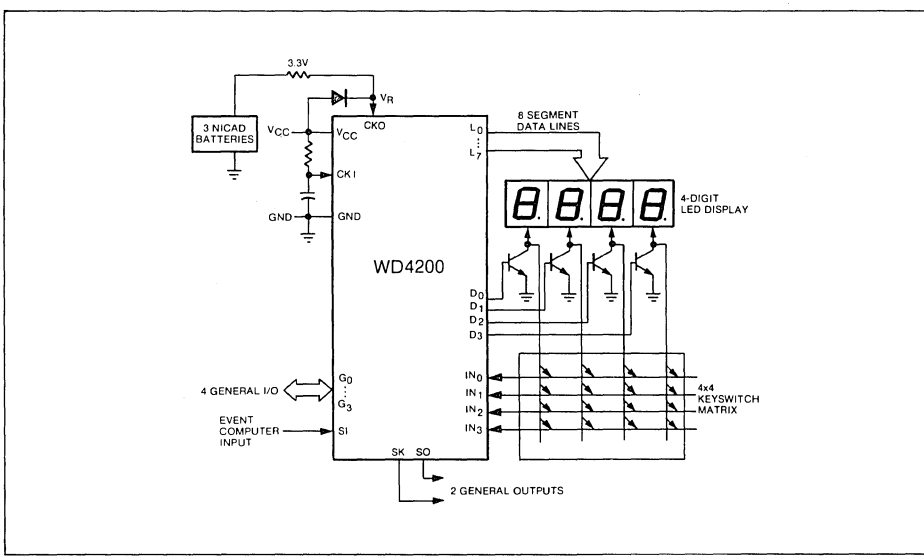
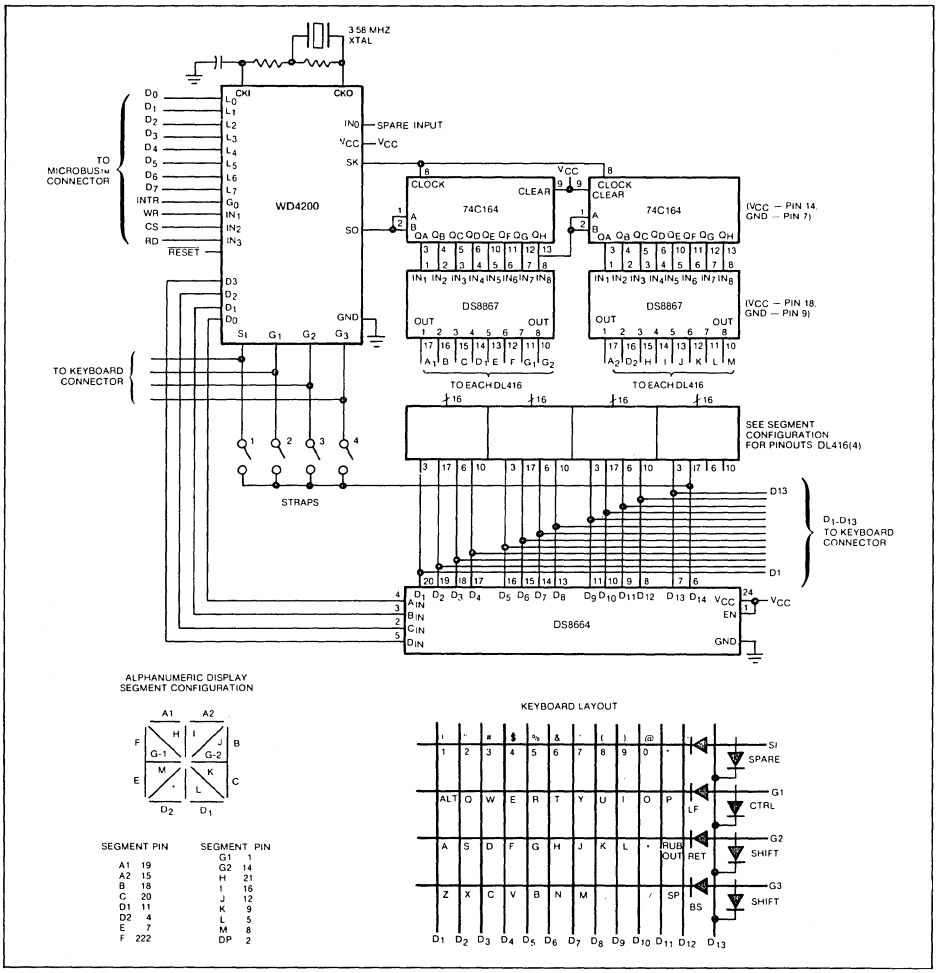


Figure 9 WD4200 KEYBOARD/DISPLAY INTERFACE

6. The G_1-G lines together with SI are connected to the four rows of the keyboard matrix and the four strap switch lines to input key or strap switch data to the WD4200. The strap switches can be used to select one of several of the system modes listed below.
7. The L_0-L_7 TRI-STATE® bidirectional I/O ports are connected to the microprocessor data bus to allow for input or output of data to and from the microprocessor and the WD4200.
8. The various operations which can be performed by the system include the following "handshaking" and WD4200 "stand-alone" modes:

a. keyboard to μP (7-bit ASCII)
b. keyboard to WD4200 buffer to μP (7-bit ASCII)
c. μP to display
d. display to μP
e. μP to clock
f. clock to μP
g. μP to timer
h. timer to μP
i. keyboard to display
j. clock to display
k. timer to display



SEGMENT PIN

A1	19
A2	15
B	18
C	20
D1	11
D2	4
E	7
F	222
G1	1
G2	14
H	21
I	16
J	12
K	9
L	5
M	8
DP	2

Figure 10 WD4200 KEYBOARD/DISPLAY INTERFACE

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND −0.5V to +7V
Ambient Operating Temperature (Note 1)
0°C to +70°C
Ambient Storage Temperature −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) 300°C
Power Dissipation 0.75 Watt at 25°C
0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

TABLE 4

DC ELECTRICAL CHARACTERISTICS

0°C≤TA≤+70°C, 4.5V≤VCC≤6.3V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	V_{CC} = 5V, T_A = 25°C (all inputs and outputs open)		30	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
TTL Input	V_{CC} = 5V ± 5%			
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.8	V
Schmitt Trigger Input				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})			0.6	V
$\overline{RESET}$ Input Levels				
Logic High		0.7 V_{CC}		V
Logic Low			0.6	V
$\overline{RESET}$ Hysteresis		1.0		V
SO Input Level (Test Mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels				
Standard Output				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = 100 μA)	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6 mA		0.4	V
CMOS Operation				
Logic High (V_{OH})	I_{OH} = 10μA	V_{CC}−1		V
Logic Low (V_{OL})	I_{OL} = −10μA		0.2	V
Output Current Levels				
LED Direct Drive Output	V_{CC} = 6V			
Logic High (I_{OH})	V_{OH} = 2.0V	2.5	14	mA
TRI-STATE® Output Leakage Current		−10	+10	μA
CKO Output				
VR Power Saving Option	V_R = 3.3V			
Power Requirements			3	mA

SECTION 4

TABLE 5

AC Electrical Characteristics
$0°C \leq TA \leq +70°C, 4.5V \leq V_{CC} \leq 6.3V$ unless otherwise stated.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Instruction Cycle Time —t_C	figure 13a	4	10	μs
CKI Using Crystal (figure 5A)				
Input Frequency — f_1	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)	figure 13b	30	55	%
CKI Using External Clock (figure 5B)				
Input Frequency	÷16 mode	1.6	4	MHz
	÷ 8 mode	0.8	2	MHz
Duty Cycle (Note 2)		30	60	%
Rise Time	f_1 = 4 MHz		60	ns
Fall Time	f_1 = 4 MHz		40	ns
CKI Using RC (figure 5C)				
Frequency	R = 15K ± 5%, C = 100 pF ± 10%	0.5	1.0	MHz
Instruction Cycle Time		4	8	μs
CKO as SYNC Input (figure 5D)				
t_{SYNO}	figure 13b	50		ns
Inputs (figure 13a):				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		1.7		μs
t_{HOLD}		100		ns
SI				
t_{SETUP}		0.3		μs
t_{HOLD}		100		ns
Outputs:				
COP to CMOS Propagation Delay	$4.5V \leq V_{CC} \leq 6.3V$, C_L = 50 pF, $V_{OH} = 0.7\ V_{CC}$, $V_{OL} = 0.3\ V_{CC}$			
SK as a Logic-Controlled Clock				
t_{PD1}			1.1	μs
t_{PD0}			0.3	μs
SO, SK as a Data Output				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
t_{PD1}	V_{OH} = 2V		0.7	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.6	μs
t_{PD0}			0.6	μs
L_7-L_0 (Standard)				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
L_7-L_0 (LED Direct Drive)				
t_{PD1}	V_{OH} = 2V		2.4	μs
t_{PD0}			0.4	μs
COP to TTL Propagation Delay	fanout = 1 Standard TTL Load V_{CC} = 5V ± 5%, C_L = 50 pF, V_{OH} = 2.4V, V_{OL} = 0.4V			
SK as a Logic-Controlled Clock				
t_{PD1}			0.8	μs
t_{PD0}			0.8	μs
SK as a Data Output, SO				
t_{PD1}			1.0	μs
t_{PD0}			1.0	μs

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Outputs (continued):				
D_3-D_0, G_3-G_0				
t_{PD1}			1.3	µs
t_{PD0}			1.3	µs
L_7-L_0				
t_{PD1}			1.4	µs
t_{PD0}			0.4	µs
L_7-L_0 (Push-Pull)				
t_{PD1}			0.4	µs
t_{PD0}			0.3	µs
CKO (figure 13C)				
t_{PD1}			0.2	µs
t_{PD0}			0.2	µs
MICROBUS™ Timing	CL = 50 pF, V_{CC} = 5V ± 5%			
Read Operation (figure 11)				
Chip Select Stable Before $\overline{RD}$ - t_{CSR}		50		ns
Chip Select Hold Time for $\overline{RD}$ - t_{RCS}		5		ns
$\overline{RD}$ Pulse Width - t_{RR}		300		ns
Data Delay from $\overline{RD}$ - $t_{\overline{RD}}$			250	ns
$\overline{RD}$ to Data Floating - t_{DF}			200	ns
Write Operation (figure 12)				
Chip Select Stable Before $\overline{WR}$ - t_{CSW}		20		ns
Chip Select Hold Time for $\overline{WR}$ - t_{WCS}		20		ns
$\overline{WR}$ Pulse Width — t_{WW}		300		ns
Data Set-Up Time for $\overline{WR}$ - t_{DW}		200		ns
Data Hold Time for $\overline{WR}$ - t_{WD}		40		ns
INTR Transition Time from $\overline{WR}$ - t_{WI}			700	ns

Note 1: An extended temperature range WD4200/4210 is available which will operate within an ambient temperature range of -40°C to +85°C.
Note 2: Duty Cycle = $t_{W1}/(t_{W1} + t_{W0})$.
Note 3: See figure 7 for additional I/O characteristics.

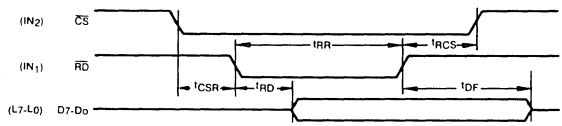


Figure 11 MICROBUS™ READ OPERATION TIMING

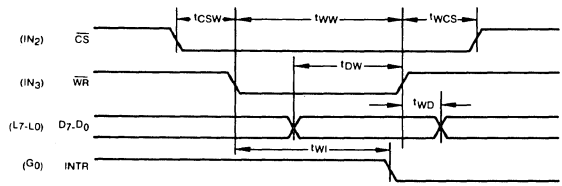


Figure 12 MICROBUS™ WRITE OPERATION TIMING

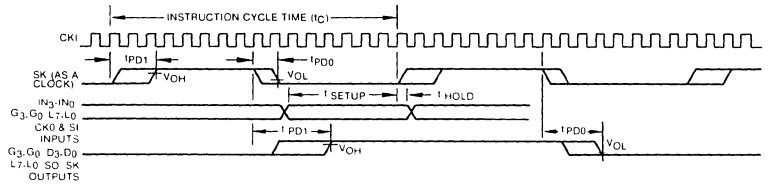


Figure 13A **INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL ÷ 16 MODE)**

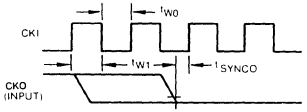


Figure 13B **SYNCHRONIZATION**

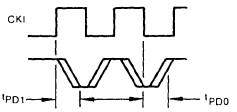
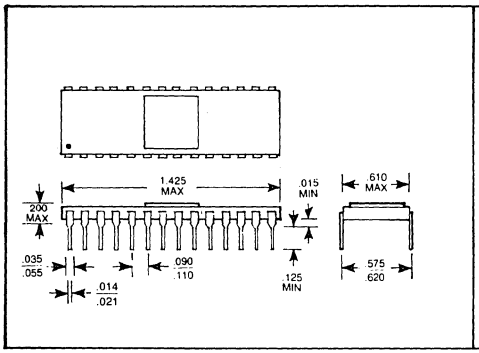
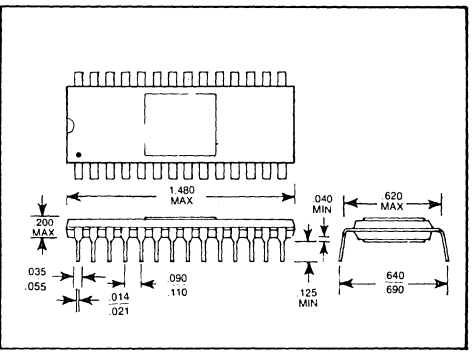


Figure 13C **CKO OUTPUT TIMING**

Figure 13 TIMING



WD4200E CERAMIC PACKAGE



WD4200F PLASTIC PACKAGE

SECTION 4

WESTERN DIGITAL CORPORATION
3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139