WESTERN DIGITAL
CORPORATION

WD 2123 DEUCE
DUAL ENHANCED UNIVERSAL COMMUNICATIONS ELEMENT

MARCH, 1981

FEATURES

- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARTS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
- SELECTABLE 5 TO 8 BIT CHARACTERS
- 1X, 16X, 64X CLOCK RATES
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, OR 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- ODD OR EVEN PARITY GENERATE AND DETECTION
- OVERRUN AND FRAMING DETECTION
- DOUBLE BUFFERING OF DATA
- TTL COMPATIBLE INPUTS AND OUTPUTS
- COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES
- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES

INTRODUCTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.

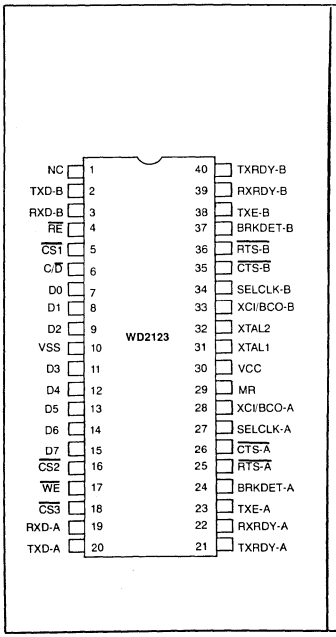


Figure 1 WD2123 PINOUT DIAGRAM

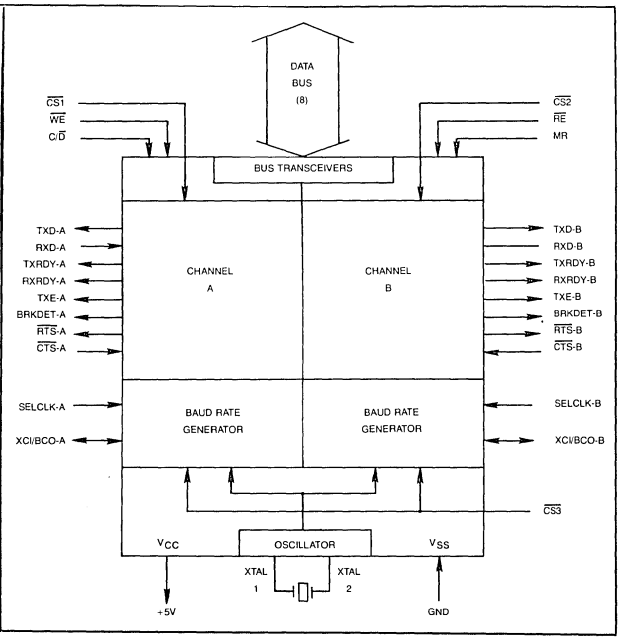


Figure 2 WD2123 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
10	GROUND	VSS	Ground
30	POWER SUPPLY	VCC	+5VDC power supply input.
7 8 9 11 12 13 14 15	DATA BUS	D0 D1 D2 D3 D4 D5 D6 D7	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
5	CHIP SELECT ONE	$\overline{CS1}$	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	CHIP SELECT TWO	$\overline{CS2}$	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	CHIP SELECT THREE	$\overline{CS3}$	V_{IL} on this input select the Baud Rate registers for programming.
6	CONTROL or DATA SELECT	C/$\overline{D}$	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	READ ENABLE	$\overline{RE}$	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	WRITE ENABLE	$\overline{WE}$	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MASTER RESET	MR	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	CRYSTAL OSCILLATOR INPUT	XTAL1	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	CRYSTAL OSCILLATOR OUTPUT	XTAL2	This is the output side of the on-chip oscillator.
27	SELECT CLOCK (Channel A)	SELCLK-A	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELECT CLOCK (Channel B)	SELCLK-B	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel A)	XCI/BCO-A	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	XCI/BCO-B	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	CLEAR-TO-SEND (Channel A)	$\overline{CTS\text{-}A}$	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.
35	CLEAR-TO-SEND (Channel B)	$\overline{CTS\text{-}B}$	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	TRANSMIT DATA (Channel A)	TXD-A	This is the Serial Data Output from Channel A.
2	TRANSMIT DATA (Channel B)	TXD-B	This is the Serial Data Output from Channel B.
19	RECEIVE DATA (Channel A)	RXD-A	This is the Serial Data Input for Channel A.
3	RECEIVE DATA (Channel B)	RXD-B	This is the Serial Data Input for Channel B.
21	TRANSMITTER READY (Channel A)	TXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
40	TRANSMITTER READY (Channel B)	TXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
22	RECEIVER READY (Channel A)	RXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RECEIVER READY (Channel B)	RXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TRANSMITTER EMPTY (Channel A)	TXE-A	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TRANSMITTER EMPTY (Channel B)	TXE-B	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BREAK DETECT (Channel A)	BRKDET-A	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BREAK DETECT (Channel B)	BRKDET-B	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	REQUEST-TO-SEND (Channel A)	$\overline{\text{RTS-A}}$	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	REQUEST-TO-SEND (Channel B)	$\overline{\text{RTS-B}}$	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1		NC	No Internal Connection.

Table 1 WD2123 PIN DESCRIPTIONS

GENERAL DESCRIPTION

The WD2123 Block Diagram is shown in Figure 2. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; $\overline{RTS}$ output is held high; the $\overline{CTS}$ and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ORGANIZATION

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8 bit data bus through a common set of bus transceivers.

A diagram of one of the two communication controllers is shown in Figure 3. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE ($\overline{RE}$), WRITE ENABLE ($\overline{WE}$) and CONTROL or DATA SELECT ($C/\overline{D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 4. The 4 low order DATA BUS bits, DO-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals $\overline{CS3}$, $\overline{WE}$ and $C/\overline{D}$ are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

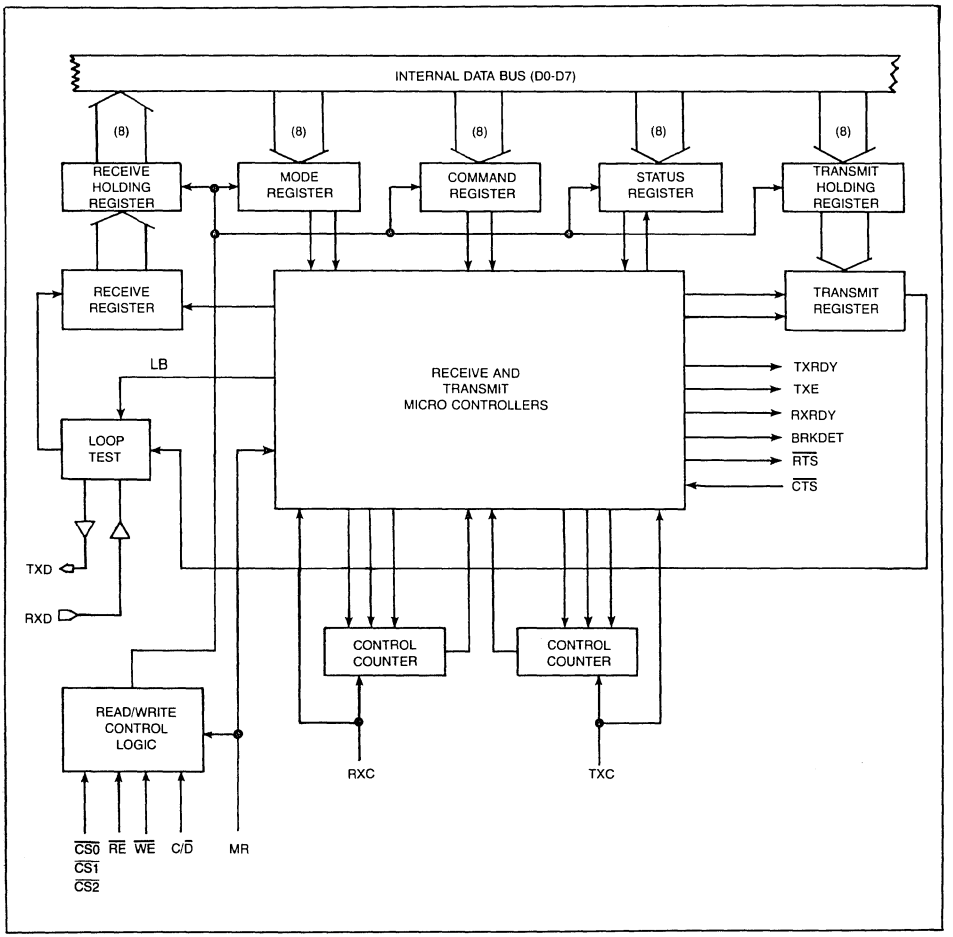


Figure 3 RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

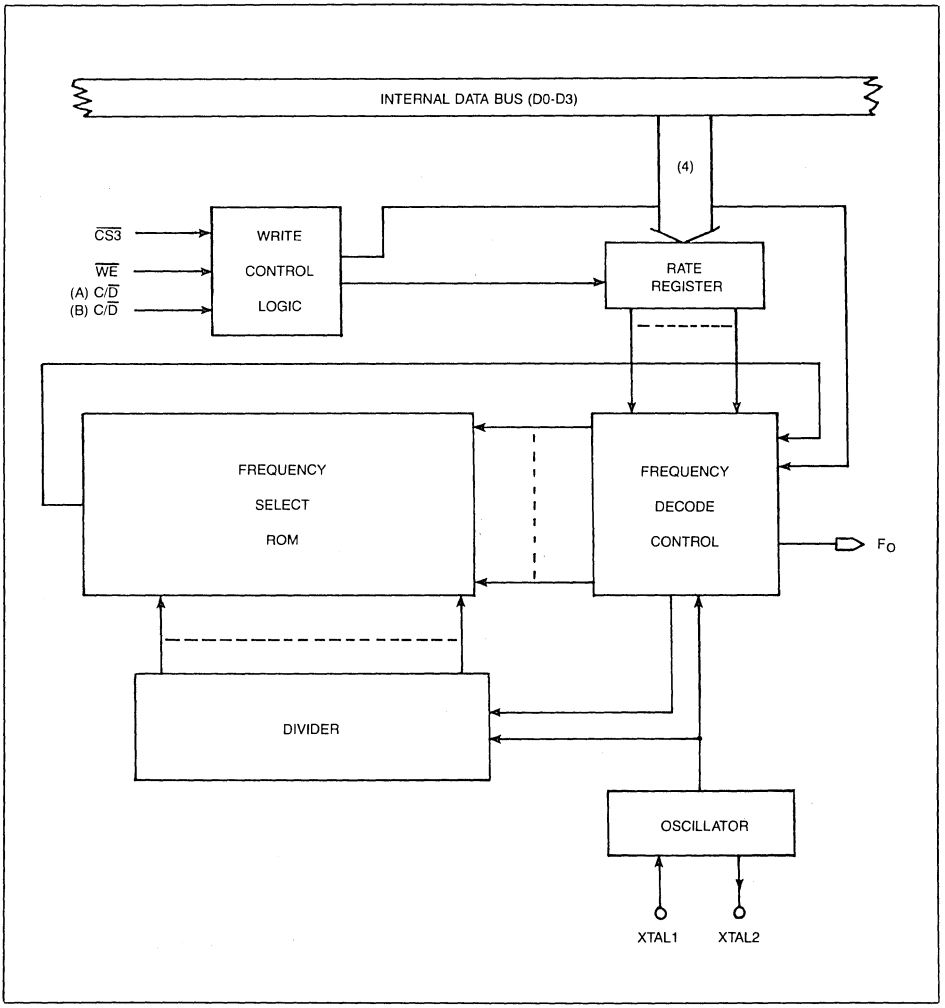


Figure 4 WD2123 BAUD RATE GENERATOR DIAGRAM

The WD2123 registers are addressed by the following table:

C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	REGISTER SELECTED		
L	L	H	L	H	H	RECEIVE HOLDING REG.	—	CHA
L	H	L	L	H	H	TRANSMIT HOLDING REG.	—	CHA
H	L	H	L	H	H	STATUS REG.	—	CHA
H	H	L	L	H	H	MODE AND COMMAND REG.	—	CHA
L	L	H	H	L	H	RECEIVE HOLDING REG.	—	CHB
L	H	L	H	L	H	TRANSMIT HOLDING REG.	—	CHB
H	L	H	H	L	H	STATUS REG.	—	CHB
H	H	L	H	L	H	MODE and COMMAND REG.	—	CHB
L	H	L	H	H	L	RATE REG.	—	CHA
H	H	L	H	H	L	RATE REG.	—	CHB
X	X	X	H	H	H	DATA BUS IN HIGH IMPEDANCE MODE		

Table 2 WD2123 REGISTER ADDRESSING

Note:

"L" means V_{IL} at pins.
"H" means V_{IH} at pins.
"X" means don't care.

The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	**L1**	**CHARACTER LENGTH**
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN		**PARITY ENABLE**
0		Disable Parity
1		Enable Parity
EP		**PARITY SELECT**
0		Odd Parity
1		Even Parity
S2	**S1**	**NUMBER OF STOP BITS**
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits
1	1	2 Bits

Table 3 WD2123 MODE REGISTERS

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN	TRANSMIT ENABLE
1	Enable
0	Disable
CS	**CLOCK SELECT**
1	External Clock Select Mode
0	Internal Clock Select Mode
REN	**RECEIVE ENABLE**
1	Enable
0	Disable
SBK	**SEND BREAK CHARACTER**
1	Force TXD Low
0	Normal Operation
ER	**ERROR RESET**
1	Reset Error Flags
0	No Reset
RTS	**REQUEST TO SEND**
1	Force $\overline{RTS}$ pin = 0 (V_{OL})
0	Force $\overline{RTS}$ pin = 1 (V_{OH})
IR	**INTERNAL RESET**
1	Returns WD2123 to Mode Instruction Format
LB	**LOOP BACK ENABLE**
0	Normal Operation Mode
1	Local Loop-Back Mode

Table 4 WD2123 CONTROL REGISTERS

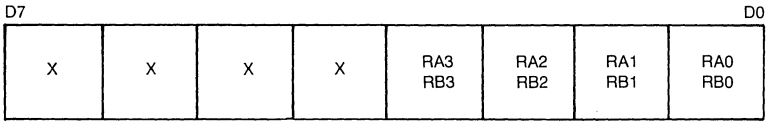
The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY	TRANSMITTER READY
1	Denotes THR is empty and ready for a new character
0	THR not empty. (Reset when THR is loaded by CPU)
RXRDY	RECEIVER READY
1	Denotes that the RHR contains a valid character
0	RHR does not contain a valid character. (Reset when the CPU reads the RHR)
TXE	TRANSMITTER EMPTY
1	Denotes that the TR is empty
0	Denotes that the TR is not empty
PE	PARITY ERROR
1	Denotes Parity Error
0	No Parity Error. (Reset by ER bit of command register)
OE	OVERRUN ERROR
1	Denotes Overrun Error
0	No Overrun Error. (Reset by ER bit of command register)
FE	FRAMING ERROR
1	Denotes Framing Error
0	No Framing Error. (Reset by ER bit of command register)
BRKDET	BREAK DETECT
1	Indicates that the receiver has detected a line break condition. (FE will also be set)
0	No Break Condition detected for at least one bit time
CTS	CLEAR-TO-SEND
1	Indicates that the $\overline{CTS}$ pin is active (V_{IL})
0	Indicates that the $\overline{CTS}$ pin is not active (V_{IH})

Table 5 WD2123 STATUS REGISTERS

The WD2123 contains two RATE REGISTERS that are used to select 16 BAUD rates when CR1 = 1 and SELCLK = 1. The Format of the RATE REGISTERS is shown below. Note that the Receiver and the Transmitter of any channel run off the same Baud clock except when CR1 = 0, then the Transmitter runs off the Baud Clock and the Receiver runs off an externally applied signal input on the SELCLK pin.



When C/D = 0, RA3 to RA0 are loaded.
When C/$\overline{D}$ = 1, RB3 to RB0 are loaded.

The C/$\overline{D}$ line is used in conjunction with $\overline{CS3}$ and $\overline{WE}$ to program the desired BAUD rate. When C/$\overline{D}$ is low, Channel A is selected, and when C/$\overline{D}$ is high, Channel B is selected. The low order 4 bits of the DATA BUS are loaded into the selected rate register, and the high order 4 bits are ignored.

When the crystal frequency equals 1.8432 MH_Z, the following baud rates may be programmed.

R3	R2	R1	R0	BAUD RATE	FREQUENCY
0	0	0	0	50	.800 KHZ
0	0	0	1	75	1.200
0	0	1	0	110	1.760
0	0	1	1	134.5	2.150
0	1	0	0	150	2.400
0	1	0	1	200	3.200
0	1	1	0	300	4.800
0	1	1	1	600	9.600
1	0	0	0	1200	19.200
1	0	0	1	1800	28.800
1	0	1	0	2400	38.400
1	0	1	1	3600	57.600
1	1	0	0	4800	76.800
1	1	0	1	7200	115.200
1	1	1	0	9600	153.600
1	1	1	1	19,200	307.200

Table 6 WD2123 BAUD RATE REGISTERS

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, C/$\overline{D}$, $\overline{RE}$, $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, $\overline{CTS}$ and $\overline{RTS}$, are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first *control write* operation (C/$\overline{D}$ = 1) to contain a *mode instruction*. Any *subsequent control write* operations will be transferred to the *command instruction* register.

Now when it is desired to *change* the *mode instruction* register contents, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write* operation to be a *new mode instruction*. After the new mode instruction is written to the chip, all subsequent control write operations will again be interpreted as *command instructions*. Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

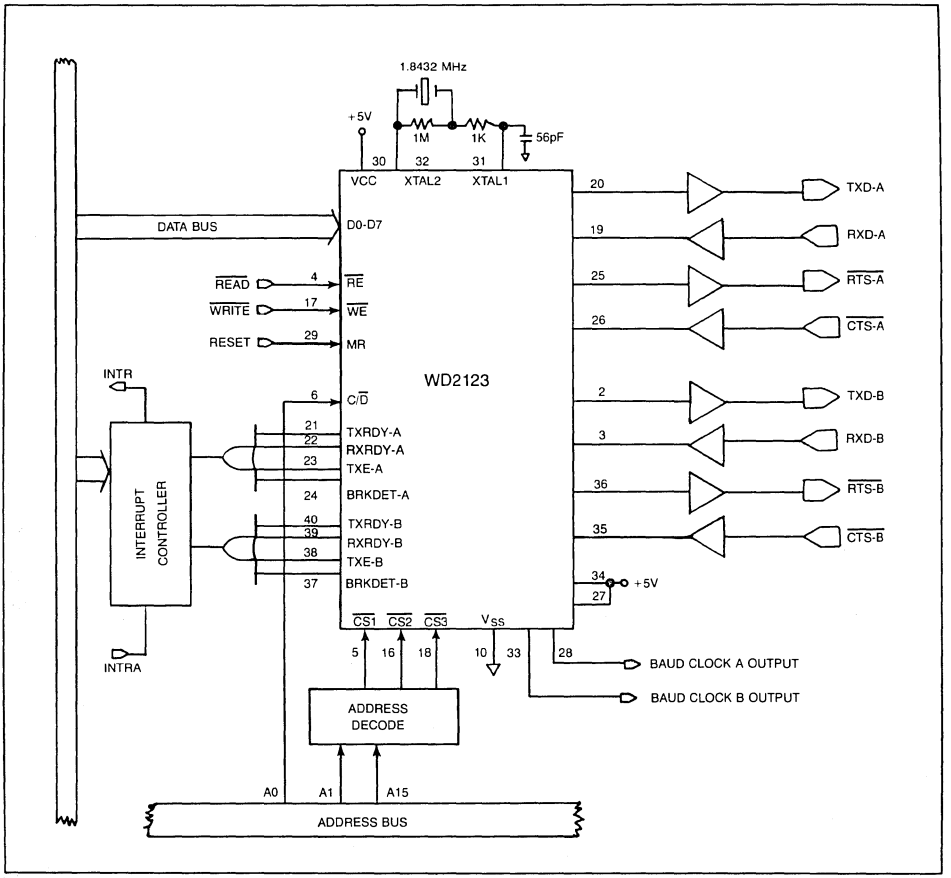


Figure 5 WD2123 MICROPROCESSOR APPLICATION

ABSOLUTE MAXIMUM RATINGS

V_{DD} with respect to V_{SS} ..... 0.5V to +12V
Voltage on Any Pin with Respect to Ground ..... —0.5V to +7V
Power Dissipation ..... 500Mw.

STORAGE TEMPERATURE:
Ceramic: —65°C to +150°C
Plastic: —55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	—0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = —100 uA
I_{DL}	Data Bus Leakage (High Impedance State)			—50 10	uA uA	V_{OUT} = 0.45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		50	100	mA	V_{CC} = 5.25V No Load

Table 7 WD2123 D.C. PARAMETERS

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Table 8 WD2123 CAPACITANCE LEVELS

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to + 70C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS Read Cycle					
t_{AR}	Address Stable Before READ (CS,C/D)	50		ns	
t_{RA}	Address Hold Time for READ (CS,C/D)	5		ns	
t_{RE}	READ Pulse Width	350		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 50 pF
t_{RDH}	READ to Data Floating		200	ns	C_L = 50pF
		25		ns	C_L = 15 pF
Write Cycle					
t_{AW}	Address Stable Before WRITE	20		ns	
t_{WA}	Address Hold Time for WRITE	20		ns	
t_{WE}	WRITE Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for WRITE	100		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		200	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	C_L = 100 pF
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	

Table 9 WD2123 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
f_{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800	 	 us ns	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800	 	 us ns	
t_{TX}	TxRDY Delay from Center of Stop Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RxRDY Delay from Center of Stop Bit		½	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t_{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t_{TOD}	TXD Output from Falling Edge of WRITE		1½	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of WRITE (RTS)		200	ns	
t_{CR}	Control to READ Set-Up Time (CTS)		1	t_{TXC}	

Table 9 WD2123 A.C. PARAMETERS

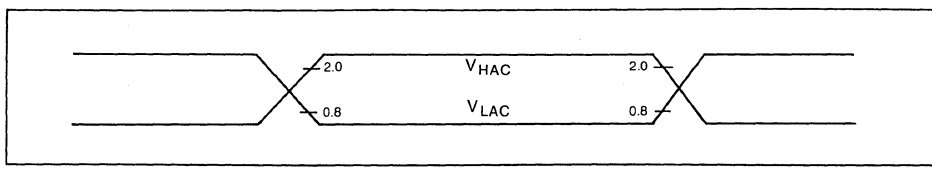


Figure 6 A.C. TEST POINTS

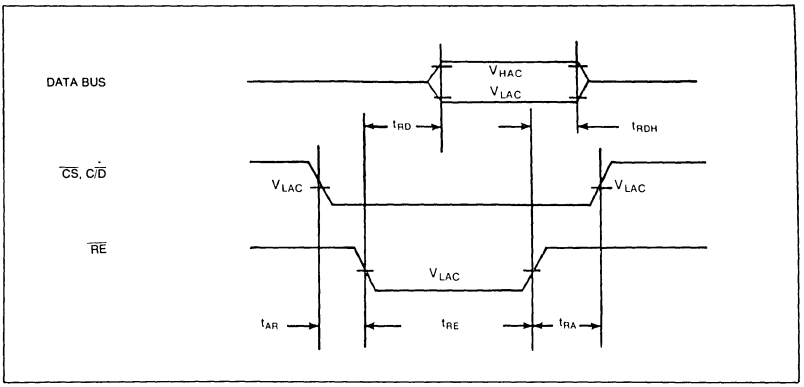


Figure 7 WD2123 READ TIMING

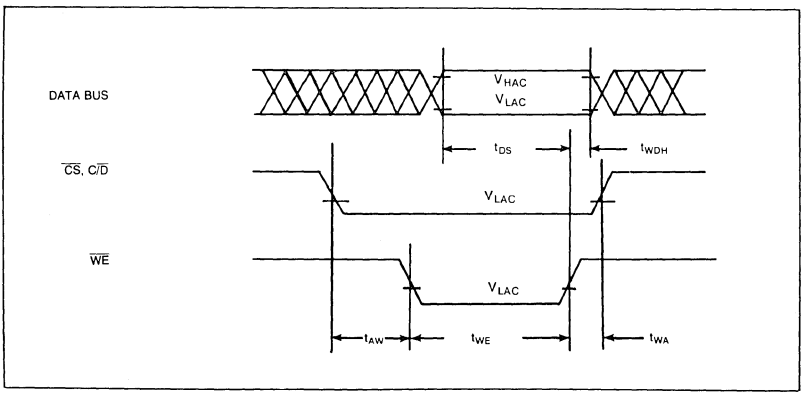


Figure 8 WD2123 WRITE TIMING

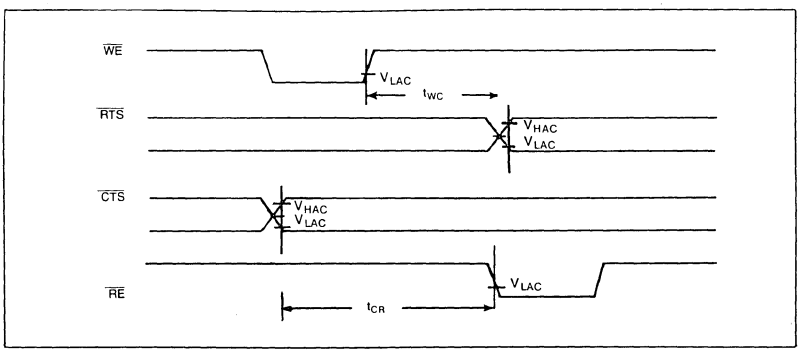


Figure 9 WD2123 INTERFACE CONTROL TIMING

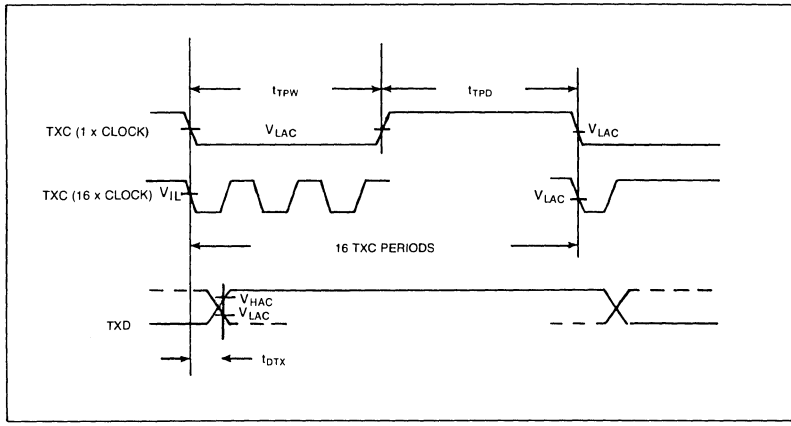


Figure 10 WD2123 TRANSMITTER CLOCK AND DATA TIMING

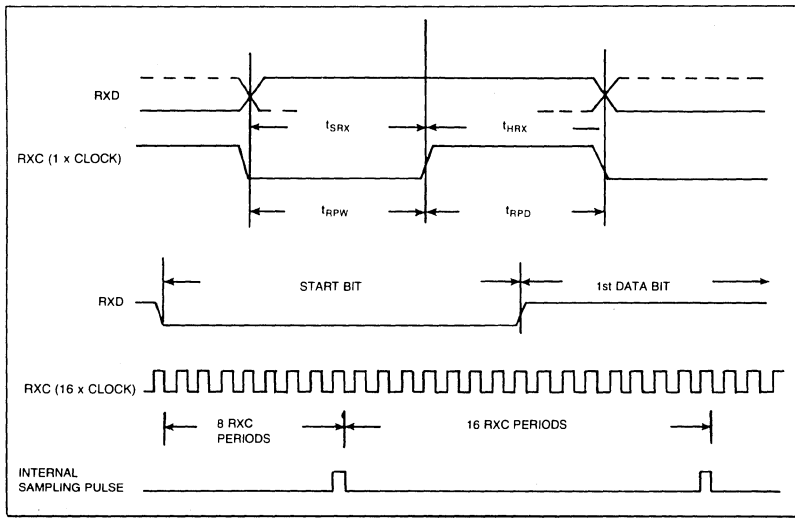


Figure 11 WD2123 RECEIVER CLOCK AND DATA TIMINGS

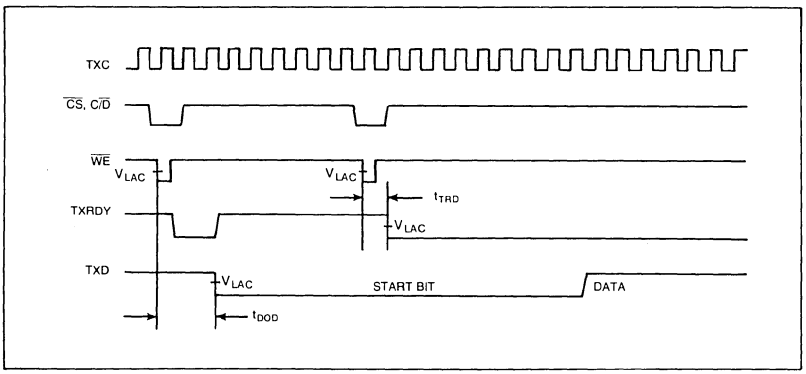


Figure 12 WD2123 TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

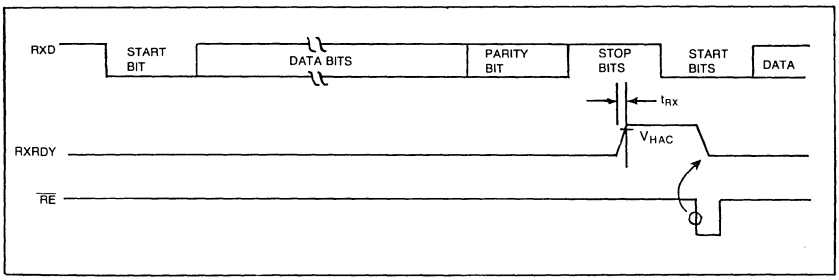


Figure 13 WD2123 RXRDY TIMING

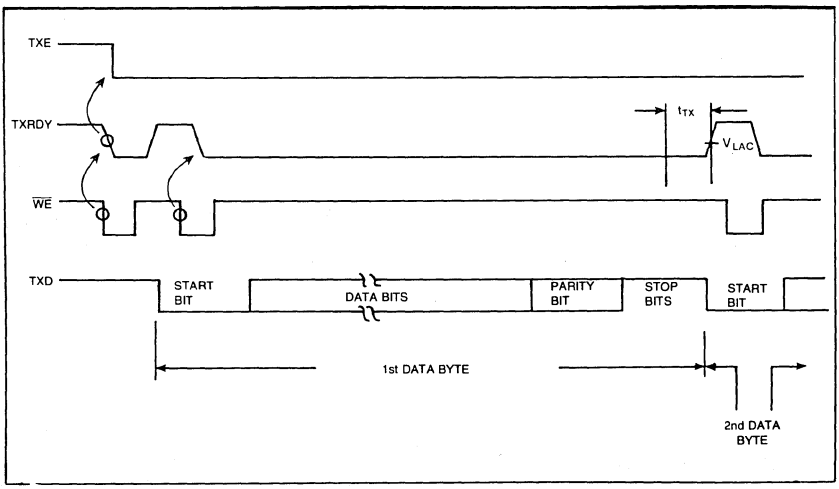
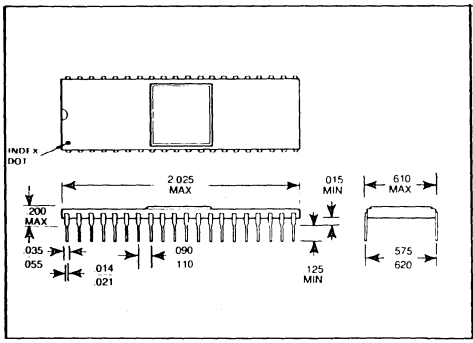
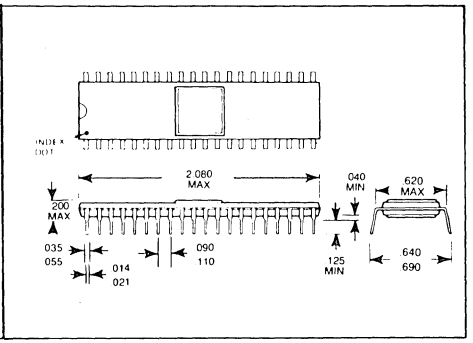


Figure 14 WD2123 TXRDY TIMING



WD2123A CERAMIC PACKAGE



WD2123B PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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