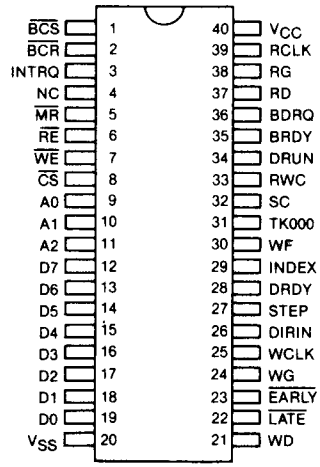
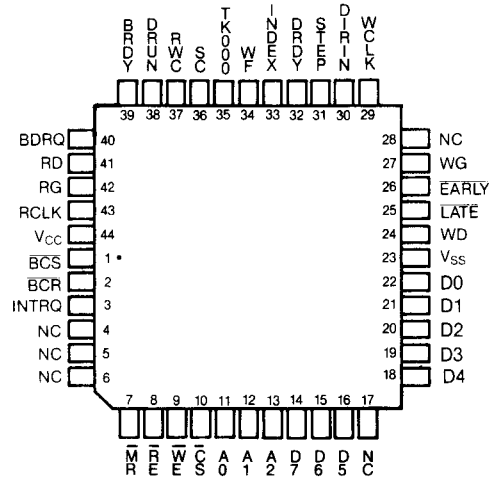
WD1010-05 Winchester Disk Controller

FEATURES

- ST506-SA1000 COMPATIBLE
- MULTIPLE SECTOR READ/WRITE
- UP TO 5 MBITS/SEC DATA RATE
- UNLIMITED SECTOR INTERLEAVE
- AUTOMATIC FORMATTING
- CRC/ECC CAPABILITY WITH EXTERNAL ECC GENERATOR/CHECKER
- PROGRAMMABLE RETRIES
- VARIABLE SECTOR SIZE
- SINGLE +5V SUPPLY



PIN DESIGNATION



QUAD PIN DESIGNATION

DESCRIPTION

The WD1010-05 is a MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. It is compatible with the Seagate ST506 and the Shugart Associates SA1000 drives, as well as all other 5 ¼" and 8" products utilizing the same type of interface. On the host side, an 8-bit bi-directional bus accepts all commands, data, and status bytes. The Western Digital WD1000 series of board level controllers are software compatible with the WD1010-05.

Operating from a single 5 volt supply, the WD1010-05 is implemented in NMOS silicon gate technology and is available in a 40-pin dual-in-line and QSM package.

ARCHITECTURE

The WD1010-05 Winchester Disk Controller provides the necessary link between an 8-bit, parallel processor and a Winchester disk drive. The WD1010-05 may be programmed to either automatically retry errors, or to terminate the command. The internal architecture of the WD1010-05 is shown in Figure 1. Its major functional blocks are:

PLA Controller

The PLA interprets commands and provides all control functions. It is synchronized with WCLK.

Magnitude Comparator

A 10-bit magnitude comparator is used for calculation of drive step, direction, present and desired cylinder position.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	Active low output used to enable reading or writing of the external sector buffer.
2	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	Active low output that is strobed by the WD1010-05 prior to read/write operations. This pin is strobed whenever $\overline{BCS}$ changes state.
3	INTRQ	INTERRUPT REQUEST	INTRQ is an output asserted upon completion of a command and de-asserted when the Status Register is read or a new command is written into the Command Register. This signal can be programmed to occur with BDRQ and DRQ during Read Command.
4	NC	NO CONNECTION	
5	$\overline{MR}$	$\overline{MASTER\ RESET}$	A logic low in this input will initialize all internal logic.
6	$\overline{RE}$	$\overline{READ\ ENABLE}$	Tri-state bi-directional line used as an input for reading the task register and an output when the WD1010-05 is reading the buffer.
7	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	Tri-state bi-directional line used as an input for writing into the task register and as an output when the WD1010-15 is writing to the buffer.
8	$\overline{CS}$	$\overline{CHIP\ SELECT}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
9 10 11	A0 A1 A2	ADDRESS 0 ADDRESS 1 ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
12 thru 19	D7 thru D0	DATA 7 thru DATA 0	8-bit tri-state bi-directional bus used for transfer of commands, status, and data.
20	V_{SS}	GROUND	Ground.
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
22 23	$\overline{LATE}$ $\overline{EARLY}$	$\overline{LATE}$ $\overline{EARLY}$	Precompensation outputs used to delay the WD pulses externally.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
25	WCLK	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
26	DIRIN	DIRECTION IN	This output determines the direction the stepping motor will move the heads. High = in, Low = out.
27	STEP	STEP PULSE	This output generates a pulse for stepping the drive motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
29	INDEX	INDEX PULSE	A rising edge on this input informs the WD1010-05 when the index hole has been encountered.
30	WF	WRITE FAULT	An error input to the WD1010-05 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010-05 which indicates positioning over track 000.

PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	SC	SEEK COMPLETE	A rising edge on this input informs the WD1010-05 when head settling time has expired. In the Format Command, it is used to extend the gap.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
34	DRUN	DATA RUN	This input informs the WD1010-05 when a field of ones or zeroes have been detected.
35	BRDY	BUFFER READY	The rising edge of this input informs the controller that the Sector Buffer is full or empty.
36	BDRQ	BUFFER DATA REQUEST	BDRA and DRQ (Bit 3 Status Register) are asserted when the Buffer is to be read from or written to, by the Host. BDRQ can be used by a DMA controller or by the Host during Programmed I/O. DRQ must be polled by the Host if used during programmed I/O.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	RCLK	READ CLOCK	A nominal square wave clock input derived from the external data recovery circuits.
40	V_{CC}	+5 VOLT	+5V

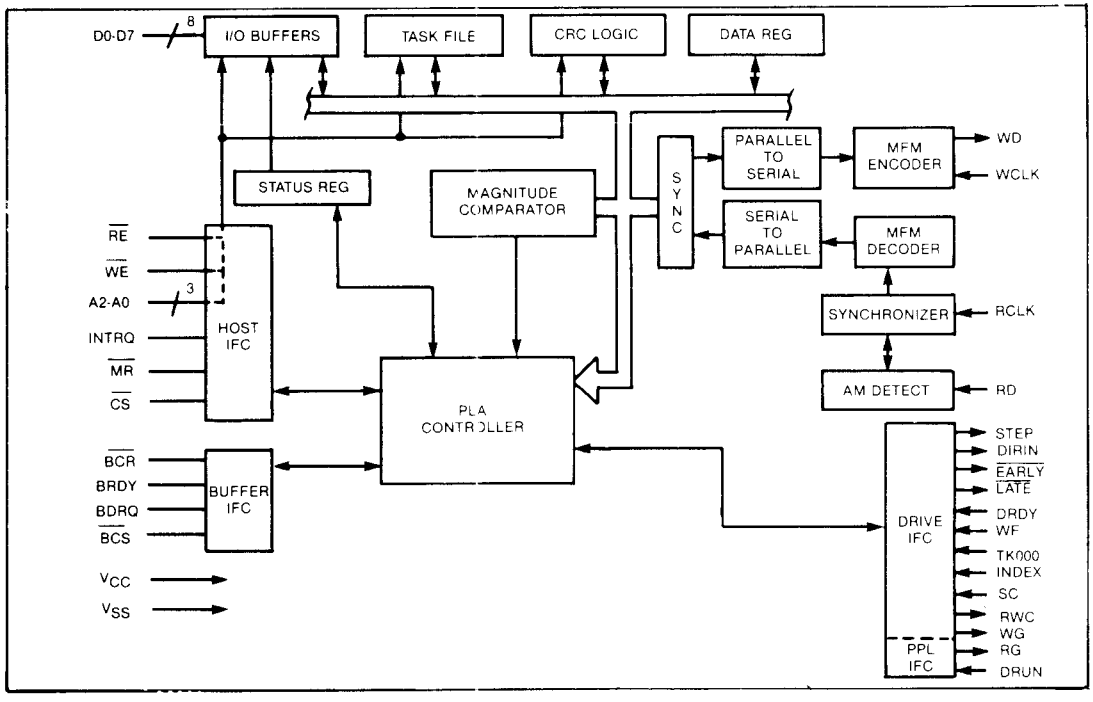


FIGURE 1.
WD1010 BLOCK DIAGRAM

CRC Logic

Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is $X^{16} + X^{12} + X^5 + 1$.

MFM Encode/Decode

Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WCLK; a clock having a frequency equivalent to the bit rate. The MFM decode operates from RCLK; a bit rate clock generated from the external data separator. RCLK and WCLK need not be synchronized.

AM Detect

The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = A1 hex, Clock = 0A hex) used in each ID and data field.

Host/Buffer IFC

This logic contains all of the necessary circuitry to communicate with the 8-bit host processor.

Drive IFC

This logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the WD1010-05 controller requires three sections of external logic. These are buffers/receivers, data separator, and write precompensation. Figure 2 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WD1010-05 supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The WD1010-05 interacts with the data separator through the DRUN and RG signals. The block diagram of the

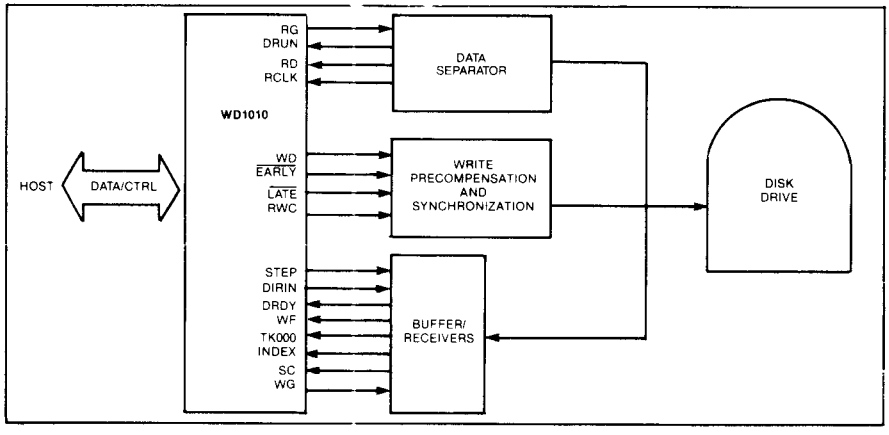


FIGURE 2. DRIVE INTERFACE BLOCK DIAGRAM

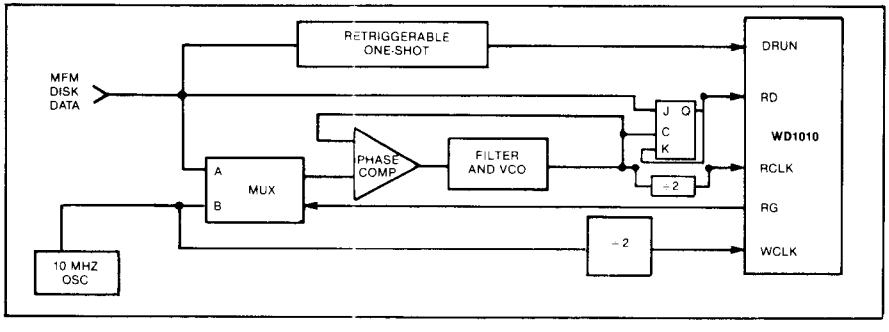


FIGURE 3. DATA RECOVERY CIRCUIT

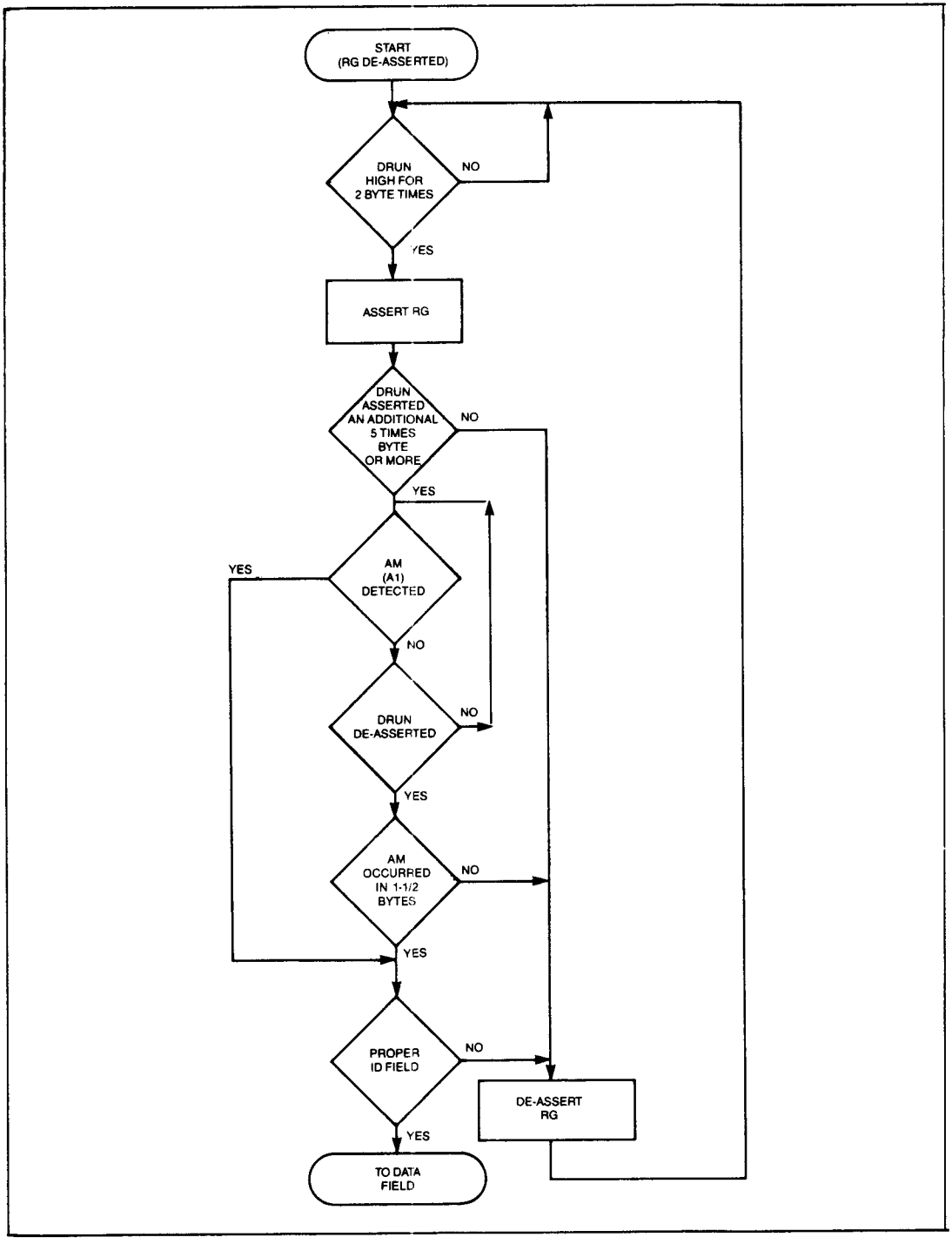


FIGURE 4. PLL CONTROL SEQUENCE FOR ID FIELD

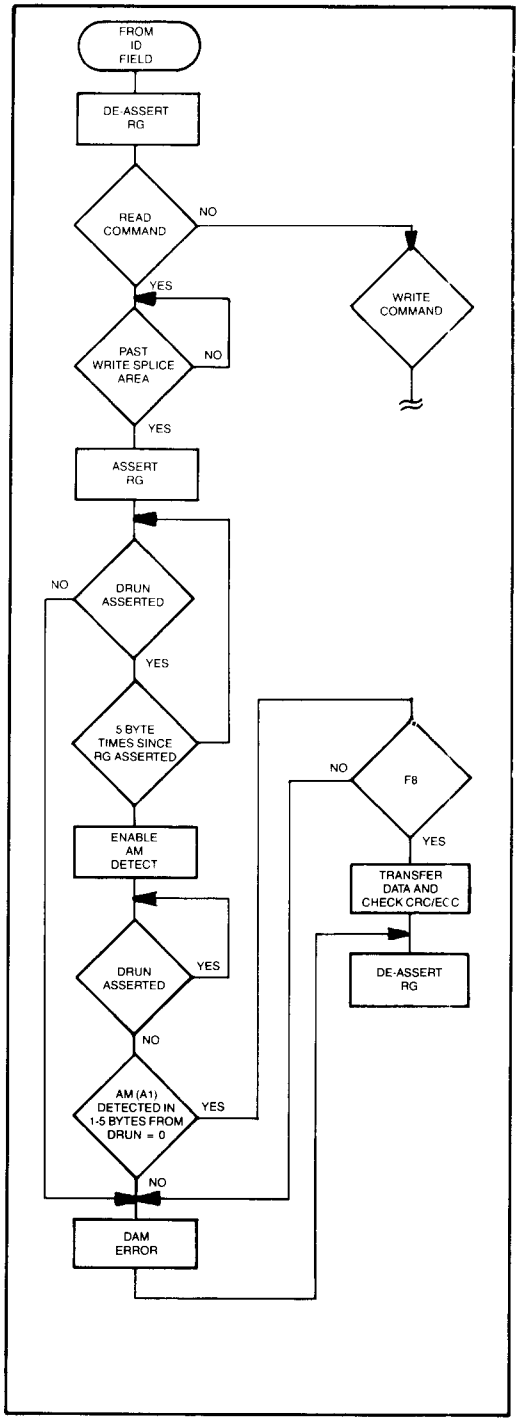


FIGURE 4. (CONT.)
PPL CONTROL SEQUENCE FOR DATA FIELD

data separator circuit is shown in Figure 3. Read data from the drive is presented to the RD input of the WD1010-05, the reference multiplexor, and a retriggerable one shot. The read gate output will be low when the WD1010-05 is not inspecting data. The PLL at this time should remain locked to the reference clock.

When any Read/Write command is initiated and a search for address marks begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeroes. An internal counter times out to see that DRUN is high for 2 byte times. Read gate is set by the WD1010-05, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to 7 bytes times, RG is lowered and the process is repeated. Read gate will remain active high until a non-zero, non-address mark byte is detected. It then will lower read gate for 2 byte times (to allow the PLL to lock back on the reference clock) and start the DRUN search over again. If an address mark is detected, read gate will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart of Figure 4.

The write precompensation logic is controlled by the signals RWC, $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$. The cylinder in which the RWC line becomes active is controlled by a register in the Task File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the write precomp register value is FF, then RWC will always be low.

The signals $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are used to tell the precomp how much delay is required on the write data pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the signal $\overline{\text{EARLY}}$ occurs after the fact, write data should be delayed one interval when both $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are deasserted; two intervals when $\overline{\text{LATE}}$ is asserted; and no delay when $\overline{\text{EARLY}}$ is asserted. An interval, for example, is 12-15 ns. on the ST506. $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ will be active slightly ahead of the write data pulse; $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ will never be asserted at the same time. The $\overline{\text{EARLY}}$ $\overline{\text{LATE}}$ signals function independently of the content of the RWC register.

Examples for all three of the above circuits can be found in the WD1010 Application Note.

HOST INTERFACE

The primary interface between the host processor and the WD1010-05 is through an 8-bit bi-directional bus. This bus is used to transmit/receive data to both the WD1010-05 and a sector buffer. The sector buffer is constructed with either FIFO memory or static RAM and a counter. Since the WD1010-05 will make the bus active when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 5 shows a typical connection to a sector buffer implemented with RAM memory.

Whenever the WD1010-05 is not using the sector buffer, the $\overline{BCS}$ is de-asserted. This allows the host to access the WD1010's Task File, and to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_0- A_2 are '000'; an unused address in the WD1010-05. A binary counter is enabled whenever $\overline{RE}$ or $\overline{WE}$ goes active and incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_0-A_2 '000'; allowing access to the WD1010-05's internal registers while keeping the RAM tri-stated.

During write sector commands, the processor sets up data in the Task File and issues the command. The WD1010 then generates a status to inform the host it may load the buffer with the data to be written. When the counter reaches its maximum count, the BRDY signal is made active (by the "carry" out of the counter), informing the WD1010-05 that the buffer is full. (BRDY is a rising edge activated signal). The $\overline{BCS}$ is then asserted, disconnecting the host through the transceivers, and the $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1010-05 to allow it access to the buffer. When the WD1010-05 is done using the buffer, it disables $\overline{BCS}$ which again allows host access to this local bus. The read sector commands operate in a similar manner, except the buffer is loaded by the WD1010-05 instead of the host.

Another control signal called BDRQ can be connected to a DMA controller in the Host, or can be polled by the Host for programmed I/O. For further explanation, refer to the description of the individual commands and the A.C. Timing Specifications. In a read command; an interrupt may be specified to occur either at the end of the command or when BDRQ is activated. The INTRQ is cleared either by reading the status register or by writing a new command in the command register.

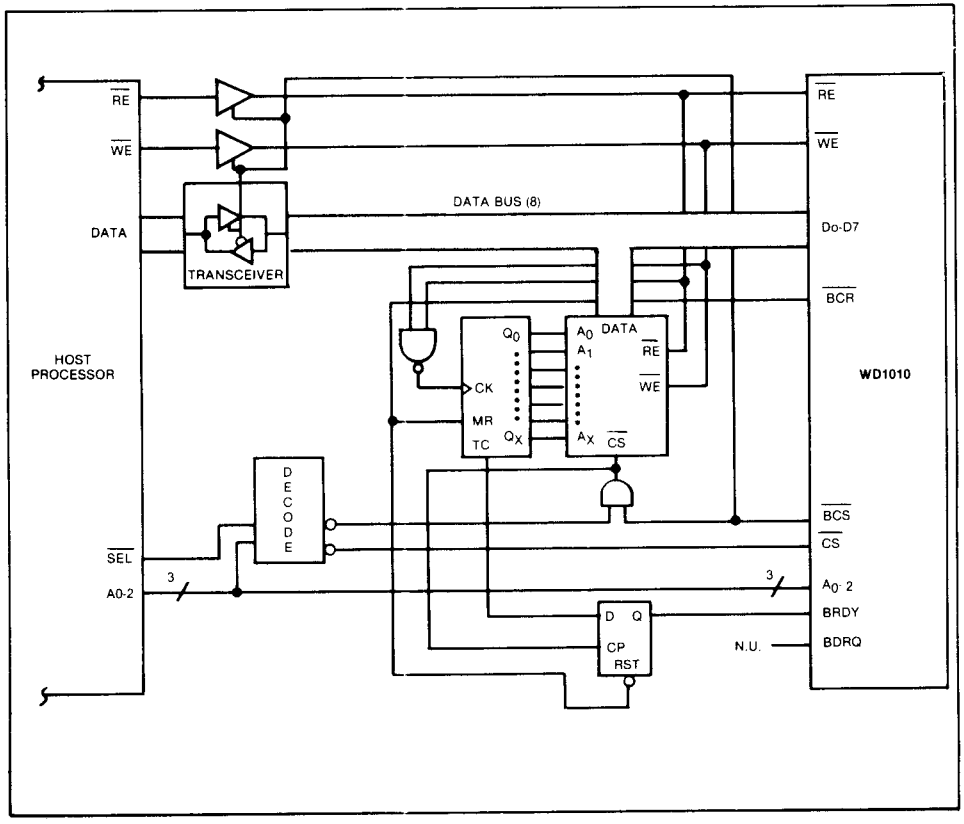


FIGURE 5.
HOST INTERFACE

TASK FILE

The Task File is a bank of nine registers used to hold parameter information pertaining to each command. These registers and their addresses are:

A_2	A_1	A_0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are not cleared by master reset ($\overline{MR}$).

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. These bits are defined as follows:

7	6	5	4	3	2	1	0
BB	CRC	-	ID	-	AC	TK	DM

Bit 7 – Bad Block Detect

This bit is set when an ID field has been encountered that contains a bad block mark. Used for bad sector mapping.

Bit 6 – CRC Data Field

This bit is set when a CRC error occurs in the data field. With Retry enabled, ten more attempts are made to read the sector correctly. If none of these attempts are successful, the Error Status is set also (bit 0 in the Status Register). If one of the attempts is successful, this bit remains set to inform the Host that a marginal condition exists. However, the Error Status bit is not set. Even if errors exist, the data can be read.

Bit 5 – Reserved

Not used; forced to a zero.

Bit 4 – ID Not Found

This bit is set to indicate that the correct cylinder, head, sector number or sector size parameter could not be found, or that a CRC error occurred on the ID field. This bit is set on the first failure and remains set even if the error is recovered on a Retry. When recovery is unsuccessful, the Error Status bit is set also (bit 0 in the Status Register).

Bit 3 – Reserved

Not used; forced to a zero.

Bit 2 – Aborted Command

This bit is set if a command was issued while the DRDY is de-asserted or the WF is asserted. The aborted command bit will also be set if an undefined command code is written into the command register, but an implied seek will be executed.

Bit 1 – Track Zero Error

This bit is set only by the restore command. It indicates that the TK000 has not gone active after the issuance of 1024 stepping pulses.

Bit 0 – Data Address Mark Not Found

This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.

WRITE PRECOMP CYLINDER

This register is used to define the cylinder number where the RWC is to be asserted:

7	6	5	4	3	2	1	0
CYLINDER NUMBER ÷ 4							

The value 00-FF loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus, a value of 01 hex will cause RWC to activate on cylinder 4; 02 hex on cylinder 8, and so on. Switching points are then 0, 4, 8, . . . The RWC will be asserted when the present cylinder is equal to 4 times or more than the value in this register. For example, the ST506 requires precomp on cylinder 128 (80 hex) and above. Therefore, the write precomp cylinder register should be loaded with 32 (20 hex).

A value of FF hex will always cause RWC to be low, no matter what the cylinder number values are.

SECTOR COUNT

This register holds the number of sectors that are to be transferred to the buffer.

7	6	5	4	3	2	1	0
# OF SECTORS							

This register is used during a multiple sector R/W command. The written value is decremented after each sector is transferred to the sector buffer. A zero represents a 256 sector transfer, a 1 = one sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of a desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. The sector number register may contain any value from 0 to 255.

CYLINDER NUMBER LOW

This register holds the least significant eight bits of the desired cylinder number.

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used with the cylinder number high register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH

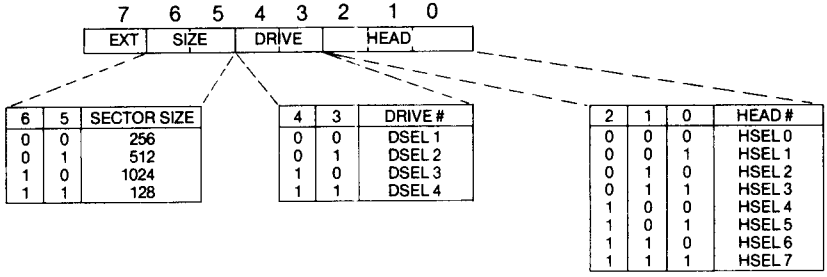
This register defines the two most significant bits of the cylinder number desired:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the WD1010-05 is another pair of registers that hold the actual position number where the R/W heads are located. The cylinder number high and lkow registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WD1010-05 automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a Restore.

SDH BYTE

This register contains the desired sector size, drive number, and head number parameters. The format is:



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL 1
0	1	DSEL 2
1	0	DSEL 3
1	1	DSEL 4

2	1	0	HEAD #
0	0	0	HSEL 0
0	0	1	HSEL 1
0	1	0	HSEL 2
0	1	1	HSEL 3
1	0	0	HSEL 4
1	0	1	HSEL 5
1	1	0	HSEL 6
1	1	1	HSEL 7

Both head number and sector size is compared against the disks' ID field. Head select and drive select lines are not available as outputs from the WD1010-05, and must be generated externally. Figure 6 shows the logic to implement these select lines.

Bit 7, the extension bit, is used to extend the data field by seven bytes when using ECC codes. CRC is not appended to the data field when EXT = 1; the data field becomes "sector size + 7" bytes long. CRC is checked on the ID field regardless of the state of the extention bit. Note that the sector size bits are written to the ID during a format command. The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written but does have bad block mark written. The format is:

BAD BLOCK	SIZE	0	0	HEAD#
7	6 5	4	3	2 1 0

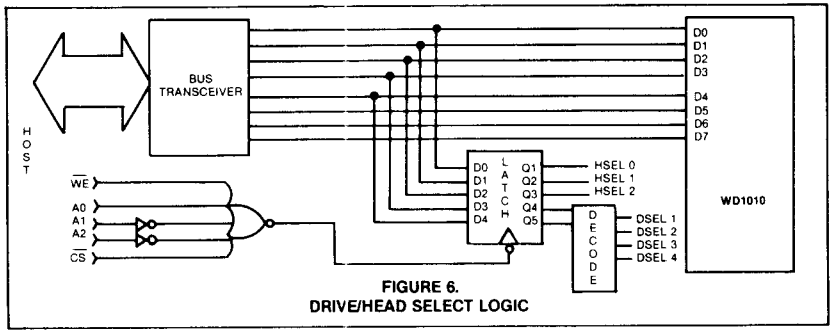


FIGURE 6.
DRIVE/HEAD SELECT LOGIC

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the WD1010 as well as reporting status from the drive control lines. The term INTRQ, if set, will be cleared when the status register is read. The format is:

7	6	5	4	3	2	1	0
BSY	RDY	WF	SC	DRQ	-	CIP	ERR

Bit 7 – Busy

This bit is set whenever the WD1010-05 is accessing the disk. Commands should not be loaded into the command register while busy is set. Busy is made active when a command is written into the WD1010-05 and is deactivated at the end of all commands except the read sector. While executing a read sector command, busy is deactivated after the sector buffer has been filled. When the BUSY bit is set, no other bits in either the status or other registers are valid.

Bit 6 – Ready

This bit reflects the state of DRDY.

Bit 5 – Write Fault

This bit reflects the state of the WF. Whenever the WF bit goes high, an interrupt will be generated.

Bit 4 – Seek Complete

This bit reflects that state of the SC. When a seek has been initiated by a command, it will pause until the seek is completed.

Bit 3 – Data Request

This bit reflects the state of the BDRQ. It is set when the sector buffer should be loaded with data or read by the host, depending upon the command. DRQ/BDRQ remains high until BRDY is sensed, indicating the operation is completed. The BRDQ signal can be used in DMA interfacing or Programmed I/O, while the DRQ bit can be used only for programmed I/O transfers.

Bit 2 – Reserved

Not used. This bit is always forced to a zero.

Bit 1 – Command In Progress

When this bit is set, a command is being executed and a new command should not be loaded until reset. Although a command may be executing, the sector buffer is still available for access by the host. When the WD1010 is not busy (bit 7 = 0) the status register may be read. If other registers are read while CIP, the status register contents are returned.

Bit 0 – Error

This bit indicates that a non-recoverable error has occurred. When the Host reads the status and finds this bit set, it must then read the Error Register to determine the type of error. This bit is reset when a new command is written into the command register.

COMMAND REGISTER

This write-only register is loaded with desired command:

7	6	5	4	3	2	1	0
C	O	M	M	A	N	D	

The command begins to execute immediately upon loading. This register should not be loaded while the Busy or CIP bits are set in the status register. The INTRQ, if set, will be cleared by a write to the command register.

INSTRUCTION SET

The WD1010 will execute six commands. Prior to loading the command register, the host must first set up the task file with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. Any subsequent writes to the command register will be ignored until execution is completed indicated by the resetting of the CIP bit in the status register.

COMMAND SUMMARY

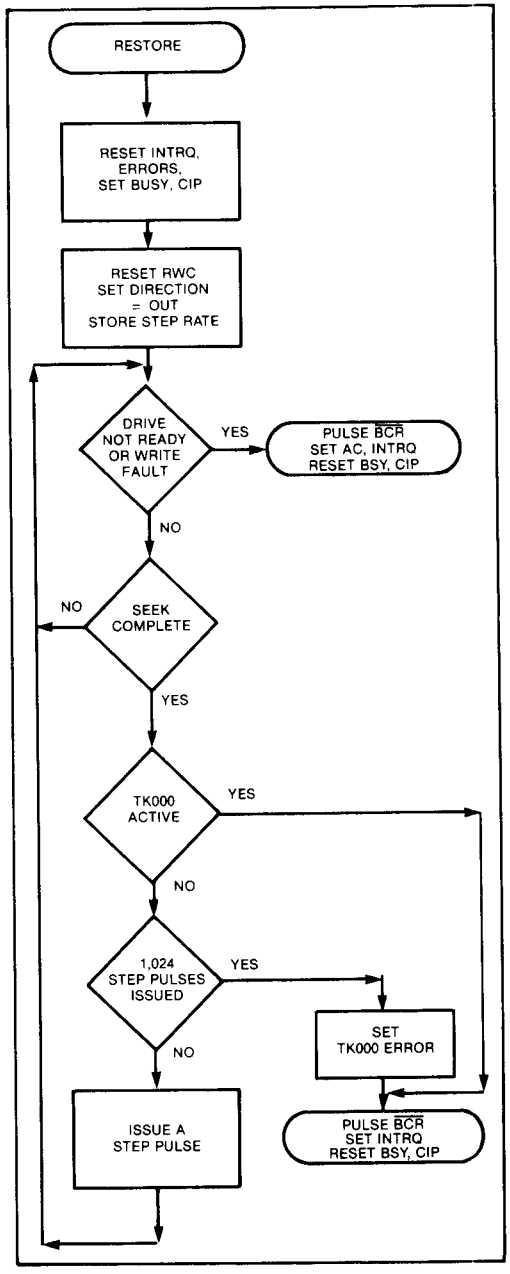
COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R_3	R_2	R_1	R_0
SEEK	0	1	1	1	R_3	R_2	R_1	R_0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_3-R_0 Rate Field
For 5 MHz WCLK:
R_3-R_0 = 0000 - 35 μs.
0001 - .5 ms.
0010 - 1.0 ms.
0011 - 1.5 ms.
0100 - 2.0 ms.
0101 - 2.5 ms.
0110 - 3.0 ms.
0111 - 3.5 ms.
1000 - 4.0 ms.
1001 - 4.5 ms.
1010 - 5.0 ms.
1011 - 5.5 ms.
1100 - 6.0 ms.
1101 - 6.5 ms.
1110 - 7.0 ms.
1111 - 7.5 ms.

Bit 0, ("T") Read Sector, Write Sector Commands
T = 0 Enable retries
T = 1 Disable retries

M = Multiple Sector Flag
M = 0 Transfer 1 sector
M = 1 Transfer multiple sectors

I = Interrupt Enable
I = 0 Interrupt at BDRQ time
I = 1 Interrupt at end of command



RESTORE COMMAND

The restore command is usually used on a power-up condition. The actual stepping rate used for the restore is determined by Seek Complete time. A step pulse is issued and the WD1010-05 waits for a rising edge on the seek complete line before issuing the next pulse. If 10 index pulses are received without a rising edge of seek complete, the WD1010 will switch to sensing the level of the SC line. If after 1,024 stepping pulses, the TK000 lines do not go active, the WD1010-05 will set the Track Zero error bit in the error register and terminate with an INTRQ. An interrupt will also occur if the write fault goes active or the DRDY goes inactive during execution.

The rate field specified (R3-R0) is stored in an internal register for future use in commands with implied seeks.

SEEK COMMAND

Since except for the SCAN ID all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The actual step rate used is taken from the rate field, which is also stored in an internal register for future use. If DRDY goes inactive or WF goes active, the command is terminated and an INTRQ is generated.

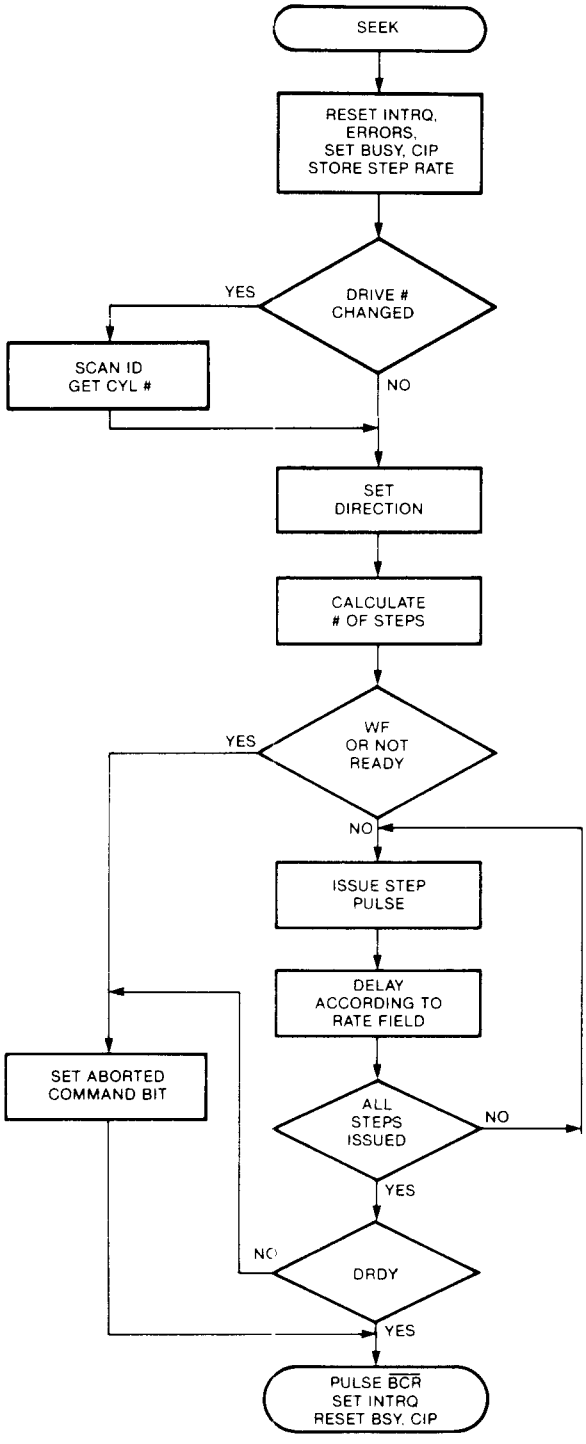
The direction and number of step pulses needed are calculated by comparing the contents of the cylinder register high/low to the cylinder position number stored internally. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. Seek complete is not checked at the beginning or end of the command.

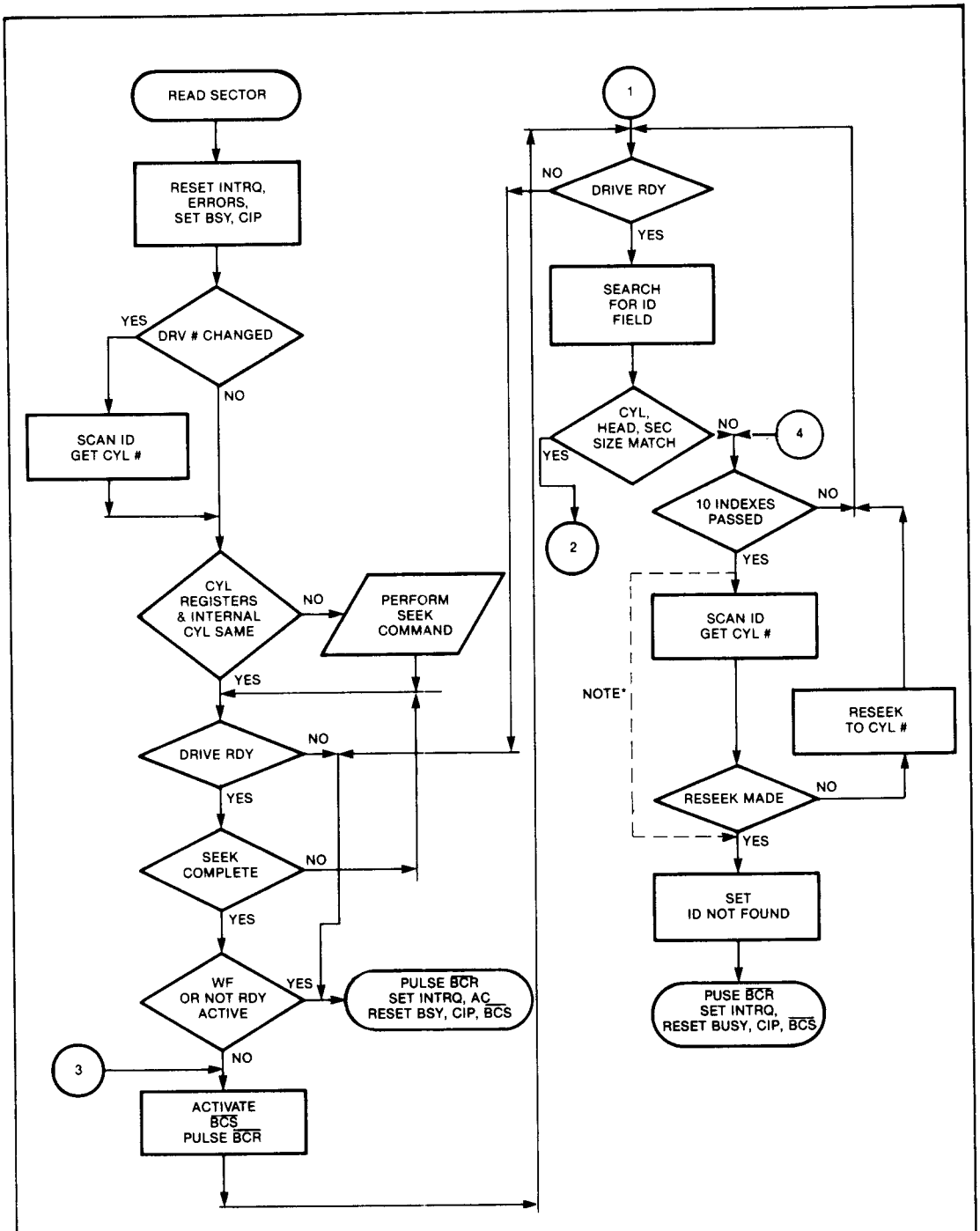
If an implied seek was performed, the WD1010-05 will wait until a rising edge of SC is received. If 10 revolutions occur before the rising edge of SC, the WD1010 will switch to level sensing of SC.

READ SECTOR

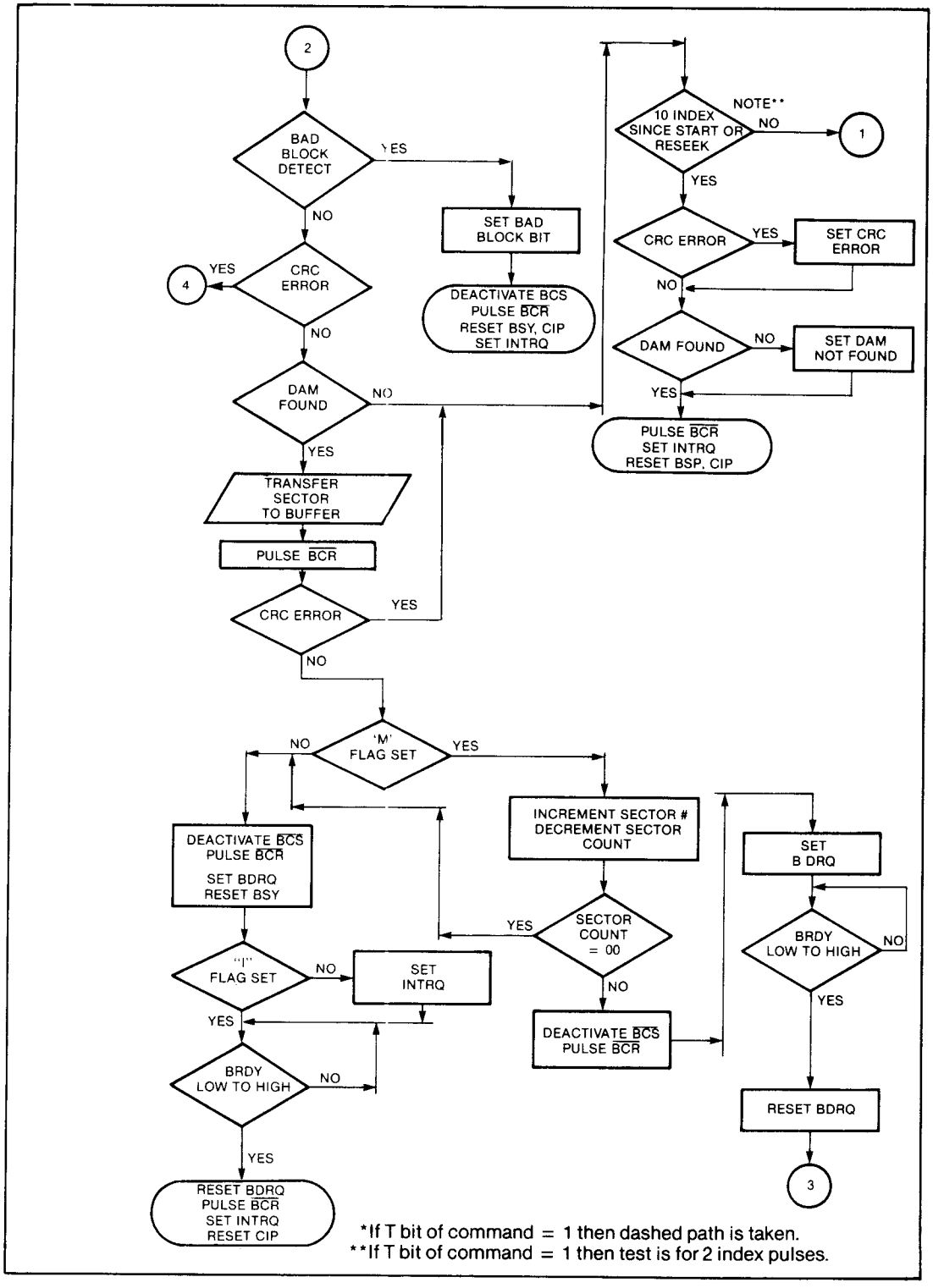
The read sector command is used to transfer one or more sectors of data from the disk to the sector buffer. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps calculation is performed and seek takes place. If an implied seek was performed, the WD1010-05 will search until a rising edge of seek complete is received. Write Fault and DRDY lines are checked throughout the command.

After seek complete is found to be true (with or without an implied seek), the search for an ID field occurs. The WD1010-05 must find an ID with the correct cylinder, head, sector size, and CRC within 10 revolutions if T bit of command is zero, and within 2 revolutions if T = 1; else the appropriate error bits will be set and the command terminated if T = 1. Both the Read and Write sector commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command. If T = 0, an automatic scan ID is performed to obtain cylinder position information and then, if necessary, a seek is performed. The search for the correct ID field is continued for 10 more disk rotations.


SEEK
RESET INTRQ, ERRORS, SET BUSY, CIP STORE STEP RATE
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SET DIRECTION
CALCULATE # OF STEPS
WF OR NOT READY
YES
NO
ISSUE STEP PULSE
DELAY ACCORDING TO RATE FIELD
SET ABORTED COMMAND BIT
ALL STEPS ISSUED
NO
YES
DRDY
NO
YES
PULSE BCR SET INTRQ RESET BSY, CIP



*If T bit of command = 1 then dashed path is taken after 2 index pulses.


2
BAD BLOCK DETECT
YES
SET BAD BLOCK BIT
DEACTIVATE BCS
PULSE BCR
RESET BSY, CIP
SET INTRQ
NO
4
YES
CRC ERROR
NO
DAM FOUND
NO
YES
TRANSFER SECTOR TO BUFFER
PULSE BCR
CRC ERROR
YES
NO
10 INDEX SINCE START OR RESEEK
NOTE**
NO
1
YES
CRC ERROR
YES
SET CRC ERROR
NO
DAM FOUND
NO
SET DAM NOT FOUND
YES
PULSE BCR
SET INTRQ
RESET BSP, CIP
'M' FLAG SET
NO
YES
DEACTIVATE BCS
PULSE BCR
SET BDRQ
RESET BSY
INCREMENT SECTOR #
DECREMENT SECTOR COUNT
SECTOR COUNT = 00
YES
NO
DEACTIVATE BCS
PULSE BCR
SET B DRQ
BRDY LOW TO HIGH
NO
YES
RESET BDRQ
3
"I" FLAG SET
NO
SET INTRQ
YES
BRDY LOW TO HIGH
NO
YES
RESET BDRQ
PULSE BCR
SET INTRQ
RESET CIP
*If T bit of command = 1 then dashed path is taken.
**If T bit of command = 1 then test is for 2 index pulses.

When the data address mark is found, the WD1010-05 is ready to transfer data to the buffer. After the sector data has been transferred, the I flag is checked. If the I flag is 0, the INTRQ is made active coincident with BDRQ, indicating a transfer of data is required by the host. If I = 1, the INTRQ will occur at the end of the command (i.e., after the buffer is unloaded by the host).

An optional M flag may be set for multiple sector transfers. When M = 0, one sector is transferred and the sector count register is ignored. When M = 1, multiple sectors are enabled. After each sector is transferred, the WD1010-05 decrements the sector count register and increments the sector number register. The next logical sector will be transferred, regardless of the interleave. Sectors are numbered at format time by a byte in the ID field.

For the WD1010 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. The sector transfers will continue until the sector count register equals zero. If the sector count register is non-zero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. Once this occurs, the buffer will again be free to accept the next sector in this multiple sector read command.

When M = 0 (Single Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes BCR; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Strobes BCR; sets $\overline{BCS}$ = 1 (Off).
(5)	1010:	Sets BDRQ = 1; sets DRQ flag.
(6)	1010:	If I bit = 1 then (9).
(7)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$).
(8)	1010:	Waits for BRDY then sets INTRQ = 1; End.
(9)	1010:	Sets INTRQ = 1.
(10)	Host:	Reads out contents of buffer (by strobing $\overline{RE}$); End.

When M = 1 (Multiple Sector Read)

(1)	Host:	Sets up parameters; issues read sector command.
(2)	1010:	Strobes BCR; sets $\overline{BCS}$ = 0 (On).
(3)	1010:	Finds sector specified; transfers data to buffer (by $\overline{WE}$ strobes).
(4)	1010:	Decrements sector count register; increments sector number register.
(5)	1010:	Strobes BCR; sets $\overline{BCS}$ = 1 (Off).
(6)	1010:	Sets BDRQ = 1; DRQ flag = 1.
(7)	Host:	Reads out content of buffer (by $\overline{RE}$ strobes).
(8)	Buffer:	Indicates data has been transferred by asserting BRDY.
(9)	1010:	When BRDY is asserted, go to (11) if sector count = 0.
(10)	1010:	Go to Step (2).
(11)	1010:	Activates INTRQ.

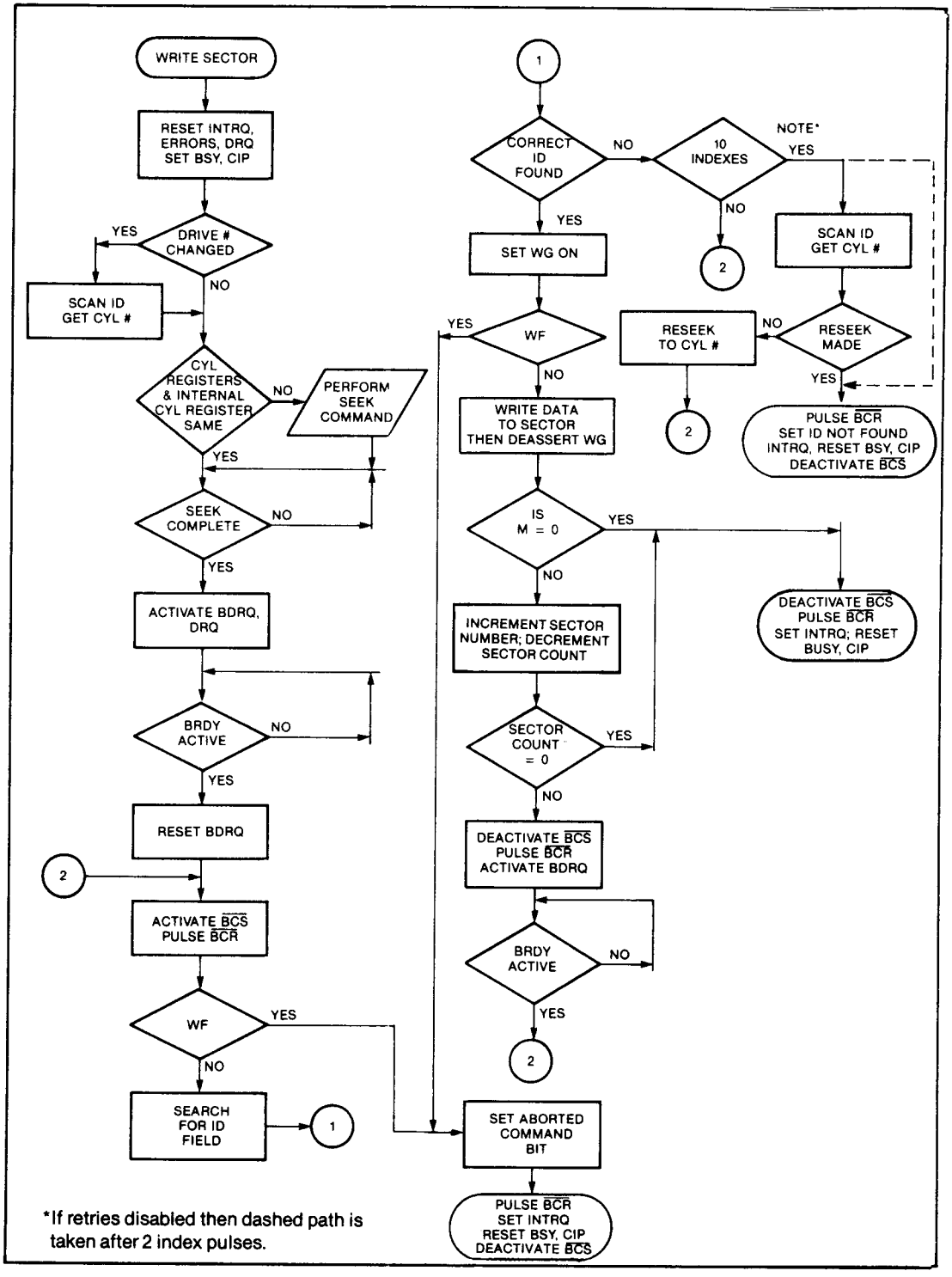
WRITE SECTOR

The write sector command is used to write one or more sectors of data to the disk. Upon receipt of this command, the WD1010-05 checks the cylinder registers against its internal cylinder position register to see if they are the same. If not, the direction and number of steps are calculated and a seek command takes place. Write fault and DRDY lines are checked throughout the command.

After Seek complete is found to be true (with or without an implied seek), the BDRQ signal is made active and the host proceeds to load the buffer. When the WD1010-05 senses the BRDY line going high, the ID field with the specified cylinder, head, and sector size is searched for. Once found, the write gate signal is raised and the data is written to the disk. It is necessary to resynchronize the write data due to the fact that a bit cell can extend from 295ns to 315ns during a write cycle. If retries are disabled and if the ID field cannot be found within 2 revolutions, the ID not found bit is set and the command is terminated.

If retries are enabled, and the ID field cannot be found within 10 revolutions, an automatic scan ID and seek commands are performed. The ID Not Found error bit is set if the ID field is not found after 10 more revolutions.

During a multiple sector write operation (M flag = 1), the sector number is incremented and the sector count register is decremented. If the BRDY lines is asserted after the first sector is read out of the buffer, the WD1010-05 will continue to read data out of the buffer for the next sector. If BRDY is inactive, the WD1010-05 will raise BRDQ and wait for the host to place more data in the buffer.


WRITE SECTOR
RESET INTRQ, ERRORS, DRQ SET BSY, CIP
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
CYL REGISTERS & INTERNAL CYL REGISTER SAME
NO
PERFORM SEEK COMMAND
YES
SEEK COMPLETE
NO
YES
ACTIVATE BDRQ, DRQ
BRDY ACTIVE
NO
YES
RESET BDRQ
2
ACTIVATE BCS PULSE BCR
WF
YES
NO
SEARCH FOR ID FIELD
1
1
CORRECT ID FOUND
NO
10 INDEXES
NOTE*
YES
NO
2
SCAN ID GET CYL #
YES
SET WG ON
WF
YES
NO
RESEEK TO CYL #
NO
RESEEK MADE
YES
2
PULSE BCR SET ID NOT FOUND INTRQ, RESET BSY, CIP DEACTIVATE BCS
WRITE DATA TO SECTOR THEN DEASSERT WG
IS M = 0
YES
NO
DEACTIVATE BCS PULSE BCR SET INTRQ; RESET BUSY, CIP
INCREMENT SECTOR NUMBER; DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
DEACTIVATE BCS PULSE BCR ACTIVATE BDRQ
BRDY ACTIVE
NO
YES
2
SET ABORTED COMMAND BIT
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
*If retries disabled then dashed path is taken after 2 index pulses.

In summary then, the write sector operation is as follows:

(1)	Host:	Sets up parameters; issues write sector command.
(2)	1010:	Sets BDRQ = 1. DRQ flag = 1.
(3)	Host:	Loads buffer with data (by WE strobes).
(4)	1010:	Waits for BRDY = low to high.
(5)	1010:	Finds specified ID field, write out sector.
(6)	1010:	If M = 0, then interrupt; End.
(7)	1010:	Increments sector number, decrements sector count.
(8)	1010:	If sector count = 0, then interrupt; End.
(9)	1010:	Go to (2).

SCAN ID

The scan ID command is used to update the head, sector size, sector number and cylinder registers.

The ready and write fault lines are checked throughout the command. When the first ID field is encountered, the ID information is loaded into the SDH, cylinder, and sector number registers. The internal cylinder position register is also updated. If a bad block is detected, the bad block bit will also be set. CRC is checked and if an error is found, the WD1010-05 will retry up to 10 revolutions to find an error-free ID field. There is no implied seek with this command and the buffer is left undisturbed.

FORMAT

The format command is used to format one track using the task file and the sector buffer. During this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 7 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. A 00 is normal; an 80 hex indicates a bad block mark for that sector. In the example of Figure 7, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY to tell the WD1010-05 to begin formatting the track.

An implied seek is also in effect on this command. As in other commands, if the drive number has changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incompatible format had been used), an IDNF error will result and the Format command will be aborted. This can be avoided by issuing a Restore command before formatting.

The sector count register is used to hold the total number of sectors to be formatted, while the sector number register holds the number of bytes minus 3 to be used for Gap 1 and Gap 3. For instance, if the sector count register value is 2 and the sector number register value is 0, then 2 sectors are written and 3 bytes of 4E hex are written for Gap 1 and Gap 3. The data fields are filled with FF hex, and CRC is automatically generated and appended. The sector extension bit of the SDH register should not be set. After the last sector is written, 4E hex is filled until index.

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining

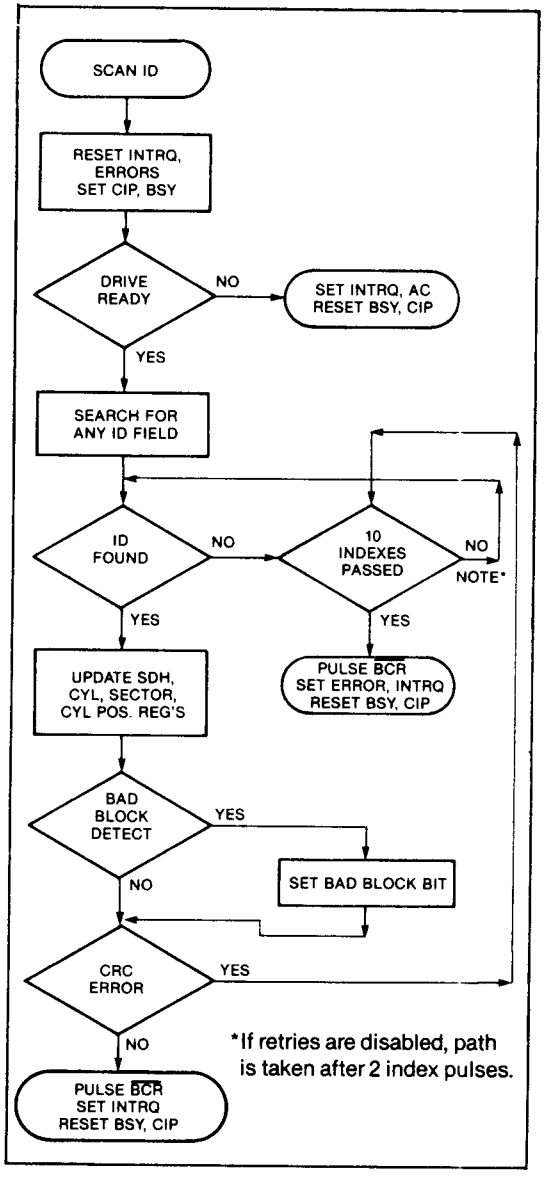
	DATA							
ADDR	0	1	2	3	4	5	6	7
00	00	00	00	10	00	01	00	11
08	00	02	00	12	00	03	00	13
10	80	04	00	14	00	05	00	15
18	00	06	00	16	00	07	00	17
20	00	08	00	18	00	09	00	19
28	00	0A	00	1A	00	0B	00	1B
30	00	0C	00	1C	00	0D	00	1D
38	00	0E	00	1E	00	0F	00	1F
40	FF	FF	FF	FF	FF	FF	FF	FF
:				:				
:				:				
F0	FF	FF	FF	FF	FF	FF	FF	FF

FIGURE 7.
FORMAT COMMAND BUFFER CONTENTS

the minimum Gap 3 value is:

Gap 3 = 2*M*S + K + E
M = motor speed variation (e.g., .03 for ± 3%)
S = sector length in bytes
K = 25 for interleave factor of 1
K = 0 for any other interleave factor
E = 7 if the sector is to be extended

Like all commands, a write fault or not ready condition will terminate the command. Figure 8 shows the format that the WD1010-05 will write on the Disk.



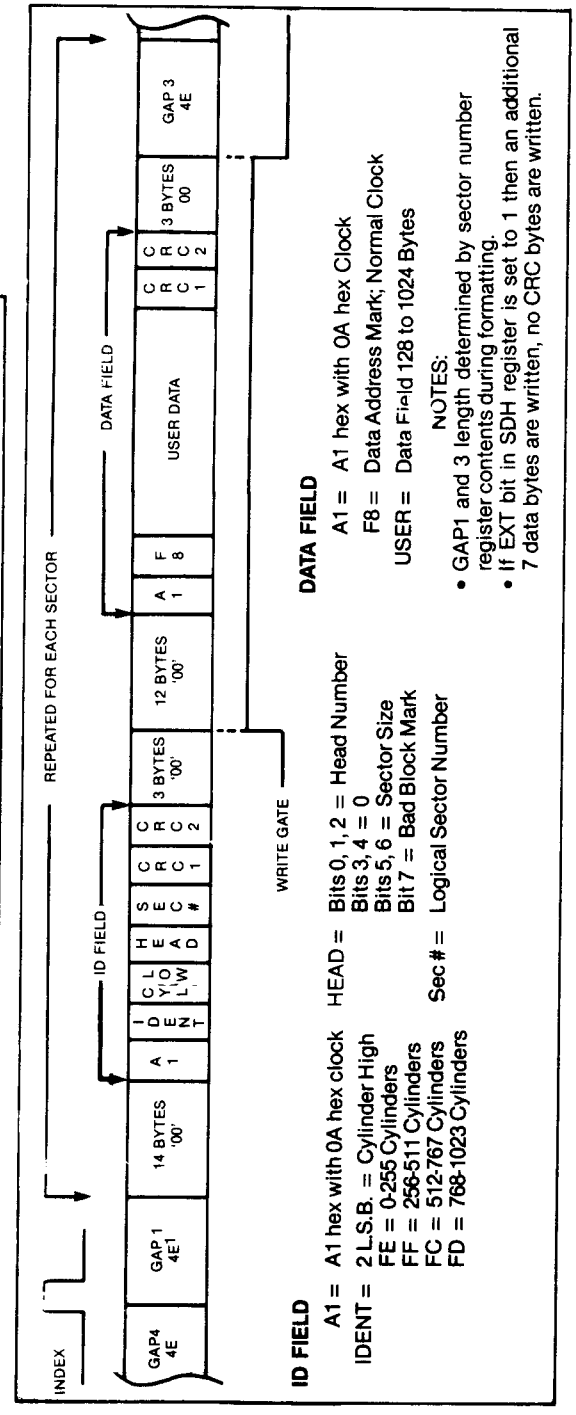
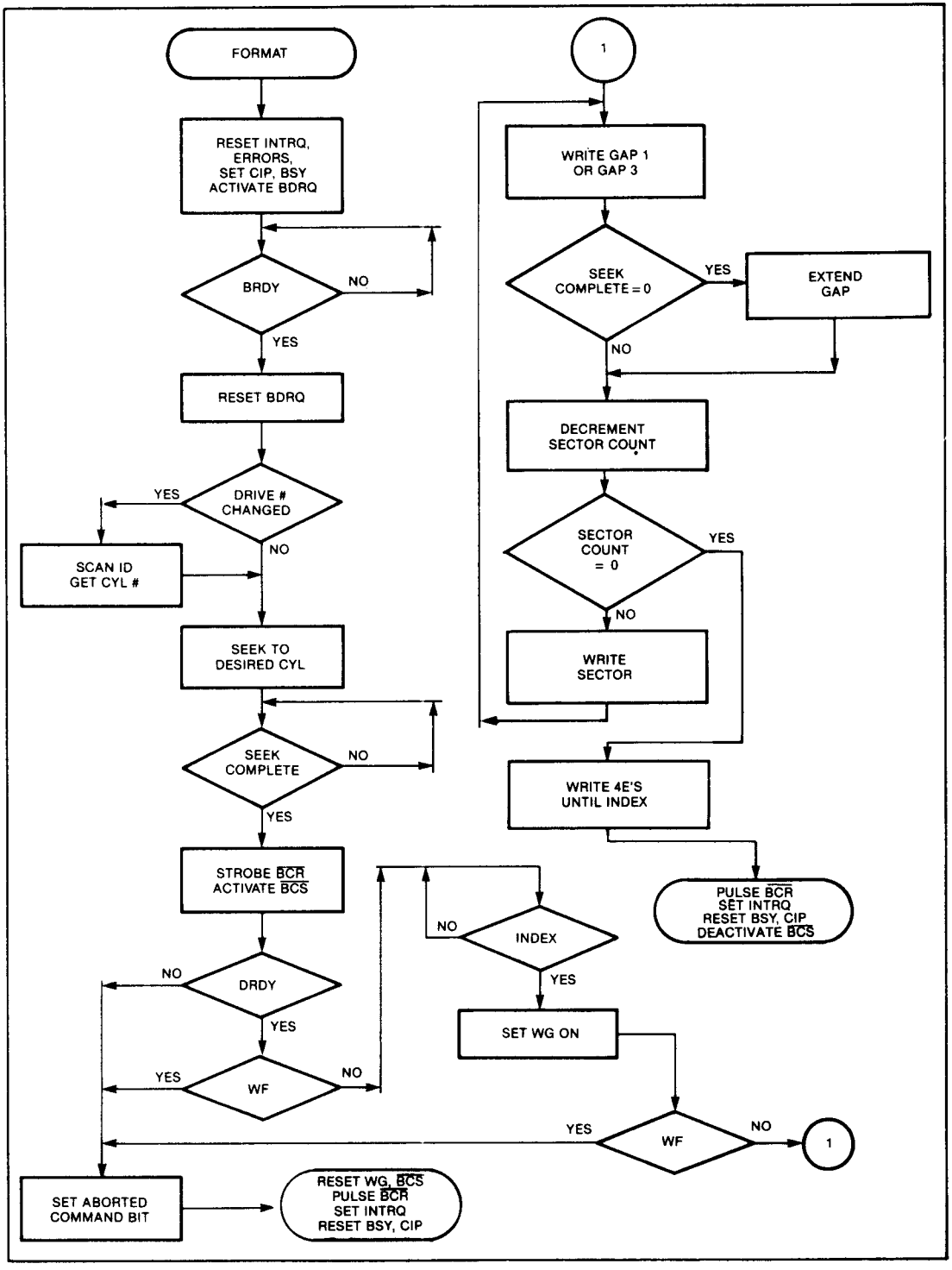


FIGURE 8.
FORMAT


FORMAT
RESET INTRQ, ERRORS, SET CIP, BSY ACTIVATE BDRQ
BRDY
NO
YES
RESET BDRQ
DRIVE # CHANGED
YES
NO
SCAN ID GET CYL #
SEEK TO DESIRED CYL
SEEK COMPLETE
NO
YES
STROBE BCR ACTIVATE BCS
DRDY
NO
YES
WF
YES
NO
SET ABORTED COMMAND BIT
RESET WG, BCS PULSE BCR SET INTRQ RESET BSY, CIP
1
WRITE GAP 1 OR GAP 3
SEEK COMPLETE = 0
YES
EXTEND GAP
NO
DECREMENT SECTOR COUNT
SECTOR COUNT = 0
YES
NO
WRITE SECTOR
WRITE 4E'S UNTIL INDEX
PULSE BCR SET INTRQ RESET BSY, CIP DEACTIVATE BCS
INDEX
NO
YES
SET WG ON
WF
YES
NO
1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

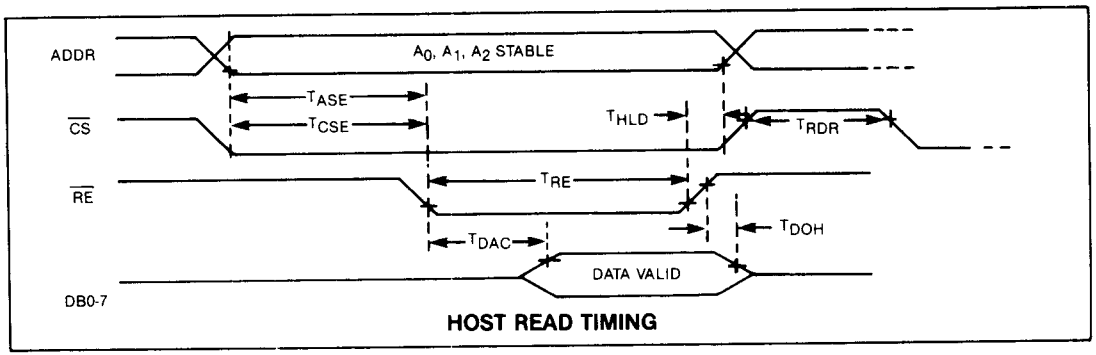
V_{CC} with respect to V_{SS} (Ground) . . . . . +7V
Max Voltage on any Pin with
respect to V_{SS} . . . . . -0.5V to +7.0V
Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -55°C to +125°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = 0V, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	μA	V_{IN} = .4 to V_{CC}
I_{OL}	Output Leakage (Tristate & Open Drain)		±10	μA	V_{OUT} = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = -100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6mA
V_{OL}	Output Low Voltage(Pins 21-23)		0.45	V	IO = 4.8mA See Note 10
I_{CC}	Supply Current		200	mA	All Outputs Open
	For Pins 25, 34, 39:				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise and Fall Time		30	nsec	.9V to 4.2V points
C_{IN}	Input Capacitance		15	pF	

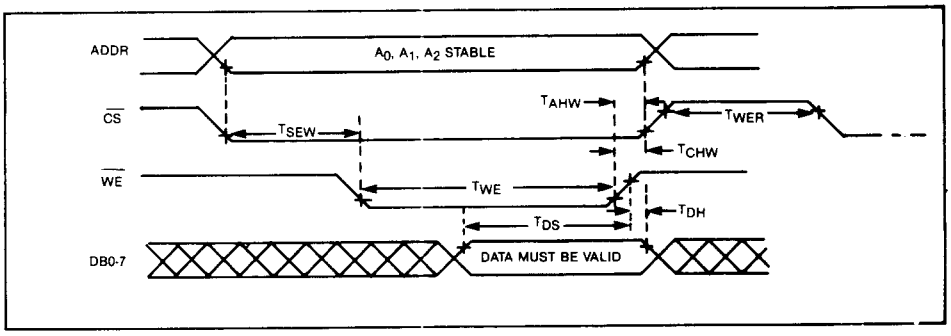
AC Timing Characteristics T_A = 0°C to 50°C; V_{SS} = 0V, V_{CC} = +5V ±.25V



HOST READ TIMING

HOST READ TIMING WD1010-05 WC = 5 MHZ

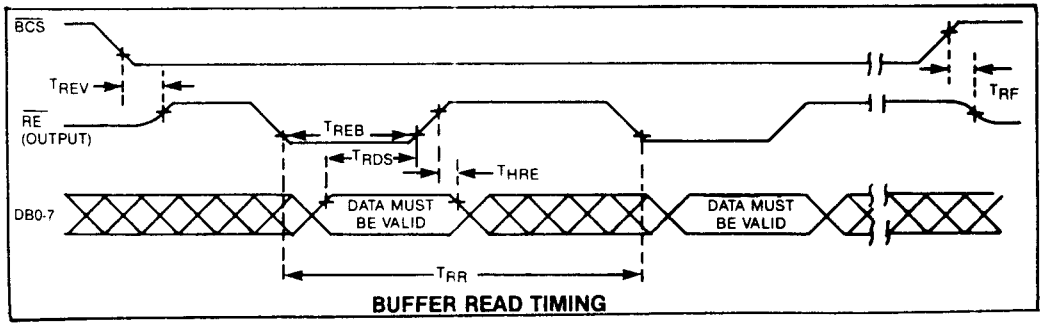
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITION
T_{ASE}	ADDR Setup to $\overline{RE}$	100		nsec	
T_{DAC}	Data Valid from $\overline{RE}$		375	nsec	
T_{RE}	Read Enable Pulse Width	.4	10	μsec	
T_{DOH}	Data Hold from $\overline{RE}$	20	200	nsec	
T_{HLD}	ADDR, $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
T_{RDR}	Read Recovery Time	300		nsec	
T_{CSE}	$\overline{CS}$ Setup to $\overline{RE}$	0		nsec	See Note 8



HOST WRITE TIMING

HOST WRITING TIMING WD1010-05

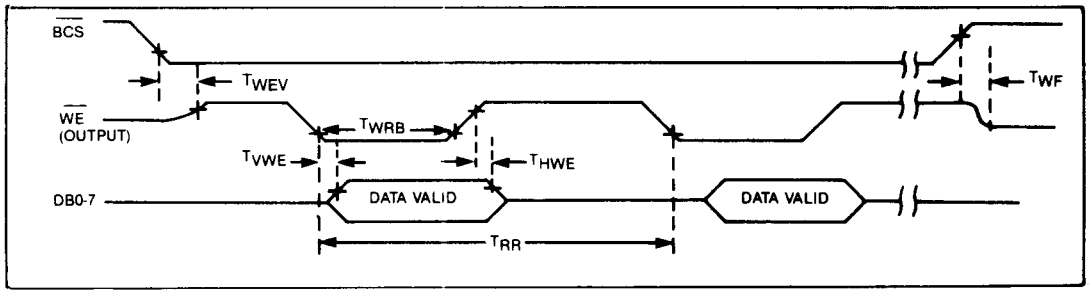
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITION
T_{SEW}	ADDR, $\overline{CS}$ Setup to $\overline{WE}$	0	10	μsec	
T_{DS}	Data Bus Setup to $\overline{WE}$	.2	10	μsec	
T_{WE}	Write Enable Pulse Width	.2	10	μsec	
T_{DH}	Data Bus Hold from $\overline{WE}$	10		nsec	
T_{AHW}	ADDR Hold from $\overline{WE}$	30		nsec	
T_{WER}	Write Recovery Time	1.0		μsec	See Note 1
T_{CHW}	$\overline{CS}$ Hold Time from $\overline{WE}$	0			See Note 9



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD) WD1010-05 WC = 5MHZ

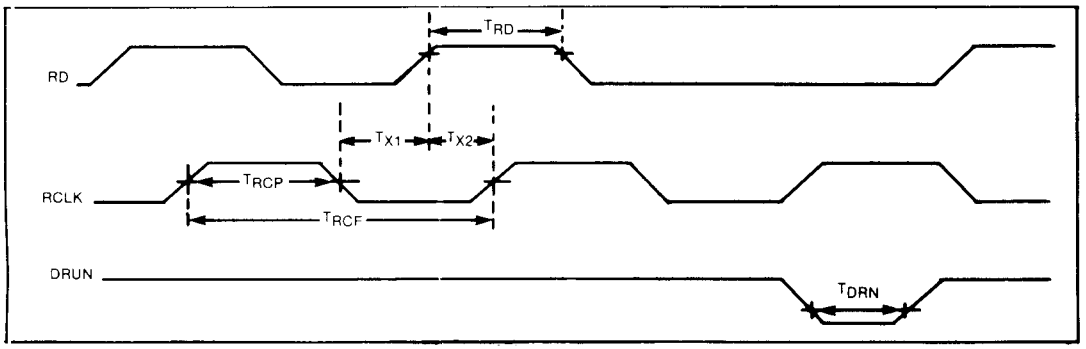
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{REV}	$\overline{RE}$ Float to $\overline{RE}$ Valid	15		100	nsec	C_L = 50 pf
T_{REB}	$\overline{RE}$ Output Pulse Width	300	400	500	nsec	See Note 4
T_{RDS}	Data Setup to $\overline{RE}$	140			nsec	
T_{RR}	$\overline{RE}$ Repetition Rate	1.2	1.6	2.0	μsec	
T_{RF}	$\overline{RE}$ Float from $\overline{BCS}$			100	nsec	C_L = 50 pf
T_{HRE}	Data Hold from $\overline{RE}$	0			nsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD) WD1010-05 WC = 5 MHZ

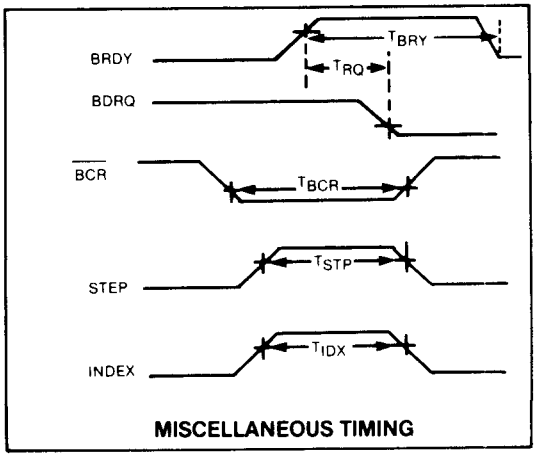
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WEV}	$\overline{WE}$ Float to $\overline{WE}$ Valid	15		100	nsec	C_L = 50 pf
T_{WRB}	$\overline{WE}$ Output Pulse Width	300	400	500	nsec	See Note 4
T_{VWE}	Data Valid from $\overline{WE}$			150	nsec	
T_{HWE}	Data Hold from $\overline{WE}$	60			nsec	
T_{RR}	$\overline{WE}$ Repetition Rate	1.2	1.6	2.0	μsec	See Note 2
T_{WF}	$\overline{WE}$ Float from $\overline{BCS}$	15		100	nsec	C_L = 50 pf



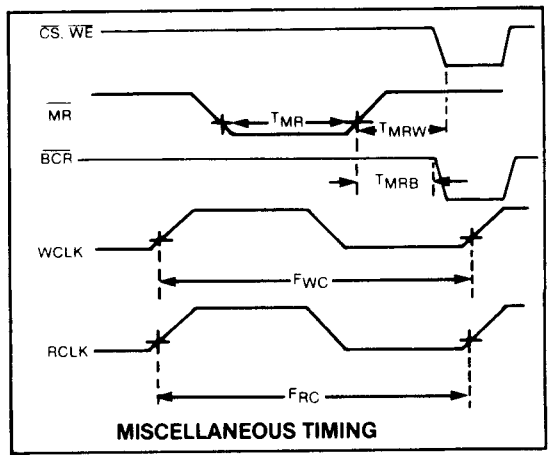
READ DATA TIMING

READ DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RCP}	RCLK Pulse Width	95		2000	nsec	50% Duty Cycle
T_{X1}	RD from RCLK Transition	0		T_{RCP}	nsec	
T_{X2}	RD to RCLK Transition	20		T_{RCP}	nsec	
T_{RD}	RD Pulse Width	40		T_{RCP}	nsec	
T_{DRN}	DRUN Pulse Width	30			nsec	
T_{RCF}	RCLK Frequency	.250		5.25	MHz	See Note 6



MISCELLANEOUS TIMING

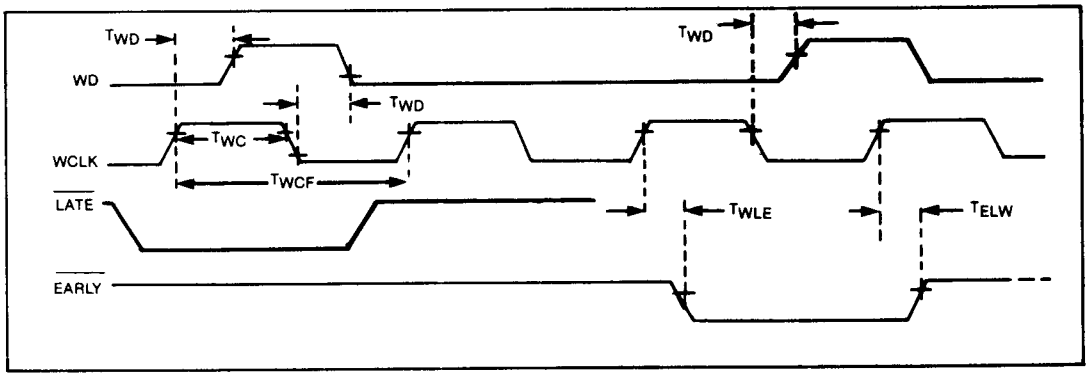


MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{RQ}	BDRQ Reset from BRDY	40		200	nsec	
T_{BCR}	Buffer Counter Reset Pulse Width	1.4	1.6	1.8	μsec	See Note 2
T_{STP}	Step Pulse Width	8.3	8.4	8.7	μsec	See Note 2
T_{IDX}	Index Pulse Width	500			nsec	
T_{MR}	Master Reset Pulse Width	24			WC	See Note 3
F_{WC}(-05)	Write Clock Frequency	.25	5.0	5.25	MHz	50% Duty Cycle
F_{RC}(-05)	Read Clock Frequency	.25	5.0	5.25	MHz	See Note 6
T_{BRY}	BRDY Pulse Width	800			nsec	See Note 5
T_{MRB}	$\overline{MR}$ Trailing to $\overline{BCR}$	1.6	3.2	6.4	μsec	See Note 2
T_{MRW}	$\overline{MR}$ Trailing to Host Write	6.4			μsec	See Note 2

NOTES:
1. AC timing measured at V_{OH} = 2.0V, V_{OL} = 0.8V, C_L = 50 pf.
2. Based on WCLK = 5.0 MHz.
3. 24 WCLK periods (4.8 μsec at 5.0 MHz).
4. 2 WCLK ± 100 nsec.
5. To drive a DMA controller, BRDY must be >4 μsec or a spurious BDRQ pulse may exist for up to 4 μsec after rising edge of BRDY.
6. T_{RCF} = T_{WCF} ± 15%.
7. 2 WCLK ± 50 nsec.
8. $\overline{RE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{RE}$ meets the TRE width.
9. $\overline{WE}$ may precede $\overline{CS}$ if $\overline{CS}$ plus $\overline{WE}$ meets the TWE width.
10. Pins 21-23 should be loaded with a 1K pull-up resistor.



WRITE DATA TIMING

WRITE DATA TIMING WD1010-05 WC = 5 MHZ

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
T_{WC}	WCLK Pulse Width	95		2000	nsec	
T_{WD}	Propagation Delay WCLK to WD	10		65	nsec	
T_{WLE}	WCLK to Leading Early/Late	10		65	nsec	
T_{ELW}	WCLK to Trailing Early/Late	10		65	nsec	
T_{WCF}	WCLK Frequency	.250		5.25	MHz	See Note 6

WD1010 Application Notes

FLEXIBLE CONTROLLER MATES WITH POPULAR WINCHESTER DRIVES

To take advantage of the growing demand for Seagate Technology-type 5 1/4-in. Winchester disk drives in personal computers, electronic work stations, and small-business systems, designers need an appropriate controller that is inexpensive. In fact, today's designs must implement the control link between a Host CPU and a disk drive at far lower cost than the drive itself. That requires a single-chip controller rather than discrete, gate-array-intensive circuits that take up valuable board space in ever smaller computer equipment.

Such a device is now available in the form of an LSI single-chip Winchester controller-formatter. The chip incorporates 80% of the circuitry required for Winchester control, eliminating between 50 and 75 SSI and MSI devices used in earlier designs.

A controller that claims Seagate compatibility must be sufficiently flexible to meet not only the company's original ST506 specifications, but also the various deviations from them. The basic specifications include a data rate of 5.0 Mbits/s and open-collector outputs and differential signal inputs for the separate control and data interface cables. The recording format is modified frequency modulation (MFM), but more importantly, the structure of the format defines both specific address-mark bytes and ID fields. These are fixed specifications, but manufacturers of Seagate-type drives sometimes make other changes. For example, the track density on high-capacity drives may be greater than that in the original ST506 specification. Also, the number of sectors and bytes per sector on each cylinder can vary according to the application. In each case, a compatible controller must be able to handle the original specifications plus the deviations.

The ST506 interface is a spinoff of the Shugart Associates SA1000 drive, first introduced in 1979. Two important differences between the interfaces are the data rates and a timing-clock differential signal on the SA1000. The latter operates at 4.34 Mbits/s vs 5 Mbits/s for the ST506, but the remaining signals have enough similarity to permit a single controller design to run either an 8-in. SA1000 drive or the 5 1/4-in. ST506 drive. The advantage of the WD1010 Winchester controller-formatter is that it works with either and with other manufacturers' variations as well.

Operation of the drive begins when a Host processor initiates a command after first loading a set of internal task registers called the task file. Information such as cylinder, sector, and head number is written to these registers, which are selected by address lines. The memory-mapped register scheme allows individual accesses to each register. Thus, the Host need not waste valuable time reading all the registers to obtain a specific parameter.

The WD1010, which comes in a 40-pin DIP or 44-pin QSM, is run by an internal microcontroller – a PLA (programmable logic array) serving as a state machine (Fig. 1). This logic controls the flow of data throughout the chip, recognizes and processes commands, and formats the data.

WRITING AND READING DATA

During a write operation, parallel data is read from the data bus and written to a specific sector. But first the cylinder and sector must be located on the requested disk drive. The WD1010's microcontroller accesses its internal cylinder-position data and compares it with the requested cylinder number. If necessary, a seek is performed automatically to position the head assembly over the desired cylinder.

If the drive requested is changed before a Seek Command is executed, the WD1010 enables its read logic and searches for an ID field on the currently selected drive. Then it reads the cylinder number for the new ID field and determines whether to seek in or out to find the requested cylinder. This so-called implied seek is a feature of all commands (see "Macro Commands Provide Multiple Options").

After the WD1010 finds an ID field that matches the cylinder, head, sector, sector size and CRC (cyclic redundancy check) value, it writes a field of 0s and a new address mark – later these two fields will be used for synchronization during a read operation. The chip then reads parallel data in from the data bus, serializes it, and converts it into the MFM format. Next, a new CRC value is calculated for the incoming data and is appended to the data field (after the last byte). If the original command specifies multiple sectors, the next logical sector must be searched for and the process repeated. After the last sector is written, the WD1010 gives the bus back to the Host and waits for the next command.

Although the chip does not generate an error correction signal, an optional command bit can be set to disable cyclic redundancy checks of the data field. The sector is extended by seven bytes to allow the Host to write its 56-bit error detection and correction code. Later, during a read operation, these seven bytes are transferred back to the Host to permit it to identify a syndrome and correct any errors that were encountered. For systems that require such operations, the WD1014 error detection and correction and

WD1015 buffer controller chips are available.

Reading is similar to writing except that data is sent out on the data bus and written into the sector buffer at the Host. MFM data is entered on the RD pin along with a synchronous clock (RCLK) generated from an external data separator (Figure 2).

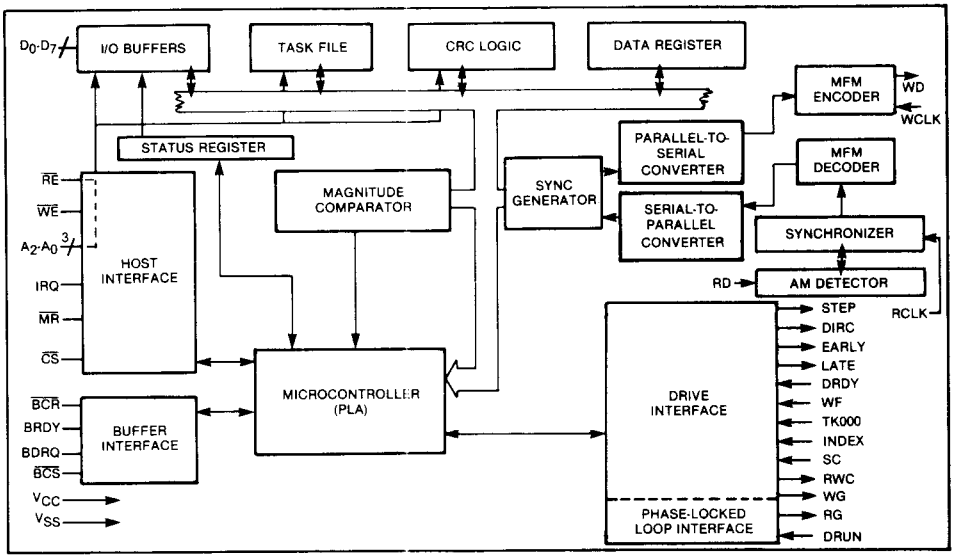


Figure 1.

The architecture of the WD1010 Winchester controller-formatter chip is designed to reduce a Host processor's overhead burden. An internal microcontroller (PLA) manages data flow, incoming commands, and formatting.

Since the data rate is relatively high, the data separator must instruct the controller to lock on to the incoming data stream only during a field of 1s and 0s. A Data Run (DRUN) signal to the WD1010 indicates such an occurrence. When DRUN is active, the WD1010 counts off 16 bits – 2 byte time – sets the Read Gate (RG) signal, and starts to search the data stream for an address mark.

IMPLEMENTING THE PRECOMPENSATION ALGORITHM				
ALREADY SENT		SENDING	TO BE SENT	SHIFT REQUIRED
X	1	1	0	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

NOTE: All other patterns produce no shift.

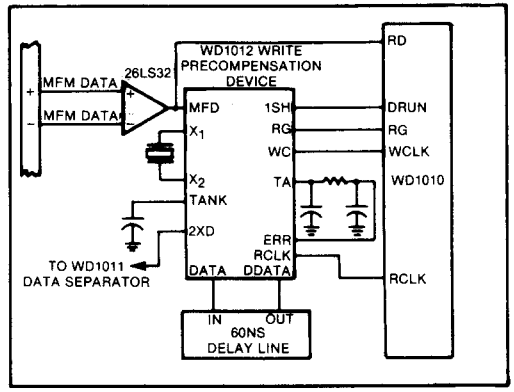


Figure 2.

A separate IC – the WD1012 – performs the data separation for the WD1010. The data separator sends a DRUN signal to the controller when it encounters a data field (1s and 0s).

An address mark is a unique pattern of clock and data bits that does not appear in any place that normal MFM data appears. If an address mark is not detected within nine bytes or if a non-0 pattern is detected within nine bytes, RG is turned off and the search is repeated. Since the data fields within sectors can contain 0s or all 1s, the DRUN algorithm is also triggered in these cases. But the address mark will not be detected, preventing erroneous data from being transferred.

After the ID field is compared and verified, a search begins for the address mark. Resynchronization occurs and the data is transferred to an internal MFM-to-NRZ converter. Data is then shifted through a double-buffered shift register and placed on the data bus for loading to the buffer. Either the cyclic redundancy code at the end of the data field is checked or the error detection and correction bytes are transferred in parallel to the host, depending on which option is used. Then the host processor can read the data from its local buffer.

Like all magnetic recording media, Winchester disks are not immune to the effects of bit shifts at high recording densities. The WD1010 uses an algorithm that informs external delay circuits when to shift outgoing data. A register within the task file specifies which cylinder receives reduced write current and if precompensation is needed. Typically, both occur on the same cylinder about half way down the disk surface.

The WD1010's precompensation signals are called $\overline{\text{Early}}$ and Late. Depending on the bit pattern leaving the device, data will be shifted early, late, or not at all. The WD1011 data separator implements the precompensation delay network (Figure 2).

Since the $\overline{\text{Early}}$ signal and the current data (or clock) bits leaving the WD1010 have already occurred, the WD1011 performs no delay function on $\overline{\text{Early}}$. If both $\overline{\text{Early}}$ and Late are inactive, the WD1011 inserts a 12-ns delay; if only Late is active, it inserts a 24-ns delay. The result is a ± 12-ns shift of the data from its nominal position. An inactive Reduced Write Current (RWC) signal from the WD1010 disables the WD1011. The WD1010 then furnishes precompensation signals independent of current cylinder position.

INTERFACING WITH CABLES AND BUSES

The remaining function on the drive side is to provide sufficient buffers to drive the cables between the chip and the interface connectors. Single-ended open-collector signals are used for the control cable, and differential receiver-drivers are used for the data cable (Figure 3). Each line must have such buffers, since the controller is designed to drive one TTL load on all inputs and outputs.

At a 5-Mbit/s data transfer rate to the host interface, a byte of data must be read every 1.6 μs – in 8-bit parallel form. Few microprocessors can access a port and check status within this period. Consequently, a design objective of the WD1010 is compatibility with a programmed I/O environment, as well as the support of off-line error detection and correction. Moreover, the chip can transfer multiple sectors on one command. To achieve such performance within the constraints of a 40-pin package, the WD1010 relies on a unique approach to the traditional peripheral interface.

Three modes of communication can exist at the host interface: between the host and the WD1010, between the host and the buffer, and between the WD1010 and the buffer. For the host-WD1010 communication the

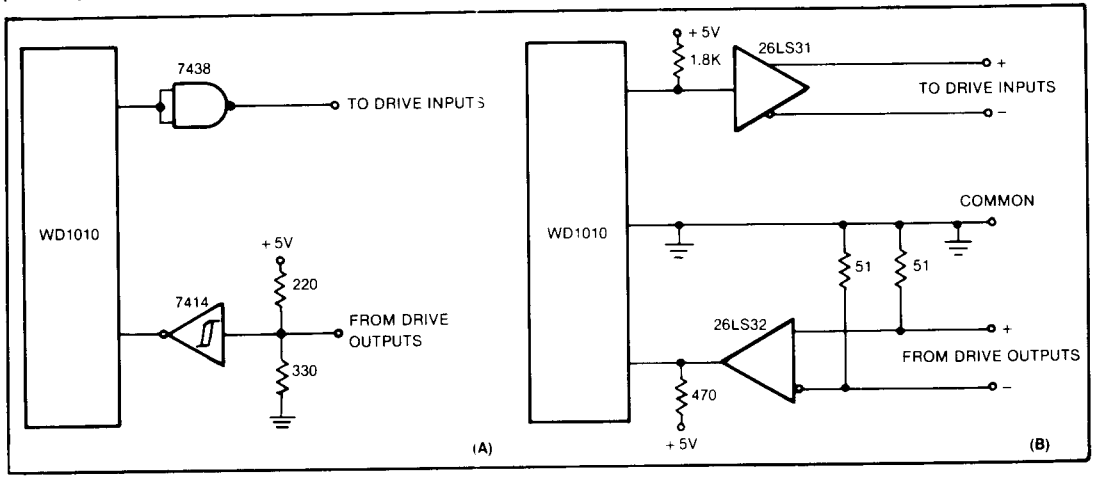


Figure 3.

Buffering circuits from the WD1010 to the control cable (A) and the data cable (B) must be used because the controller has a rather limited drive capability (one TTL load each on inputs and outputs).

chip, like many microprocessors, talks over an 8-bit bi-directional bus, plus Read, Write and chip select lines (Figures 4,5). Three address lines access registers within the chip.

In host-buffer or WD1010-buffer communications (Figures 4,5), when the chip reads or writes to the buffer, the Buffer Chip Select (BSC) line is pulled low. This signal should be used to disconnect the host data bus and Read and Write lines from the WD1010.

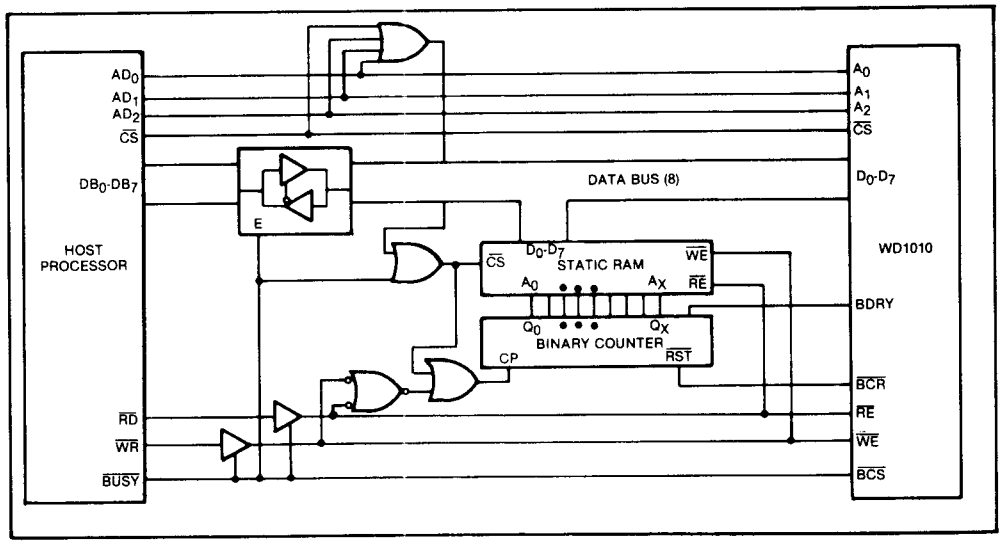


Figure 4.

Communications between a host and the WD1010 can be effected with the static RAM and binary counter circuitry shown in Figure 4. These devices form a sector buffer that stores data sent from the host or the controller. This hardware handles both read and write operations on multiple sectors.

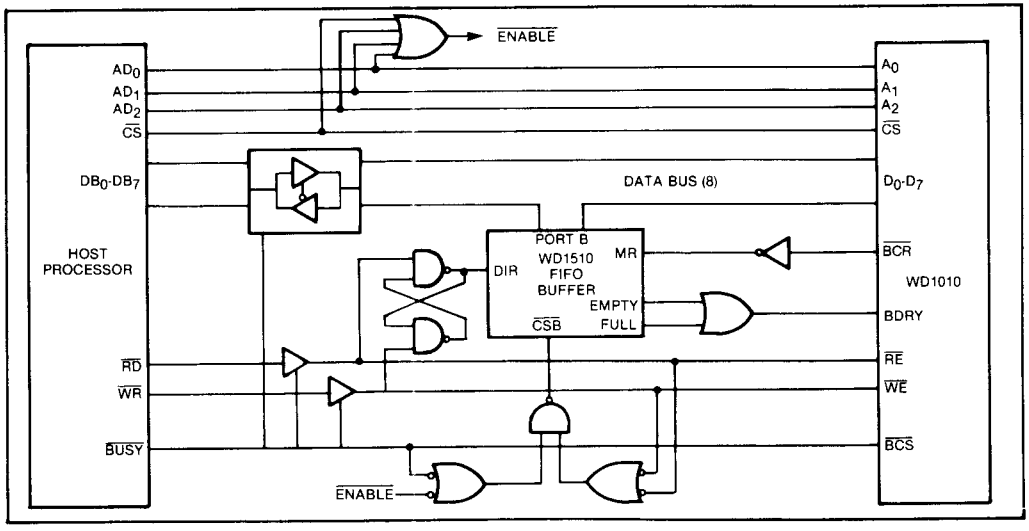


Figure 5.

A variation on the circuit of Figure 4. uses a WD1510 FIFO buffer to replace the counter-RAM circuitry. The scheme works well at high throughput rates since the buffer need not be filled to transfer data supplied by the WD1010 to the host.

The Read ($\overline{RE}$) and Write ($\overline{WR}$) lines become outputs from the WD1010 and are strobed as each byte is placed on the bus.

The sector buffer in Figure 4 is implemented with a binary counter and a static RAM. With each RE or WE probe, the counter is incremented so that the following byte can be read from or written to the next sequential location in the RAM. After all memory locations are written to, a carry signal from the counter goes to the Buffer Ready (BRDY) line of the WD1010. This signal informs the controller that the counter has rolled over and that the buffer is either full or empty, depending on the command.

During multiple-sector transfers, the RAM can be as large as the available sectors on each cylinder. The controller continues to load the RAM with data when a sector is being read. When no more memory is available, BRDY signals the WD1010. The command will then pause, wait for the host to dump the memory, and then begin filling the RAM again. This scheme permits both read and write operations on multiple sectors.

Signals for host and buffer control include the Buffer Counter Reset (BCR) line, which is pulsed when $\overline{BCS}$ makes an active transition. BCR resets the binary counter before a read or write operation. Since address location 000 does not exist in the WD1010, a decoder can be used to make this address location enable the RAM and simulate a data register. For DMA applications, the Buffer Data Request (BRDQ) line is activated when data is available for host use.

Numerous other methods can be used with these same control signals. For example, a first-in, first-out buffer (Figure 5) can replace the counter-RAM. In this scheme, the host can dump data before the WD1010 fills the buffer. With sufficient throughput, the FIFO buffer need not have the storage capacity of an entire sector if the host can empty it quickly enough with a burst mode. In that case, the BRDY signal becomes the OR function of the Empty and Full signals from the FIFO buffer.

MACRO COMMANDS PROVIDE MULTIPLE OPTIONS

Each of the WD1010 Winchester controller-formatter's six macro commands contains several option flags. These flags allow the selection of stepping rates, multiple-sector transfers, and interrupt timing. The WD1010's task file contains additional options that are programmed before the command is actually issued. The operations of each command are as follows:

Restore causes the read/write head assembly to move to track 000. The stepping rate is determined by the state of Seek Complete (pin 32), which is activated by the drive to indicate its readiness. The stepping rate specified in the Restore Command is not actually used but retained internally for an implied track later on.

Activation of Seek causes a seek operation for any desired cylinder. The selected cylinder is loaded into the cylinder register. Then the controller decides which way to seek and how many steps to use. The Seek Complete line is not checked, making possible overlapping seek operations on several drives.

The actual transfer of data from the WD1010 to sector buffer is performed under the Read Sector command. This command also causes a search for the specified cylinder, drive, head, and sector. Multiple sectors are specified and enabled through the sector count register. If the multiple-option flag is set, the number of sectors specified are transferred to the buffer.

Data in the sector buffer is written on the disk under the Write Sector command. Like the Read Sector command, it specifies and enables multiple drives through the sector count register.

Both the Read and Write Sector commands will retry up to eight times before automatically performing a restore operation. After a restoration, the controller seeks out the marginal sector and tries to determine whether an error condition was caused by a mispositioning of the head or a problem in the actuator.

The Format command is used to initialize a track with ID fields, gaps, and all information necessary for subsequent read and write operations. The sector buffer plays a unique role in this command, since it provides information on error mapping and interleaving rather than data from a sector. The order in which each sector is to be recorded is specified in the buffer, together with information indicating whether a sector contains a bad block or an error flag. Gap sizes, number of sectors, and other information are specified in the task file to allow further control over the format. By incrementing the cylinder number register, an entire surface can be formatted by accessing just two registers.

THE WD1010'S MACRO COMMANDS

	CODE							
	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R_3	R_2	R_1	R_0
Seek	0	1	1	1	R_3	R_2	R_1	R_0
Read Sector	0	0	1	0	1	M	0	0
Write Sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0

M = Multiple Sector Flag

M = 0 - transfer 1 sector
M = 1 - transfer multiple sectors

I = Interrupt Enable

I = 0 - interrupt at BDRQ time
I = 1 - interrupt at end of command

A MULTIPLE-DRIVE SYSTEM

For multiple drive-head configurations, the WD1010's sector-drive-head (SDH) register is decoded at address 110 to produce individual, latched drive-selection signals whenever the host writes to this address location. Binary head selection does not require a separate decoder, since one is located at the drive.

When the WD1010 senses a change in drive number, it automatically reads a cylinder. This takes place before the execution of the current command. The chip records the new cylinder number it has read and stores it internally as a reference for future seek operations on the current drive.

After the execution of any command, the WD1010 informs the host processor of any errors encountered during execution. On-board status and error registers report error conditons and signal status from the drive. To eliminate tedious error detection procedures, the host processor need only check the error bit in the status register to determine whether any bits are set in the error register.

Bit 0 of the status register is set if any of 5 bits in the 8-bit error register are set – bit 0 establishes the logical OR of the status register. Other error indicators include a Bad Block Detect bit, which is activated when an ID field contains a bad block mark, and an ID Not Found bit, which is set when the desired cylinder, head, sector, or size parameter is not found after 16 revolutions of the disk. The latter is also set if the data address mark of the data field is incorrect when a read is executed.

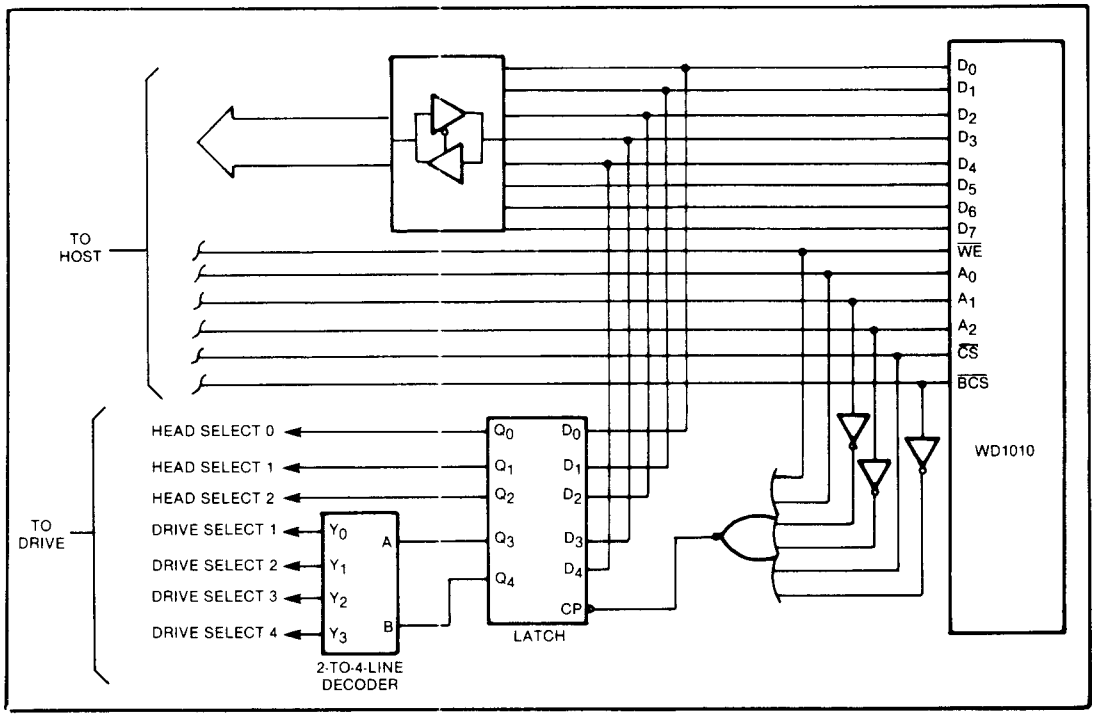


Figure 6.

Four Winchester drives can be controlled by the WD1010 using an external latch and a 2-to-4-line decoder. If the drive being accessed changes, the controller performs an automatic read operation. It records the cylinder number of the read for future seeks.