

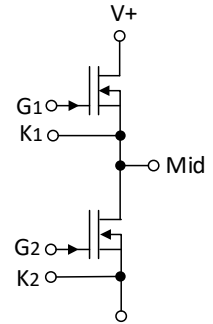
WAB400M12BM3

1200 V, 400 A All-Silicon Carbide
THB-80 Qualified, Conduction Optimized, Half-Bridge Module

V_{DS}	1200 V
I_{DS}	400 A

Technical Features

- Industry Standard 62 mm Footprint
- High Humidity Operation THB-80 (HV-H3TRB)
- High Junction Temperature (175 °C) Operation
- Implements Conduction Optimized Third Generation SiC MOSFET Technology
- Low Inductance (10.2 nH) Design
- Silicon Nitride Insulator and Copper Baseplate



Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Fast Time-to-Market with Minimal Development Required for Transition from 62 mm Si IGBT Packages
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	$T_C = 25\text{ °C}$	
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-8		+19		Transient	Note 1
Gate-Source Voltage, Recommended	$V_{GS(op)}$		-4/+15			Static	Fig. 32
DC Continuous Drain Current	I_D		468		A	$V_{GS} = 15\text{ V}, T_C = 25\text{ °C}, T_{VJ} \leq 175\text{ °C}$	Notes 2, 3 Fig. 20
			353			$V_{GS} = 15\text{ V}, T_C = 90\text{ °C}, T_{VJ} \leq 175\text{ °C}$	
DC Source-Drain Current (Body Diode)	$I_{SD(BD)}$		262			$V_{GS} = -4\text{ V}, T_C = 25\text{ °C}, T_{VJ} \leq 175\text{ °C}$	
Pulsed Drain-Source Current	I_{DM}		800			t_{Pmax} limited by T_{VJmax} $V_{GS} = 15\text{ V}, T_C = 25\text{ °C}$	
Power Dissipation	P_D		1154		W	$T_C = 25\text{ °C}, T_{VJ} \leq 175\text{ °C}$	Note 4 Fig. 20
Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with $\pm 5\%$ regulation tolerance

Note (2): Current limit at $T_C = 90\text{ °C}$ calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)} - T_{D(max)}))}$

Note (3): Verified by design

Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

MOSFET Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	$V_{GS} = 0\text{ V}, T_{VJ} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 106\text{ mA}$	
			2.0			$V_{DS} = V_{GS}, I_D = 106\text{ mA}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		10	200	μA	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		0.04	1		$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		3.25	4.25	$\text{m}\Omega$	$V_{GS} = 15\text{ V}, I_D = 400\text{ A}$	Fig. 2 Fig. 3
			5.25			$V_{GS} = 15\text{ V}, I_D = 400\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Transconductance	g_{fs}		290		S	$V_{DS} = 20\text{ V}, I_{DS} = 400\text{ A}$	Fig. 4
			273			$V_{DS} = 20\text{ V}, I_{DS} = 400\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_J = 25\text{ }^{\circ}\text{C}$ $T_J = 125\text{ }^{\circ}\text{C}$ $T_J = 175\text{ }^{\circ}\text{C}$	E_{ON}		13.2 12.9 14.3		mJ	$V_{DS} = 600\text{ V},$ $I_D = 400\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(ext)} = 3.0\text{ }\Omega,$ $L = 13.6\text{ }\mu\text{H}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_J = 25\text{ }^{\circ}\text{C}$ $T_J = 125\text{ }^{\circ}\text{C}$ $T_J = 175\text{ }^{\circ}\text{C}$	E_{OFF}		11.3 12.0 12.6				
Internal Gate Resistance	$R_{G(int)}$		2.68		Ω	$T_{VJ} = 25\text{ }^{\circ}\text{C}$	
Input Capacitance	C_{iss}		29.7		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		1.18				
Reverse Transfer Capacitance	C_{rss}		62.5		pF		
Gate to Source Charge	Q_{GS}		308		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 400\text{ A}$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		380				
Total Gate Charge	Q_G		1040				
FET Thermal Resistance, Junction to Case	R_{thJC}		0.13	0.15	$^{\circ}\text{C}/\text{W}$		Fig. 17

Body Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Body Diode Forward Voltage	V_{SD}		5.4		V	$V_{GS} = -4\text{ V}, I_{SD} = 400\text{ A}$	Fig. 7
			4.9			$V_{GS} = -4\text{ V}, I_{SD} = 400\text{ A}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Reverse Recovery Time	t_{RR}		48.6		ns	$V_{GS} = -4\text{ V}, I_{SD} = 400\text{ A}, V_R = 600\text{ V}$ $di/dt = 10.0\text{ A/ns}, T_J = 175\text{ }^{\circ}\text{C}$	
Reverse Recovery Charge	Q_{RR}		7.6		μC		
Peak Reverse Recovery Current	I_{RRM}		265		A		
Reverse Recovery Energy $T_J = 25\text{ }^{\circ}\text{C}$ $T_J = 125\text{ }^{\circ}\text{C}$ $T_J = 175\text{ }^{\circ}\text{C}$	E_{RR}		0.36 1.33 2.28		mJ	$V_{DS} = 600\text{ V}, I_D = 400\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ext)} = 3.0\text{ }\Omega,$ $L = 13.6\text{ }\mu\text{H}$	Fig. 14



Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1	R ₃₋₁		0.60		mΩ	T _C = 125 °C, Note 5
Package Resistance, M2	R ₁₋₂		0.51			T _C = 125 °C, Note 5
Stray Inductance	L _{Stray}		10.2		nH	Between Terminals 2 and 3
Case Temperature	T _C			125	°C	
Weight	W		300		g	
Mounting Torque	M _S	4.5	5	5.5	N-m	Baseplate, M6 Bolts
		4.5	5	5.5		Power Terminals, M6 Bolts
Case Isolation Voltage	V _{isol}			5.5	kV	AC, 50 Hz, 1 min
Comparative Tracking Index	CTI		600			
Clearance Distance		9			mm	Terminal to Terminal
		30				Terminal to Baseplate
Creepage Distance		30				Terminal to Terminal
		40				Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET R_{DS(on)} + Switch Position Package Resistance

Typical Performance

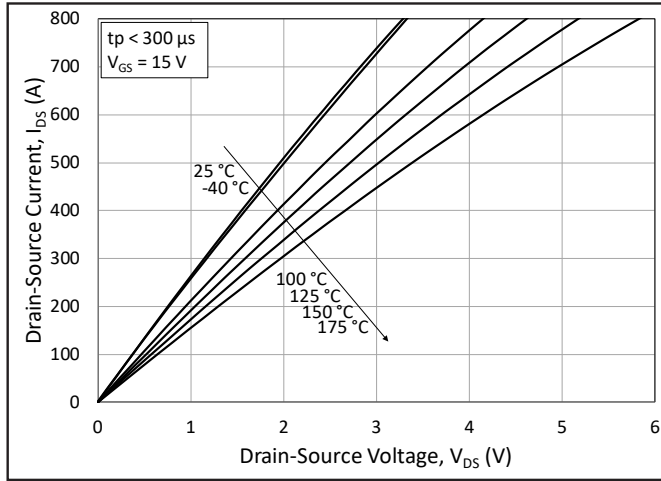


Figure 1. Output Characteristics for Various Junction Temperatures

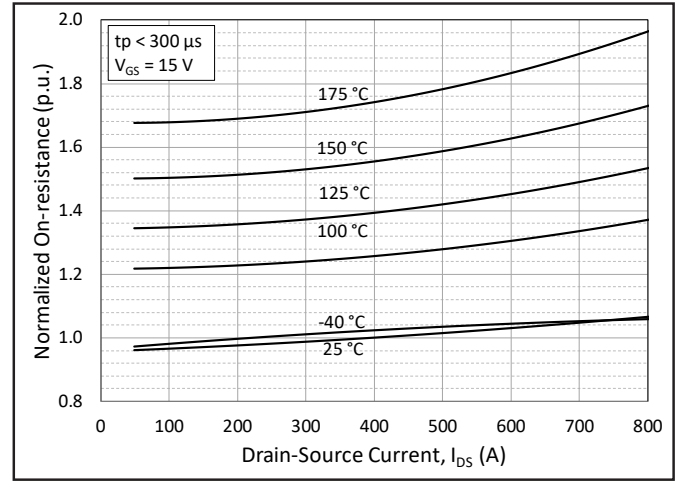


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

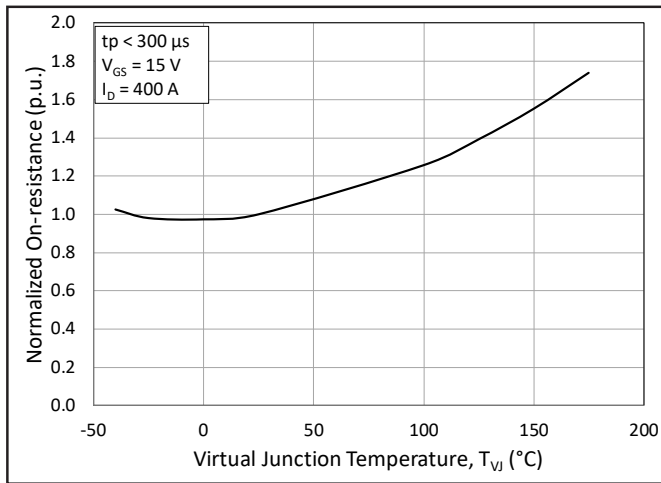


Figure 3. Normalized On-State Resistance vs. Junction Temperature

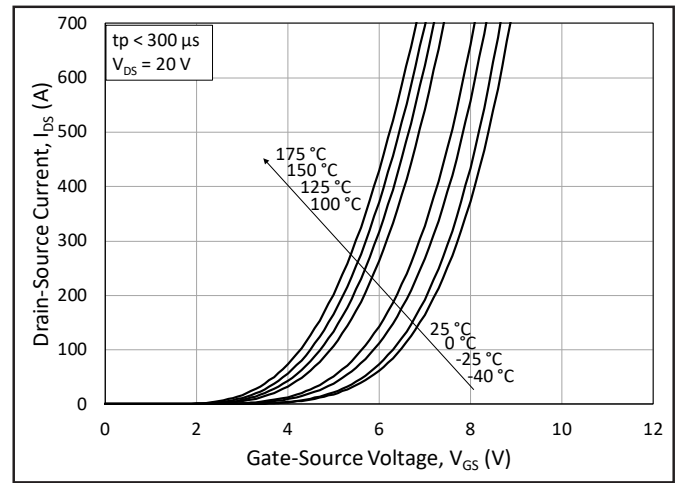


Figure 4. Transfer Characteristic for Various Junction Temperatures

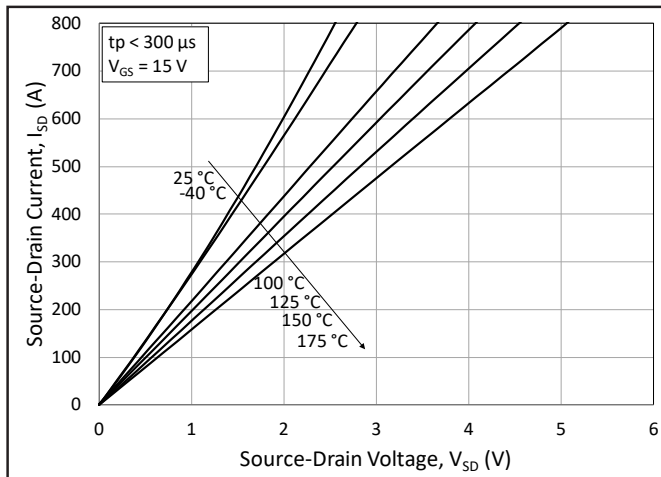


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

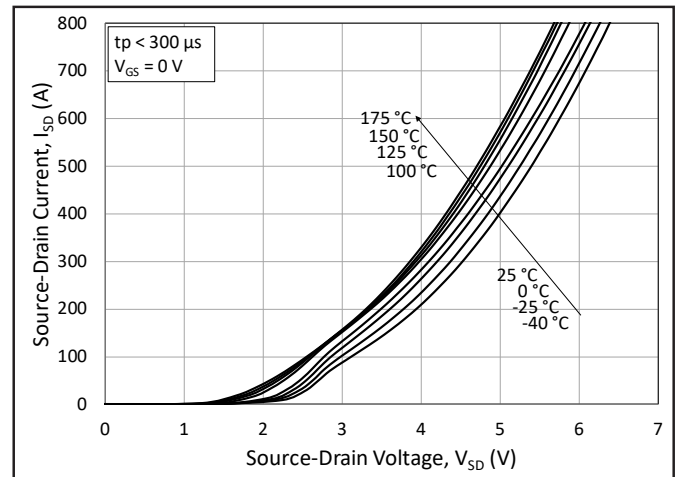


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$ (Body Diode)

Typical Performance

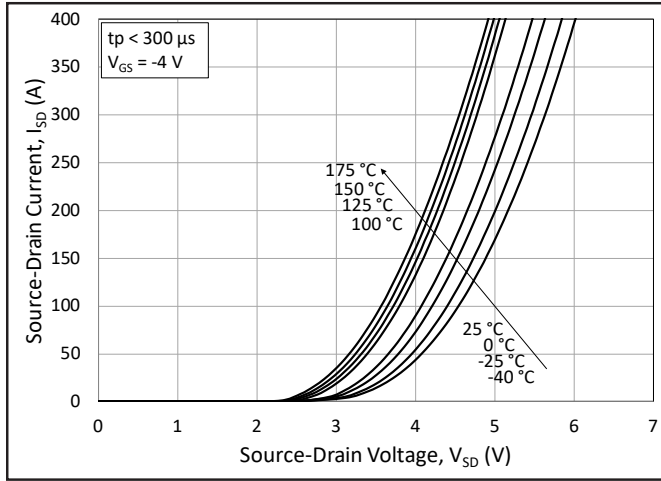


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

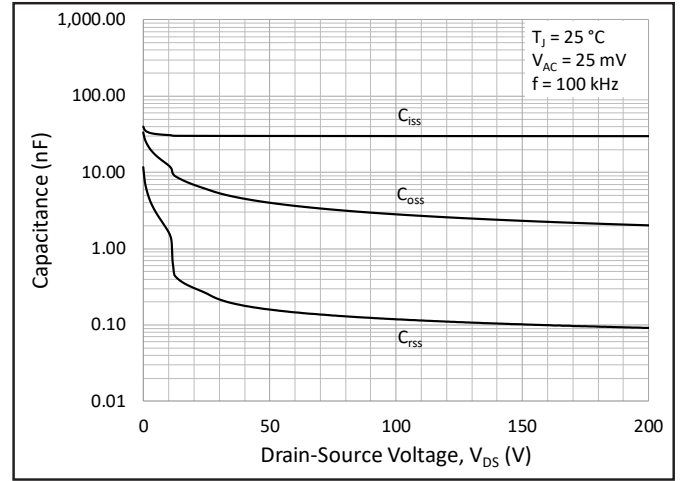


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

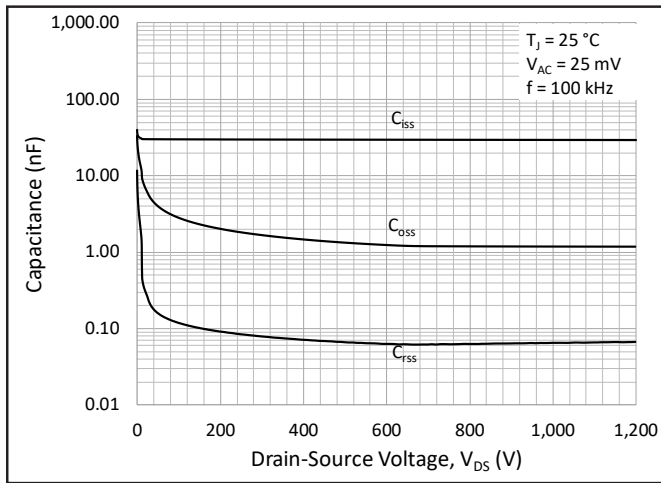


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

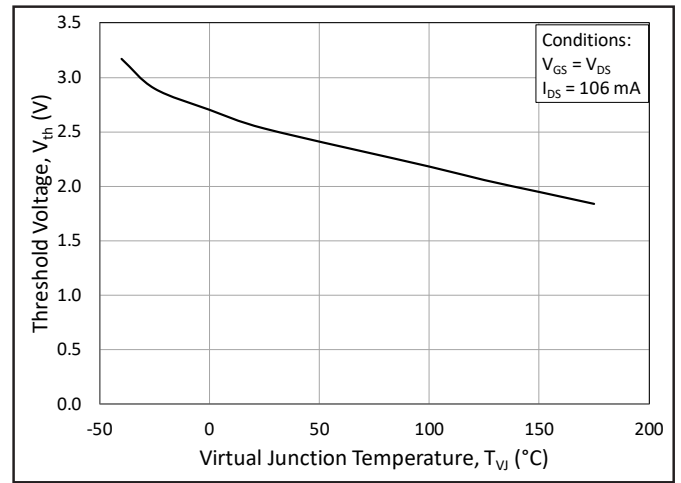


Figure 10. Threshold Voltage vs. Junction Temperature

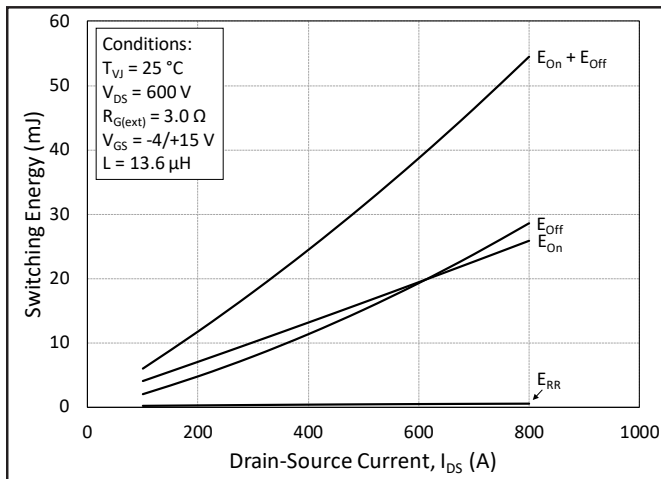


Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600$ V)

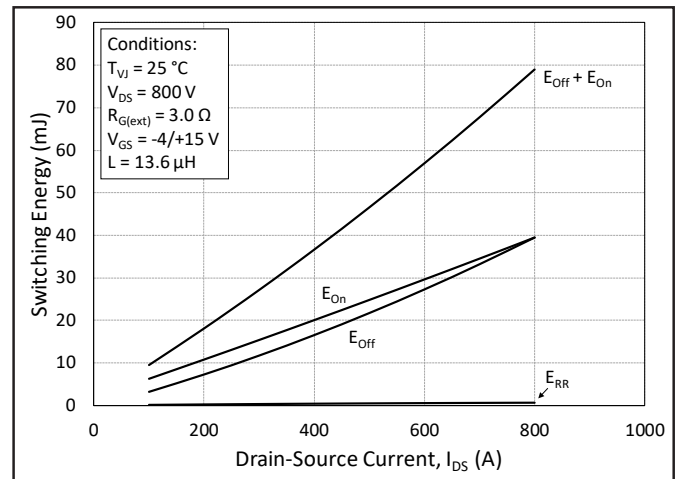


Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800$ V)

Typical Performance

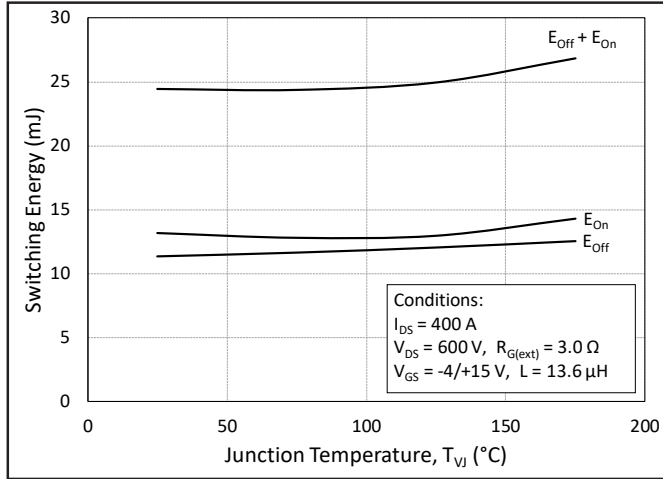


Figure 13. MOSFET Switching Energy vs. Junction Temperature

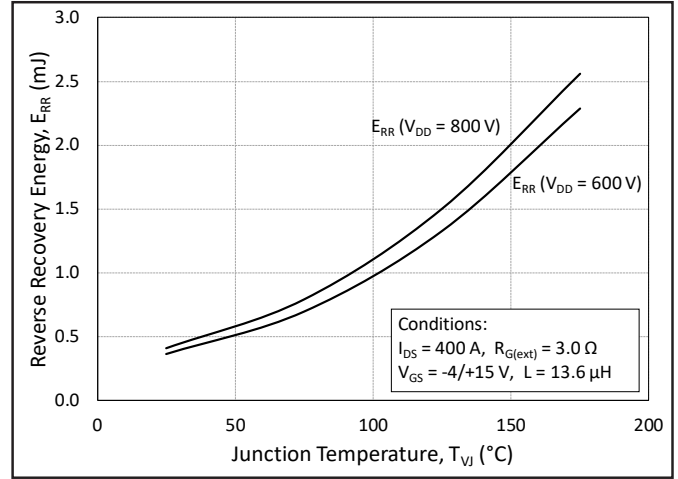


Figure 14. Reverse Recovery Energy vs. Junction Temperature

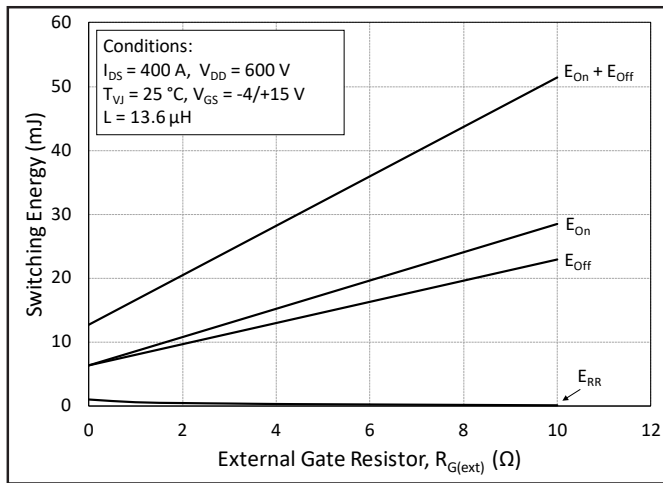


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

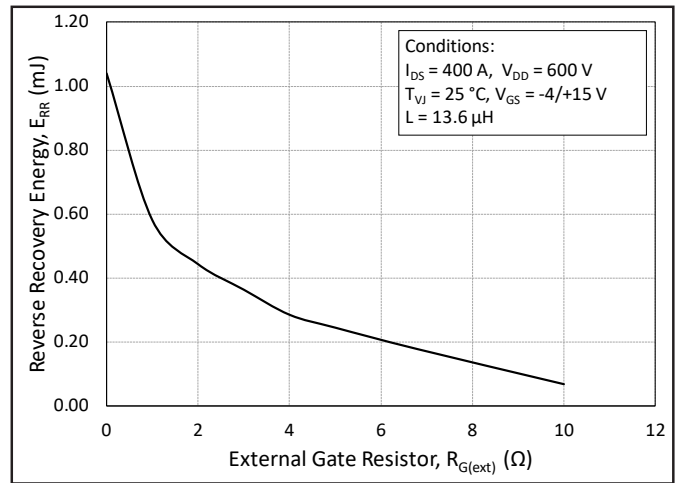


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

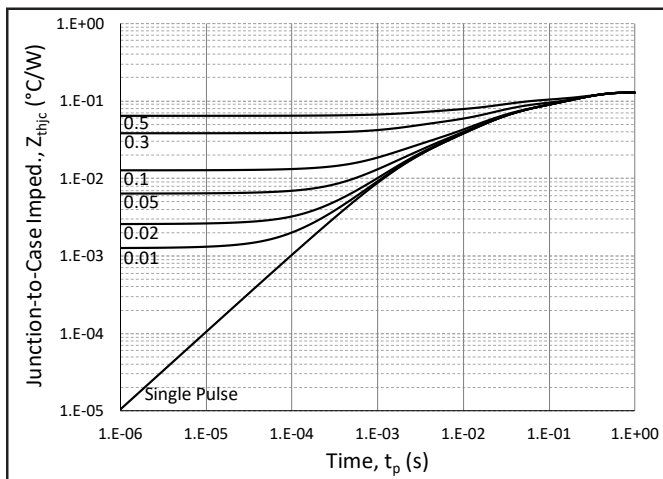


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thJC} (°C/W)

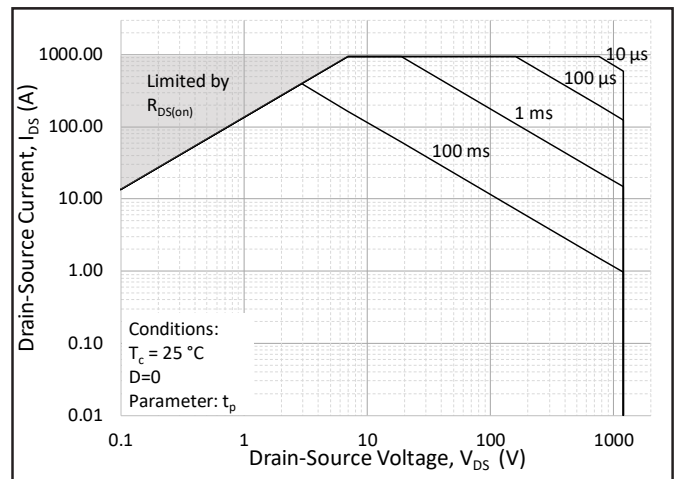


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

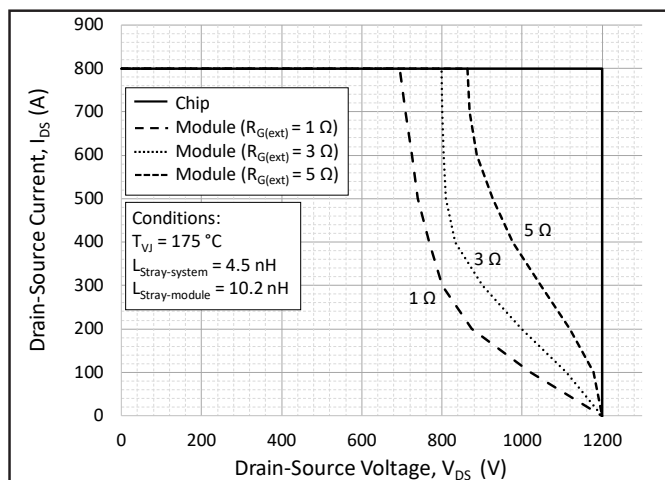


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

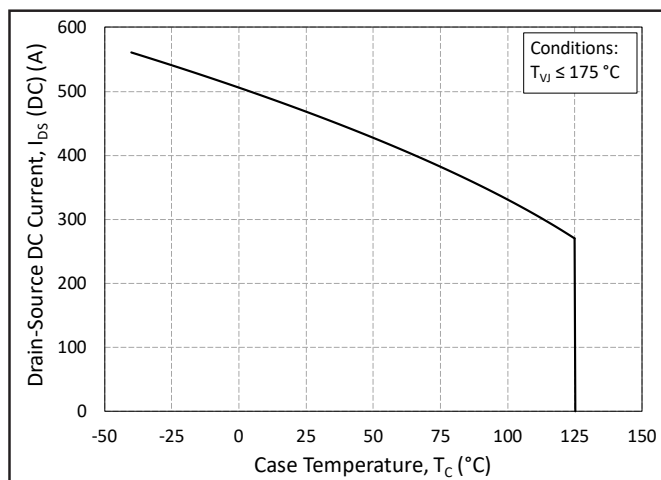


Figure 20. Continuous Drain Current Derating vs. Case Temperature

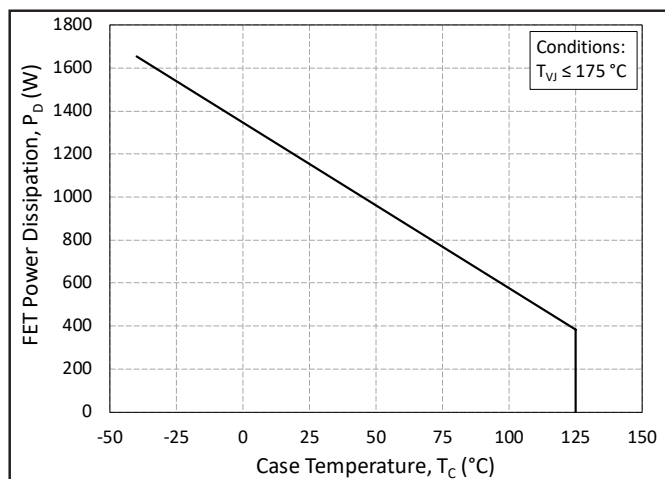


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

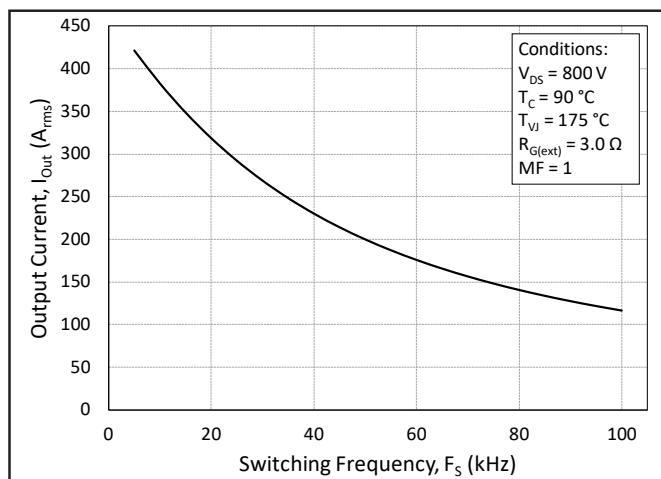


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

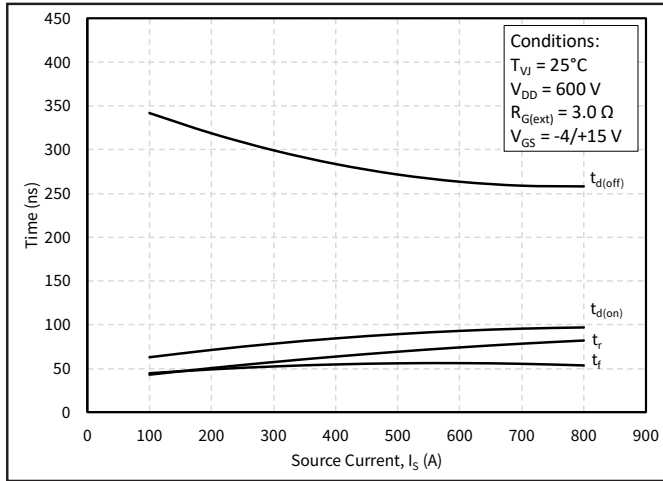


Figure 23. Timing vs. Source Current

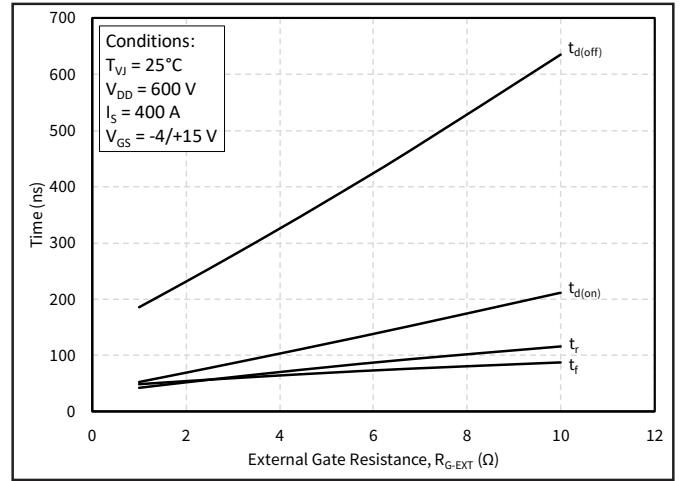


Figure 24. Timing vs. External Gate Resistance

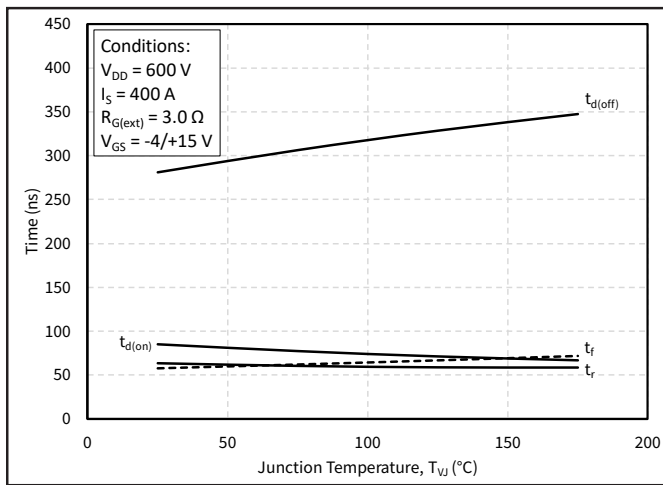


Figure 25. Timing vs. Junction Temperature

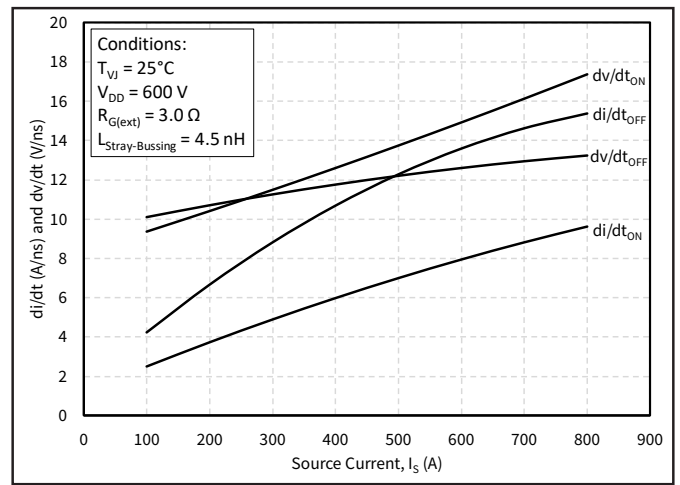


Figure 26. dv/dt and di/dt vs. Source Current

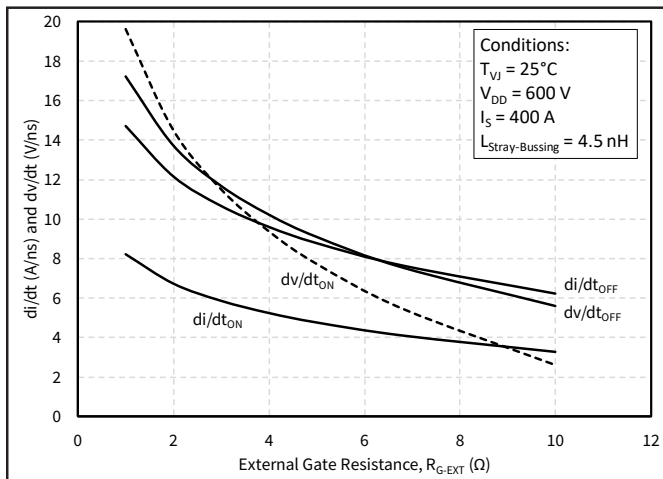


Figure 27. dv/dt and di/dt vs. External Gate Resistance

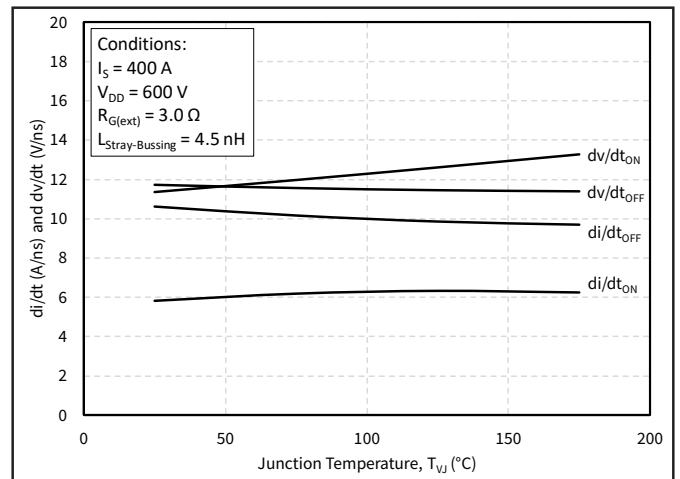


Figure 28. dv/dt and di/dt vs. Junction Temperature

Definitions

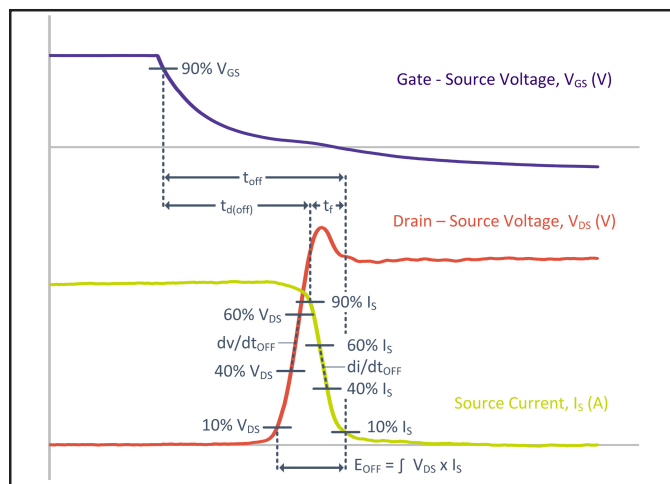


Figure 29. Turn-Off Transient Definitions

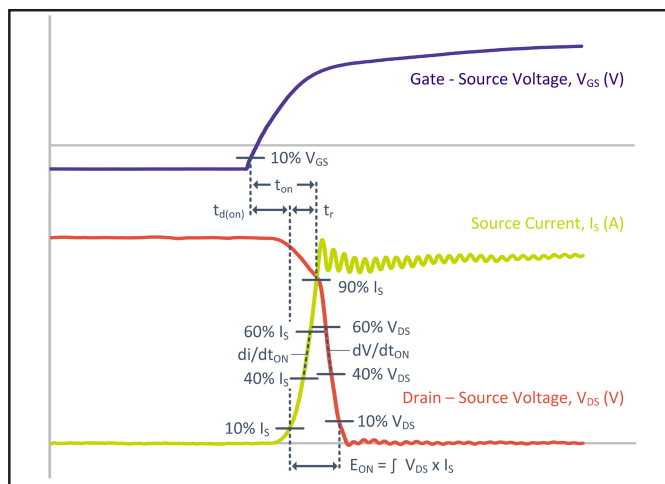


Figure 30. Turn-On Transient Definitions

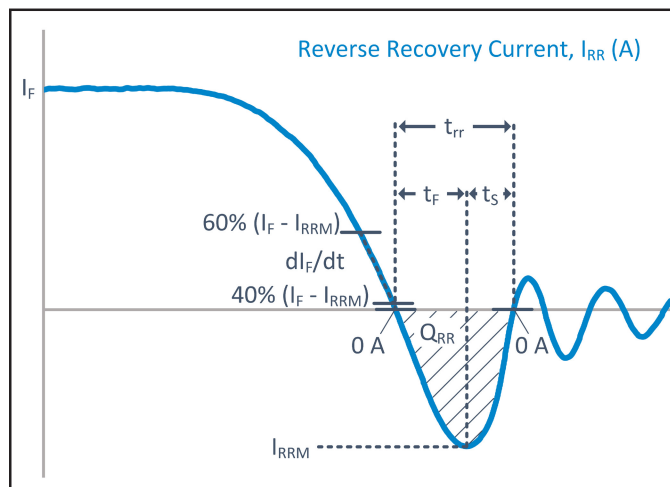


Figure 31. Reverse Recovery Definitions

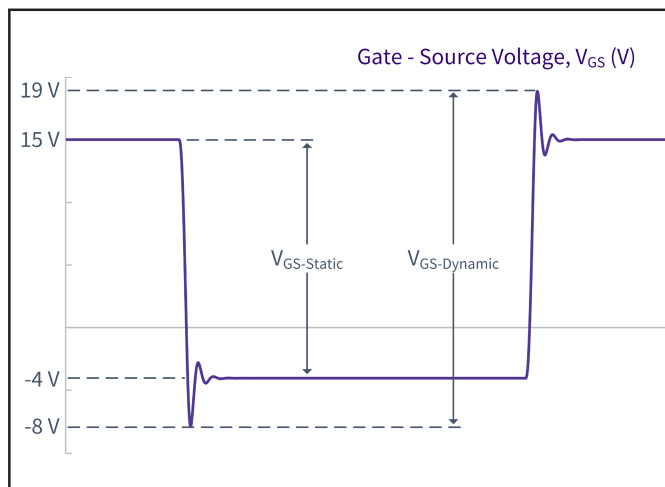
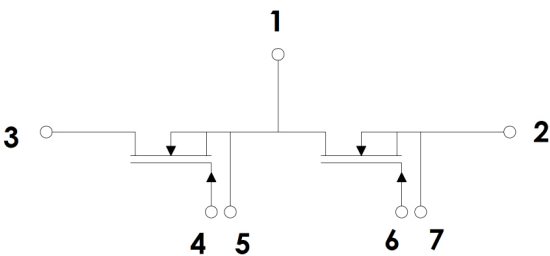
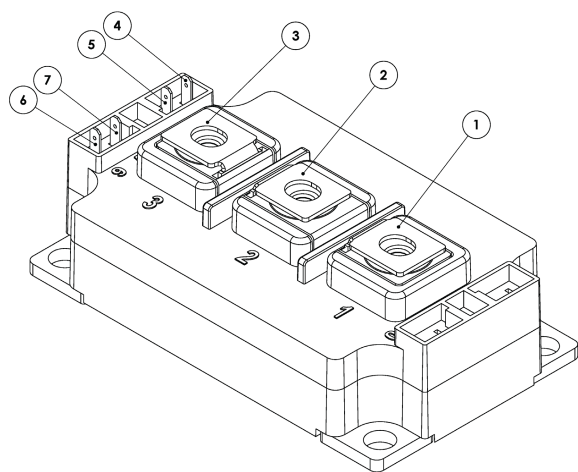


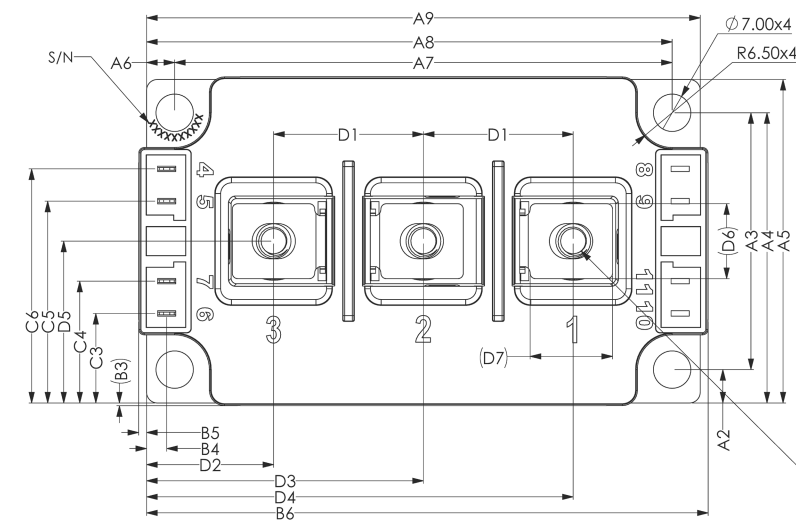
Figure 32. V_{GS} Transient Definitions



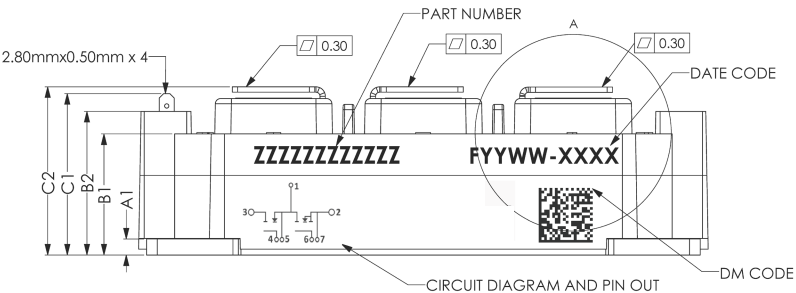
Schematic and Pin Out



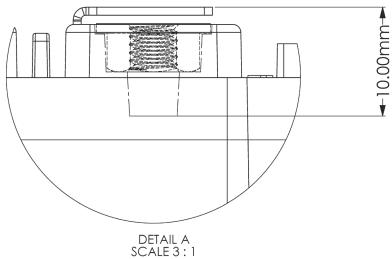
Package Dimensions (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION (mm)	TOLERANCE (mm)
A1	3.00	+0.30
A2	6.22	+0.30
A3	48.00	+0.30
A4	54.22	+0.30
A5	60.44	+0.30
A6	5.25	+0.30
A7	93	+0.30
A8	98.25	+0.30
A9	103.50	+0.30
B1	22.75	+0.30
B2	27.30	+0.30
B3	0.51 x 2	REF
B4	3.76	+0.40
B5	1.25	+0.40
B6	105.00	+0.30
C1	30.60	+0.50
C2	31.40	+0.40
C3	16.72	+0.40
C4	22.75	+0.40
C5	37.7	+0.40
C6	43.73	+0.40
D1	28.00	+0.50
D2	24.20	+0.40
D3	52.00	+0.40
D4	79.80	+0.40
D5	30.22	+0.40
D6	14.00 x 3	REF
D7	15.40 x 3	REF



M6x6mm HEX NUT x 3
MAXIMUM BOLT PENETRATION DEPTH: 10mm





Supporting Links & Tools

- [CGD1200HB2P-BM3 Evaluation Gate Driver](#)
- [CGD12HB00D: Differential Transceiver Board](#)
- [KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 & BM3 Module \(CPWR-AN-36\)](#)
- [CPWR-AN-34: Module Mounting Application Note](#)
- [CPWR-AN-35: Thermal Interface Material Application Note](#)



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