Winbond Electronics Corp.

W83L197R-16
Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

1.0 GENERAL DESCRIPTION

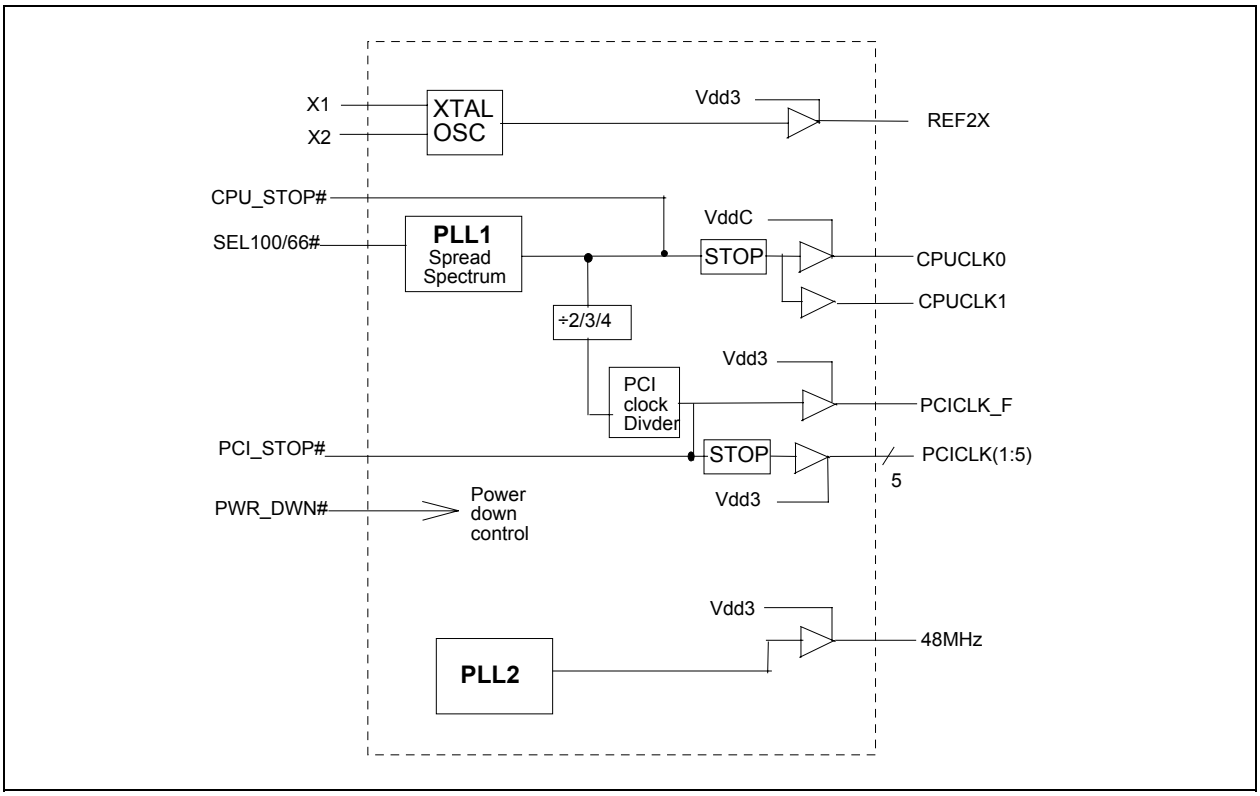
The W83L197R-16 is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor. Four different frequency of CPU, and PCI clocks are externally selectable with smooth transitions. The 0.5% or 0.75% center type spread spectrum can be selected to reduce EMI.

The W83L197R-16 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 48 MHz provide better than 0.5V /ns slew rate.

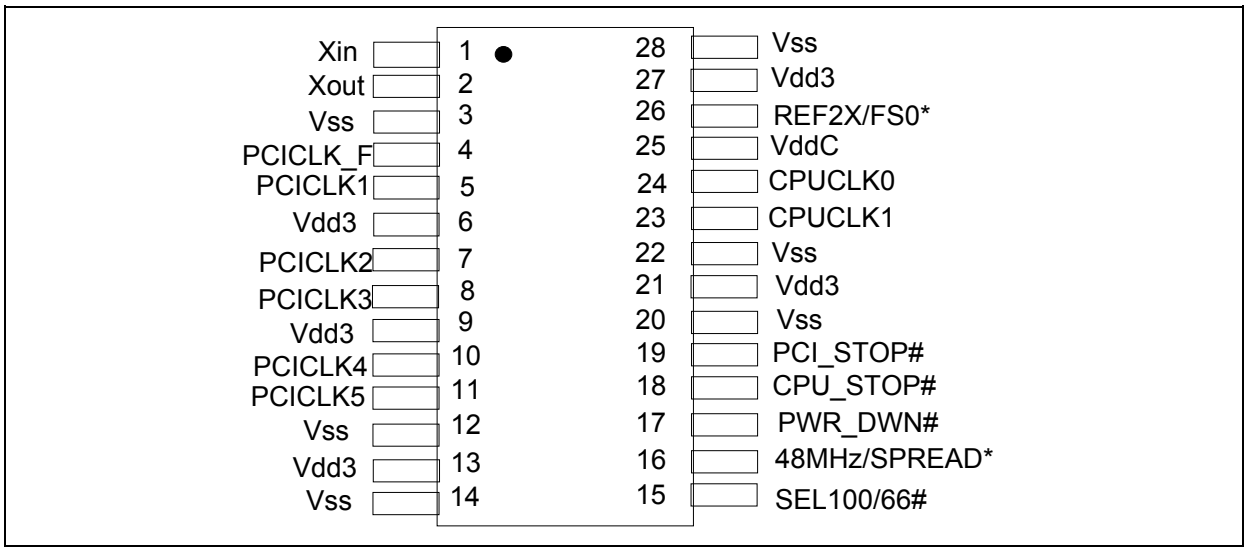
2.0 PRODUCT FEATURES

- Supports Pentium™ II CPUs
- 4 sets of CPU frequencies selection
- 2 CPU clocks (one free running CPU clock)
- 6 PCI synchronous clocks(one free running PCI clock)
- Optional single or mixed supply:
  (Vdd3 = VddC= 3.3V±5%) or (VddC = 2.5V±5%)
- Skew form CPU to PCI clock 1.5 to 4.0 ns, CPU leads.
- CPU clock jitter less than 200ps
- PCI_F,PCI1:6 clock skew less than 500ps
- ±0.5% or ±0.75% center type spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz for USB
- 28-pin SOP package (209mil)

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION



5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Low active

* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	1	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	2	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK0 CPUCLK1	24,23	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. VddC is the supply voltage for these outputs.
PCICLK [1:5] PCICLK_F	5,7,8,10,11 4	OUT	Low skew (< 250ps) PCI clock outputs.
PCI_STOP#	19	I/O	PCI_STOP# input used in power management mode for synchronously stopping the all CPU clocks.
CPU_STOP#	18	I/O	this pin is CPU_STOP # and used in power management mode for synchronously stopping the all PCI clocks.

5.3 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
SEL100/66#	15	IN	CPU clock frequency select pin.
REF2X / FS0*	26	I/O	Internal 250kΩ pull-up. Latched input for FS0* to chose frequencies at initial power up. Reference clock during normal operation.
48MHz/SPREAD*	16	I/O	Internal 250kΩ pull-up. 48MHz output for USB during normal operation. Latched input for SPREAD* to select the spread spectrum spend at initial power up.

5.4 Power Pins

SYMBOL	PIN	FUNCTION
VddC	25	Power supply for core logic and PLL circuitry. Connect to 3.3V supply.
Vdd3	6,9,13,21,27	Power supply for others Connect to 3.3V supply.
Vss	3, 12,14,20,22,28	Circuit Ground.

6.0 FREQUENCY SELECTION

FS0*	SEL100/66#	CPUCLK0, CPUCLK1	PCI
1	1	100MHz	33.3MHz
1	0	66.8MHz	33.4MHz
0	1	112MHz	37.3MHz
0	0	103MHz	34.33MHz

7.0 FUNTION DESCRIPTION

7.1 SPREAD SPECTRUM FUNCTION SELECTION TABLE

SPREAD*	Spread Spectrum	Type
1	±0.5%	Center
0	±0.75%	Center

7.2 POWER MANAGEMENT FUNCTIONS

The W83L197R-16 may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPUCLK1	PCICLK1:5	PCICLK_F	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING

8.0 SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

8.2 AC CHARACTERISTICS

Vdd3 = VddCore = 3.3V±5%, VddC = 2.5V±5% , T_A = 0℃ to +70℃						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU to PCI Offset	t_{OFF}	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
Cycle to Cycle Jitter	t_{CCJ}			200	ps	
CPU Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V_{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

8.3 DC CHARACTERISTICS

Vdd3 = VddCore = 3.3V±5%, VddC = 2.5V±5% , T_A = 0℃ to +70℃						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-25	μA	
Input High Current	I_{IH}			10	μA	
Output Low Voltage I_{OL} = 1 mA	V_{OL}			50	mV_{dc}	CPU_F, CPU1
Output High Voltage I_{OH} = -1mA	V_{OH}	3.1			V_{dc}	CPU_F, CPU1
Output Low Current	**I_{OL}**	27	57	97	mA	CPU_F,CPI1
		20.5	53	139	mA	PCI_F,PCI1:6
		40	85	140	mA	IOAPIC
		50	74	152	mA	REF2X
		25	37	76	mA	48,24MHz
Output High Current	I_{OH}	25	55	97	mA	CPU_F,CPI1
		31	55	189	mA	PCI_F,PCI1:6
		40	87	155	mA	IOAPIC
		54	88	188	mA	REF2X
		27	44	94	mA	48,24MHz

8.4 BUFFER CHARACTERISTICS

8.4.1 TYPE 1 BUFFER FOR CPUCLK

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-27			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-27	mA	Vout = 2.0V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.2 V
Pull-Down Current Max	$I_{OL(max)}$			27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20 pF Load

8.4.2 TYPE 3 BUFFER FOR REF2X, 48MHZ

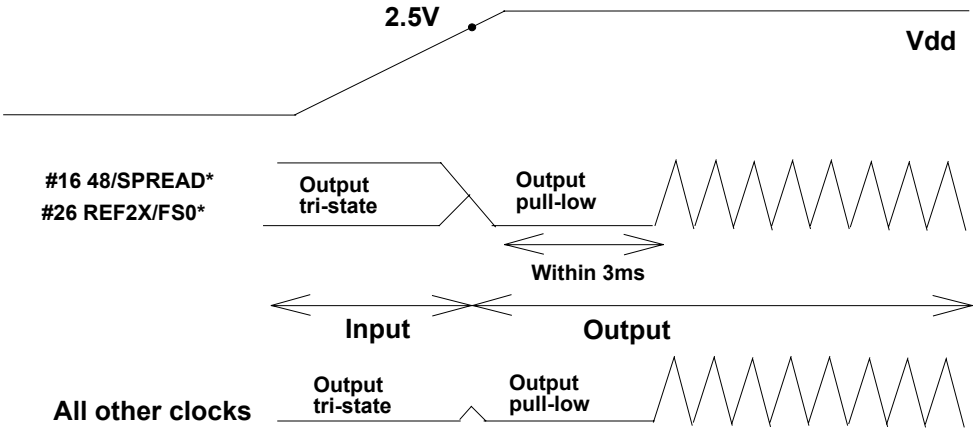
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-29			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-23	mA	Vout = 3.135V
Pull-Down Current Min	$I_{OL(min)}$	29			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$				mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	1.0			ns	10 pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			4.0	ns	20 pF Load

8.4.3 TYPE 5 BUFFER FOR PCICLK(1:5,F)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-33			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-33	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$	30			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$			38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	15 pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			2.0	ns	30 pF Load

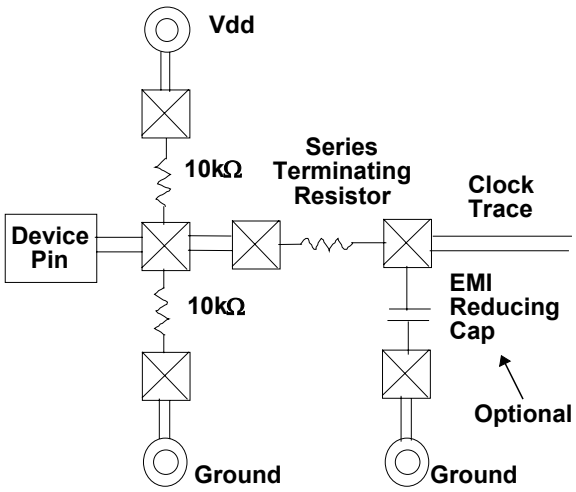
9.0 OPERATION OF DUAL FUCTION PINS

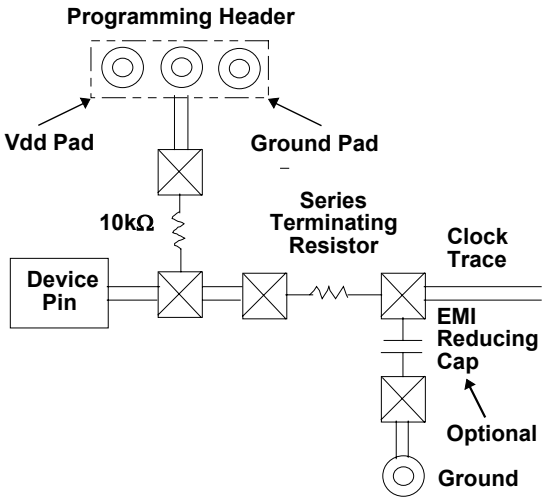
Pin16 and pin26 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Fig1), therefore, and are considered input select pins. When Vdd reaches 2.5V, the logic level that is present on these pins are latched into their appropriate internal registers. Once the correct information are properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins are a large pull-up resistor (250 kΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 kΩ resistor is recommended to be connected to Vdd if logic 1 is expected. The same 10 kΩ connection to ground if a logic 0 is desired. The 10 kΩ resistor should be place before the serious terminating resistor. Note that these logic will only be latched at initial power on.

If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitor has typical values ranging from 4.7pF to 22pF.

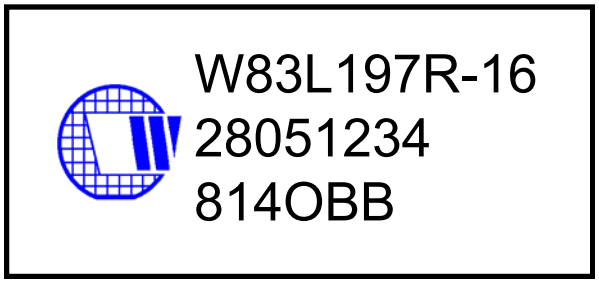

Vdd
10kΩ
Series
Terminating
Resistor
Clock
Trace
Device
Pin
10kΩ
EMI
Reducing
Cap
Optional
Ground
Ground


Programming Header
Vdd Pad
Ground Pad
10kΩ
Series
Terminating
Resistor
Clock
Trace
Device
Pin
EMI
Reducing
Cap
Optional
Ground

10.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83L197R-16	28 PIN SOP (209mil)	Commercial, 0°C to +70°C

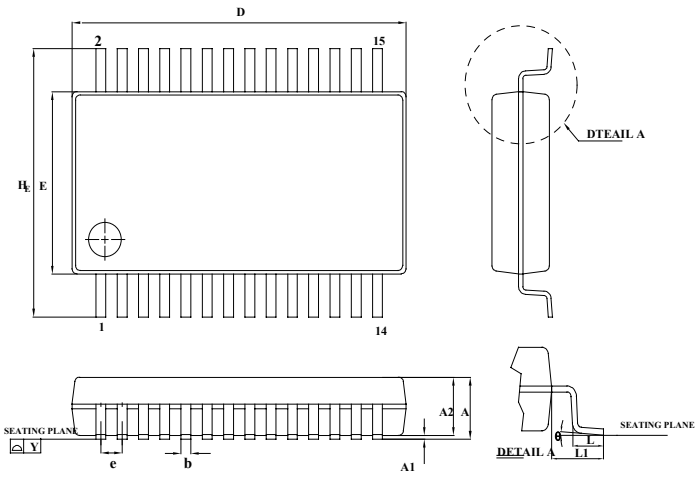
11.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83L197R-16
2nd line: Tracking code 2 8051234
2: wafers manufactured in Winbond FAB 2
8051234: wafer production series lot number
3rd line: Tracking code 814 G B B
814: packages made in '98, week 14
G: assembly house ID; A means ASE, S means SPIL, G means GR
BB: IC revision

12.0 PACKAGE DRAWING AND DIMENSIONS

28-SOP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	9.90	10.20	10.50	0.389	0.401	0.413
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

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