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W83791SD/
W83791SG

WINBOND
H/W MONITORING IC

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Revision History

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	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All version before 0.50 are for internal use.
2	n.a.	01/Jan	0.5	n.a.	First publication.
3	n.a.	02/Apr	1.0	1.0	Change all version include version on web site to 1.0
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5					
6					
7					

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1. GENERAL DESCRIPTION

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W83791SD/SG is a programmable speech synthesizer with 9-bit current DAC output that can connect to speaker or LINE_OUT by the AC'97 audio codec. It supports 1 CPU present or absent event trap, 5 external event traps, and 127 internal programmable event traps to trigger maximum 133 different speech output. If more than two events happen simultaneously, the priority set is: SLOTOCC# > EVNTRP1 > EVNTRP2 > EVNTRP3 > EVNTRP4 > EVNTRP5 > 127 Programmable events (Bank0 index 09h).

For the application of error messages from BIOS, 127 Programmable events are enabled with a watch dog timer. The time interval is programmable and events will be triggered when time out.

External flash memory interface with Winbond W55FXX is flexible to change warning voice message and support on-line programming flash data through I^2C^{TM} interface. An external resistor is added to provide ring oscillator.

Through the application software or BIOS, the users can edit and change the voice database in the serial flash chip by themselves under O.S. A free Windows AP --- Voice Editor^{TM} is provided for the voice editing, which can accept the *.wav file as the voice database resource. Users can replace the voice with which they like through the S/W.

W83791SD/SG also provides two addresses setting pins A0 & A1 for different I^2C^{TM} address and can be connected up to 4 devices if necessary.

2. FEATURES

Speech Item

- Programmable speech synthesizer
- New high fidelity synthesis algorithm
- Build in 8-bit current D/A converter
- Instruction cycle ˙ 400 μS typically
- Section control provided in each voice section
  ˙˜ Variable frequency: 4.8/6/8/12 KHz
- External resistor for ring oscillator
- 1 CPU present or absent trigger input
- 5 External trigger inputs
- 127 Internal programmable trigger inputs with a watch dog timer
- Programmable 0-255 seconds timeout trigger inputs

General

- I^2C^{TM} serial bus interface
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C^{TM} interface
- Winbond hardware monitoring application software (Voice Editor^{TM}) support, for both Windows 95/98/ME/2000 and Windows NT 4.0/5.0
- Internal clock Oscillator with 3M Hz
- 5V V_{DD} operation

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Package

- 48-pin LQFP

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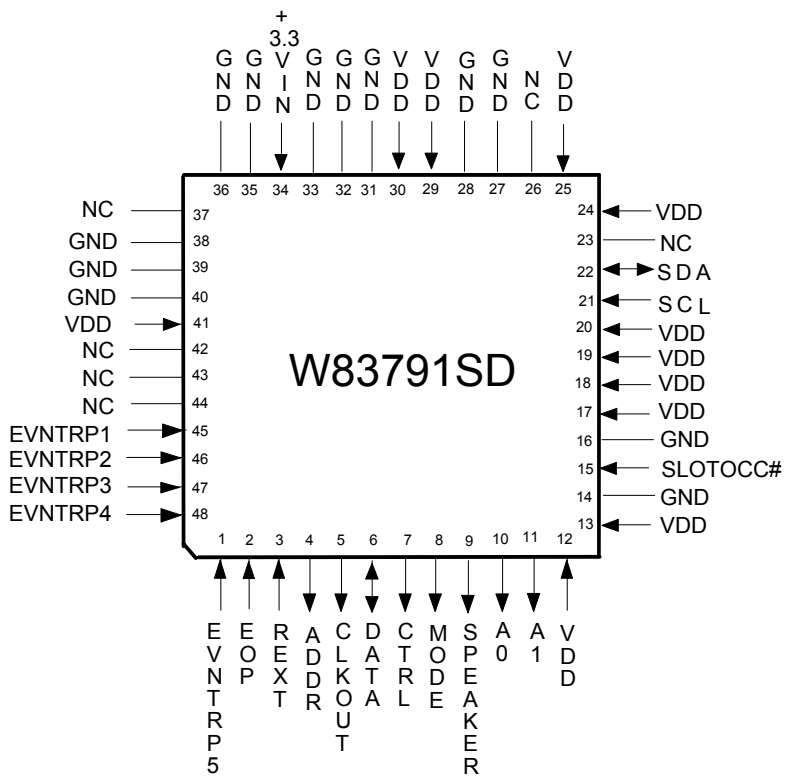
3. KEY SPECIFICATIONS

- Supply Voltage 5V
- Operating Supply Current 5 mA typ.

4. PIN CONFIGURATION



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5. PIN DESCRIPTION

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I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger with 12 mA source-sink capability
I/OD_{8ts} - TTL level and schmitt trigger open drain output with 8 mA sink capability
OUT_{12} - Output pin with 12 mA source-sink capability
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin (Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
EVNTRP5	1	IN_t	Event trapping to selection speech output sound.
EOP	2	IN_t	End of Process signal input from cascaded Flash.
REXT	3	IN_t	Resistor (Rosc) connects to VSB to adjust ring oscillator frequency.
ADDR	4	OUT_{12}	Speech address pulse output, connect to W55FXX. When this pin translates from logic high to logic low, it will latch the data pin 6 and shift it into a speech flash address counter.
CLKOUT	5	OUT_{12}	Speech clock output, for speech data read-out and write-in, connect to W55FXX. When this pin translates from logic high to logic low, the data pin 6 will be latched by this clock.
DATA	6	I/O_{12t}	Serial data input/output, connect to W55FXX. The pin is latched by CLKOUT and ADDR acted as speech data and address respectively.
CTRL	7	OUT_{12}	Output clock numbers of this pin decide which mode is selected. Connect to W55FXX.
MODE	8	OUT_{12}	Output mode signal to W55FXX serial Flash.
SPEAKER	9	OUT_{12}	Current type output driving an external speaker. The function is only working in VSB 5V OK.
A0	10	IN_{ts}	I^2C device address bit0 trapping during 5VDD power on.
A1	11	IN_{ts}	I^2C device address bit1 trapping during 5VDD power on.
VDD (5V)	12, 13, 17, 18, 19, 20, 24, 25, 29, 30, 41	POWER	+5V VDD pins.
GND	14, 16, 27, 28, 31, 32, 33, 35, 36, 38, 39, 40	GROUND	Ground pins
SLOTOCC#	15	IN_{ts}	CPU presence signal. 0 means CPU is present. 1 means CPU is absent.
NC	23, 26, 37, 42, 43, 44		No connect.
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	I/OD_{8ts}	Serial Bus bi-directional Data.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
EVNTRP1-4	45-48	I/O_{12ts}	Event trapping to selection speech output sound.

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6. FUNCTION DESCRIPTION

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6.1 Speech Function

6.1.1 General Description

The W83791SD/SG is a derivative of Winbond's *PowerSpeech*™ synthesizers. There are up to 5 hardware trigger inputs and 128 programmable software event trigger inputs. If more than two events happen simultaneously, the priority set by the internal H/W is: SLOTOCC# > EVNTRAP1 > EVNTRAP2 > EVNTRAP3 > EVNTRAP4 > EVNTRAP5 > TRIGREG (Index 09h) 128 events. Software trigger is able to accommodate 128 event triggers, with timeout register (index 08h) enabled in advance for allowance of time on detecting devices. That is, once the system's power is on, BIOS can fill trigger event and speech voice will not be sent until the system fails owing to timeout. In addition, to prevent events from taking place simultaneously.

6.1.2 Event Trigger Queue

W83791SD/SG provides 8 byte FIFO queue to store event trigger, i.e., the first 8 event can be served by speech and speech will clear FIFO queue after service. Coding of Speech program must assign correct CPU_MODE event vector to issue correct speech voices correspondent to speech trigger events. For example, CPU_MODE event vector =1 represents absence of CPU, then coding speech with CPU is absent voice. When W83791SD/SG detects no CPU exists, it will send vector = 1 to speech synthesizer and play this voice data. Following is the block diagram of the 8-Byte event trigger queue.

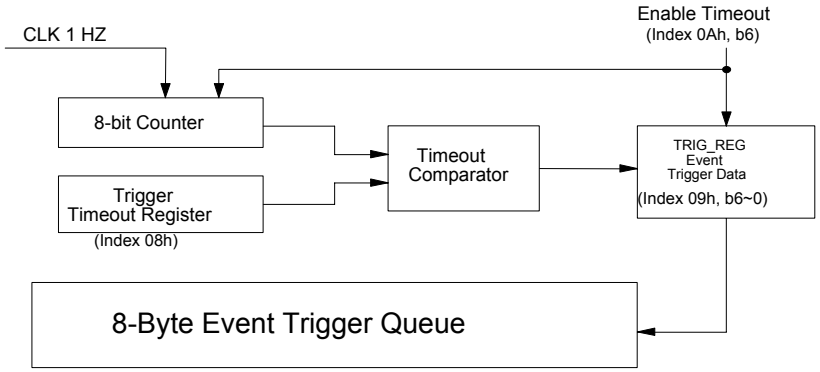

Figure 1. Event trigger Queue

For example: As BIOS usually has POST (Power On Self Test) program, then it will test every item step by step if no failure takes place, however, if it detects a failure on a specific item, it will hang on there. Therefore, BIOS could write timeout value to register 08h and start timer setup speech trigger event (register 09h), then BIOS test program starts. Whenever the system is hang on specific item such as DRAM testing, W83791SD/SG would say "DRAM test fails" after the timeout previously set at CR [08h]. On the contrary, if DRAM test is ok, then BIOS could update the timeout value and proceed to the next test program.

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Below is the speech CPU_MODE table of W83791SD/SG.

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CPU_MODE ITEM	DEFINITION	VECTOR (H)
POI	Reserverd	0,32
SLOTOCC	CPU present or absent	1
EVNTRAP1(TG1)	Hardware trgger1	2
EVNTRAP2	Hardware trgger2	3
EVNTRAP3	Hardware trgger3	4
EVNTRAP4	Hardware trgger4	5
EVNTRAP5	Hardware trgger5	6
TRIGREG	I2C setting software trigger	80-FF

Table 1 CPU_MODE

6.1.3 Connection of EEPROM

As described previously the W83791SD/SG could connect W55FXX to store voice data. To expand the storage capacity, users could select more than one W55FXX to connect together. The maximum capacity could be up to 16Mbit. Following is the connection chart of W55FX with W83791SD/SG.

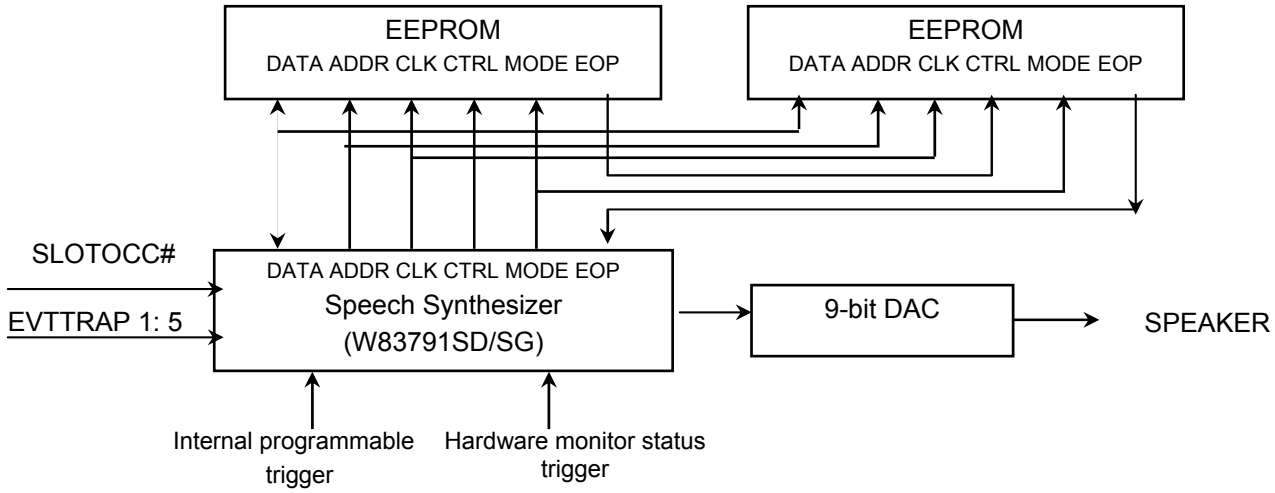

Figure 2 Speech Function Diagram

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6.1.4 Speaker Output

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Speech output pin is an 8 bit Current D/A converter, with which loading is needed. The resistor could range from 510~1K ohm and bipolar junction transistor could be a low power NPN type bipolar with β of 120 - 160. Usually, an 8050D transistor is appropriate. The spec of the speaker is 8Ω. Besides, SPK can also connect to AC97 codec chip Line_Out. C is decouple capacitor and is usually 200p- 0.01uF.

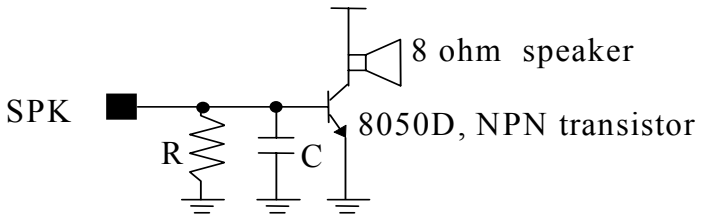

Figure. 3

7. CONTROL AND STATUS REGISTER

7.1 Speech Flash Memory Address Registers — Index 00h-02h (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
00h	SPEECHA0	R/W	**Speech Flash Address 0.** Set speech flash programming address bits [7:0].
01h	SPEECHA1	R/W	**Speech Flash Address 1.** Set speech flash programming address bits [15:8].
02h	SPEECHA2	R/W	**Speech Flash Address 2.** Set speech flash programming address bits [23:16].

7.2 Speech Flash Memory Data Registers — Index 03h-06h (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
03h	SPEECHD0	R/W	**Speech Flash Data 0.** Set speech flash programming data bits [7:0].
04h	SPEECHD1	R/W	**Speech Flash Data 1.** Set speech flash programming data bits [15:8].
05h	SPEECHD2	R/W	**Speech Flash Data 2.** Set speech flash programming data bits [23:16].
06h	SPEECHD3	R/W	**Speech Flash Data 3.** Set speech flash programming data bits [31:24].

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Power on default: 00h

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BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PROG_ACTIVE	R/W	**Program Active Command. If set this bit to 1, the serial flash will be active according the Flash Program Mode. Reading this bit, the bit will return a Serial Flash Busy (SER_BUSY). And this is pulse, if read this bit show "**0"
6:4	Reserved		**Reserved.**
3:0	PROGMODE	R/W	**Flash Program Mode** FLASHCTRL[3:0] | 0000b | No action 0001b | Program mode 0010b | Erase all 0011b | Page code 0100b | Erase 4K bytes 0101b | Erase 16K bytes 0110b | Page code read out 0111b | Read flash data

Program procedure:

1. Set Flash address (3-bytes)
2. Set Flash Data (4-bytes)
3. Set Flash control "Program mode"
4. Set program command active (PROG_ACTIVE)

Erase 4K:

1. Set Flash Address (must be 4K address boundary)
2. Set Flash control register

7.3 Event Trigger Timeout Register — Index 08h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:0	TRIG_TIME	R/W	Event Trigger Timeout Timer Setting. When software or firmware write trigger event, that don't write to speech queue until this register is timeout. This unit is Second. Default is 00, that is, the software event doesn't need to wait then write to sound event queue. Note that, this function is controlled by Speech Input Property (Index 0Ah).

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7.4 Speech Programmable Trigger Register — Index 09h (Bank 0)

Power on default: 80h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TR_RDY	RO	Programmable Trigger Register Ready. If return to 1, the software or firmware can write next event to trigger register. If return to 0, the software or firmware cannot write trigger event to event queue, that is, the timer is not timeout yet.
6:0	TRIG_REG	R/W	Speech Programmable Trigger Register. The software or firmware can set these bits to trigger speech sound. The vectors of sound trigger are shown as follows. If the bit of trigger register ready is logic 0, this trigger register will be ignored. Therefore, the bit of the trigger ready should be read before programming this register.

TRIG_REG<6:0>	Speech Sound Vector
00h	Vector 80h (1000_0000b) (=80h+00h)
01h	Vector 81h (1000_0001b) (=80h+01h)
02h	Vector 82h (1000_0010b) (=80h+02h)
:	:
N	Vector (80h+*n*)
:	:
7Eh	Vector FEh (1111_1110b) (=80h+7Eh)
7Fh	Vector FFh (1111_1111b) (=80h+7Fh)

7.5 Speech Input Trigger Property Register — Index 0Ah (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	En_Program	R/W	Enable W83791SD/SG to program external serial flash memory.
6	En_Timeout	WO	Enable Software/Firmware Trigger Timeout Function. This bit sets the Event Trigger Timeout Function in Index 08h.
5	Busy	RO	If read this bit return “1” means SPKOUT is in busy.
4:0	EVNTRAP5-1 Polarity	R/W	Write ‘0’ the EVNTRAP5-1 will positive edge trigger, Write ‘1’ will negative edge trigger. Default is ‘0’.

7.6 Speech Flash Memory Read Data Registers — Index 0Dh-0Eh (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
0Dh	SPEECHRD0	RO	Speech Flash Read Data 0. Speech flash reading data bits [7:0].
0Eh	SPEECHRD1	RO	Speech Flash Read Data 1. Speech flash reading data bits [15:8].

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7.7 User Defined Registers — Index 18h-1Ch (Bank 0)

User defined registers. Write a data to the mapped register will return a prior written data when read this mapped register.

7.8 Speech Control Register 1 — Index 1Fh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Dis_SLOC_SPK	R/W	Disable SPEECH output from SLOTOCC# if the CPU is absent. Write 1, disable SPEECH output. Default 0.
6	Dis_ET5_SPK	R/W	Disable SPEECH output from EVNTRP5 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
5	Dis_ET4_SPK	R/W	Disable SPEECH output from EVNTRP4 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
4	Dis_ET3_SPK	R/W	Disable SPEECH output from EVNTRP3 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
3	Dis_ET2_SPK	R/W	Disable SPEECH output from EVNTRP2 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
2	Dis_ET1_SPK	R/W	Disable SPEECH output from EVNTRP1if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
1:0	Reserved		

7.9 Serial Bus Address Register — Index 48h (Bank 0)

Power on default: 0010_11xx.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6-0	SMBADDR1	R/W	Serial Bus Address <7:1> for general index registers. The address bit 0 and bit 1 are trapped by the pin 10 and pin 11, respectively.

7.10 Device ID — Index 49h (Bank 0)

Power on default: 0001_000x

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-1	DID<6:0>	Read only	Device ID<6:0>, W83791D version ID that differentiates chip serial product number. This default value is 0010000b, that means is 1.0.
0	Reserved		

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7.11 Disable Abnormal BEEP Control Register — Index 4Dh (Bank 0)

Power on default [7:0]: 0001_0101; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	DIS_ABN	R/W	Disable power-on abnormal the monitor voltage including Vcore, and +3.3V. If these voltages exceed the limit value, the pin of BEEP (Open Drain) will drive 300Hz and 600Hz frequency signal. Write 1, the frequency will be disabled. Default 0. After power on, the system should set 1 to this bit to 1 in order to disable BEEP.
6:0	Reserved		Reserved.

7.12 High Byte Access — Index 4Eh (Bank 0)

Power on default [7:0] 1000_0000b; Reset by MR.

	NAME	ATTRIBUTE	DESCRIPTION
7	HBACS	R/W	High byte access. Set to 1, access Register 4Fh high byte register. Set to 0, access Register 4Fh low byte register. Default 1.
6:0	Reserved		Reserved

7.13 Winbond Vendor ID — Index 4Fh (Bank 0)

Power on default: A3h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:0	Vendor ID	Read Only	Vendor ID low byte if CR4E.bit7=0. Default A3h. Vendor ID high byte if CR4E.bit7=1. Default 5Ch.

7.14 Winbond Test Register — Index 50h - 55h (Bank 0)

These Registers is reserved for Winbond test only. Users do not use these registers.

7.15 Chip ID -- Index 58h (Bank 0)

Power on default: 71h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	CHIPID	Read Only	Winbond Chip ID. Read this register will return 71h.

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7.16 Speech Flash Memory Read Data Registers — Index A4h-A5h (Bank 0)

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Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
A4h	SPEECHRD2	RO	**Speech Flash Read Data 2.** Speech flash reading data bits [23:16].
A5h	SPEECHRD3	RO	**Speech Flash Read Data 3.** Speech flash reading data bits [31:24].

7.17 Flash Page count — Index A7h (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-5	Reserved		Reserved
4-0	Page count	RO	Flash (W55FXX) size of each page is 512K, so read these bits may know the flash size when finish page coding program.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 5V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

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DC Characteristics, continued

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PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

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8.3 AC Characteristics

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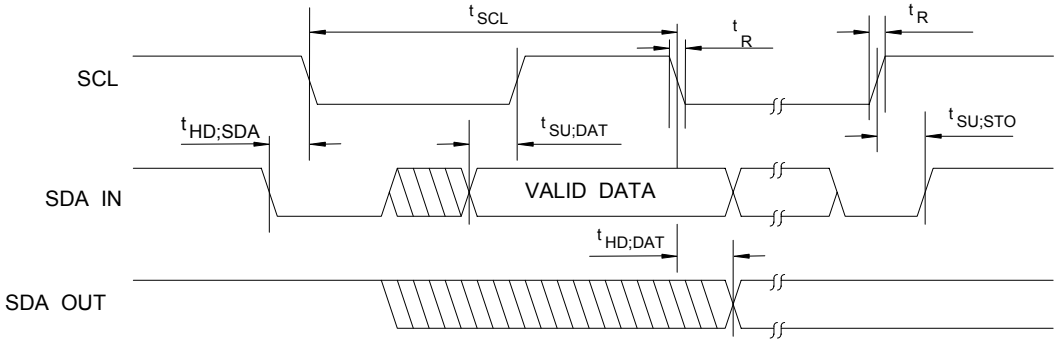
8.3.1 Serial Bus Timing Diagram



Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

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9. HOW TO READ THE TOP MARKING

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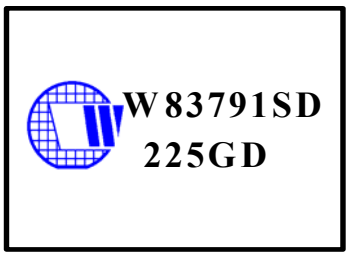
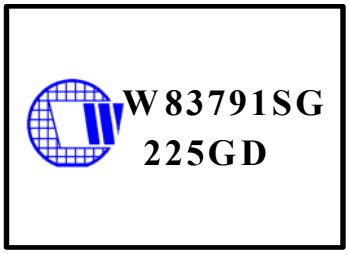
The top marking of W83791SD



Left: Winbond logo
1st line: part number W83791SD, D means LQFP (Thickness = 1.4 mm).
2nd line: Tracking code 025 GD

225: packages made in 2002, week 25
G: assembly house ID; A means ASE, O means OSE, G means Greatek.
D: IC revision; D means version D.

The top marking of W83791SG



Left: Winbond logo
1st line: part number W83791SG; G means lead-free package.
2nd line: Tracking code 225 GD

225: packages made in 2002, week 25
G: assembly house ID; A means ASE, O means OSE, G means Greatek
D: IC revision; D means version D.

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10. PACKAGE SPECIFICATION

48-pin LQFP

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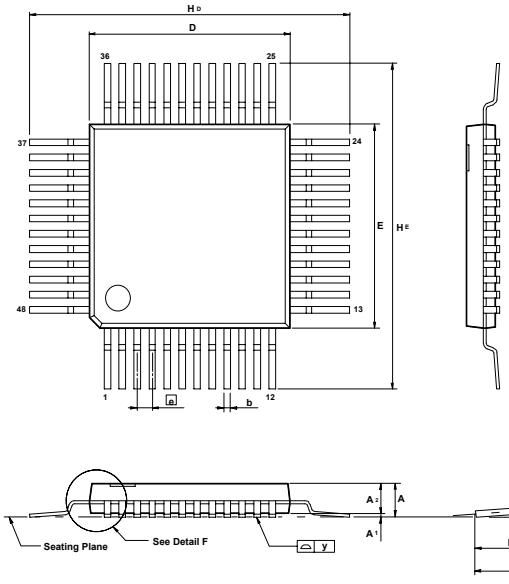

Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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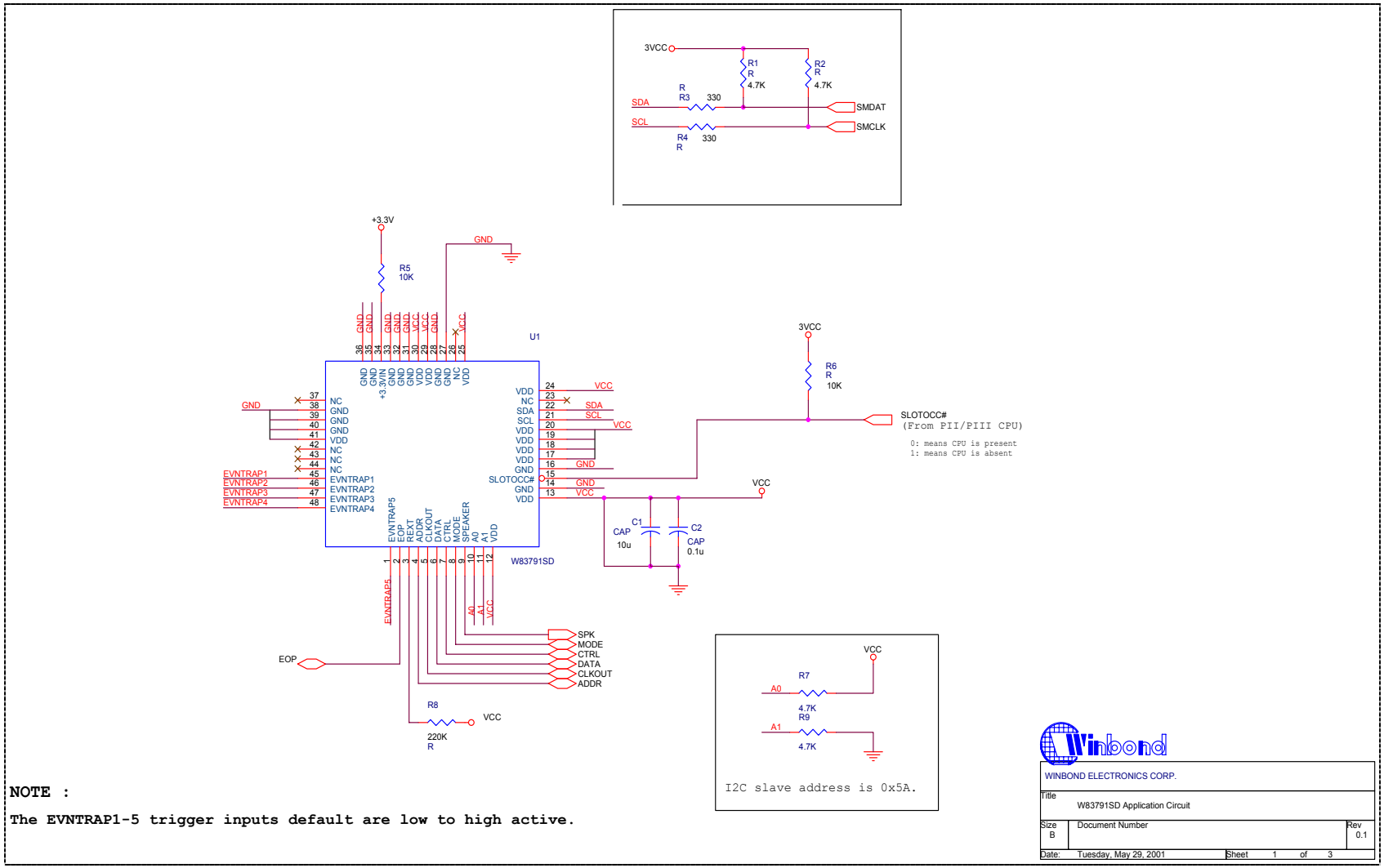
11. APPLICATION CIRCUITS



NOTE :

The EVNTRAP1-5 trigger inputs default are low to high active.

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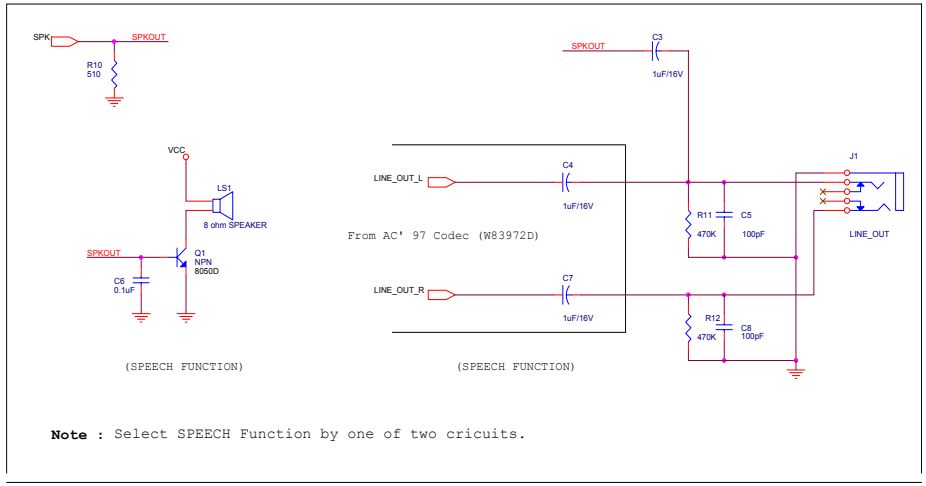

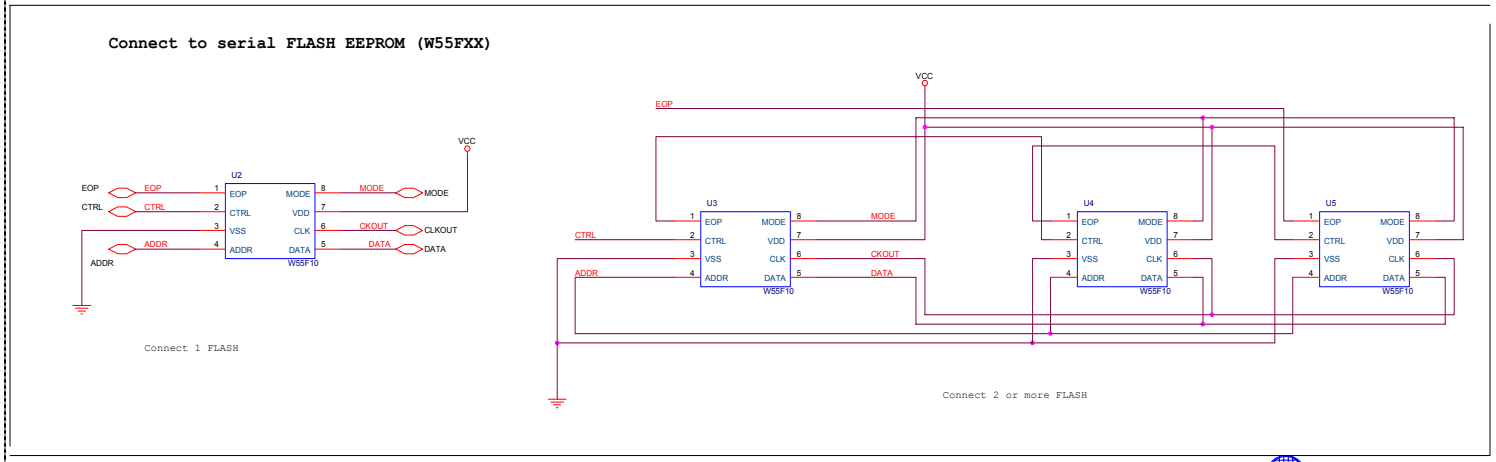

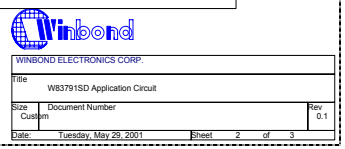

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0.1	First Publication

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Title: W83791SD Application circuit		
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