

## 256MB- 32Mx64 SDRAM UNBUFFERED

### FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V  $\pm$  0.3V Power Supply
- 168 pin DIMM JEDEC

### DESCRIPTION

The W3DG6432V is a 32Mx64 synchronous DRAM module which consists of eight 16Mx16 SDRAM components in TSOP II package and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 pin DIMM multilayer FR4 Substrate.

#### PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

| Pin | Front           | Pin | Front           | Pin | Front           | Pin | Back            | Pin | Back            | Pin | Back            |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|
| 1   | V <sub>ss</sub> | 29  | DQM1            | 57  | DQ18            | 85  | V <sub>ss</sub> | 113 | DQM5            | 141 | DQ50            |
| 2   | DQ0             | 30  | CS0#            | 58  | DQ19            | 86  | DQ32            | 114 | CS1#            | 142 | DQ51            |
| 3   | DQ1             | 31  | DNU             | 59  | V <sub>cc</sub> | 87  | DQ33            | 115 | RAS#            | 143 | V <sub>cc</sub> |
| 4   | DQ2             | 32  | V <sub>ss</sub> | 60  | DQ20            | 88  | DQ34            | 116 | V <sub>ss</sub> | 144 | DQ52            |
| 5   | DQ3             | 33  | A0              | 61  | NC              | 89  | DQ35            | 117 | A1              | 145 | NC              |
| 6   | V <sub>cc</sub> | 34  | A2              | 62  | NC              | 90  | V <sub>cc</sub> | 118 | A3              | 146 | NC              |
| 7   | DQ4             | 35  | A4              | 63  | CKE1            | 91  | DQ36            | 119 | A5              | 147 | DNU             |
| 8   | DQ5             | 36  | A6              | 64  | V <sub>ss</sub> | 92  | DQ37            | 120 | A7              | 148 | V <sub>ss</sub> |
| 9   | DQ6             | 37  | A8              | 65  | DQ21            | 93  | DQ38            | 121 | A9              | 149 | DQ53            |
| 10  | DQ7             | 38  | A10/AP          | 66  | DQ22            | 94  | DQ39            | 122 | BA0             | 150 | DQ54            |
| 11  | DQ8             | 39  | BA1             | 67  | DQ23            | 95  | DQ40            | 123 | A11             | 151 | DQ55            |
| 12  | V <sub>ss</sub> | 40  | V <sub>cc</sub> | 68  | V <sub>ss</sub> | 96  | V <sub>ss</sub> | 124 | V <sub>cc</sub> | 152 | V <sub>ss</sub> |
| 13  | DQ9             | 41  | V <sub>cc</sub> | 69  | DQ24            | 97  | DQ41            | 125 | NC              | 153 | DQ56            |
| 14  | DQ10            | 42  | CK0             | 70  | DQ25            | 98  | DQ42            | 126 | A12             | 154 | DQ57            |
| 15  | DQ11            | 43  | V <sub>ss</sub> | 71  | DQ26            | 99  | DQ43            | 127 | V <sub>ss</sub> | 155 | DQ58            |
| 16  | DQ12            | 44  | DNU             | 72  | DQ27            | 100 | DQ44            | 128 | CKE0            | 156 | DQ59            |
| 17  | DQ13            | 45  | CS2#            | 73  | V <sub>cc</sub> | 101 | DQ45            | 129 | CS3#            | 157 | V <sub>cc</sub> |
| 18  | V <sub>cc</sub> | 46  | DQM2            | 74  | DQ28            | 102 | V <sub>cc</sub> | 130 | DQM6            | 158 | DQ60            |
| 19  | DQ14            | 47  | DQM3            | 75  | DQ29            | 103 | DQ46            | 131 | DQM7            | 159 | DQ61            |
| 20  | DQ15            | 48  | DNU             | 76  | DQ30            | 104 | DQ47            | 132 | NC              | 160 | DQ62            |
| 21  | NC              | 49  | V <sub>cc</sub> | 77  | DQ31            | 105 | NC              | 133 | V <sub>cc</sub> | 161 | DQ63            |
| 22  | NC              | 50  | NC              | 78  | V <sub>ss</sub> | 106 | NC              | 134 | NC              | 162 | V <sub>ss</sub> |
| 23  | V <sub>ss</sub> | 51  | NC              | 79  | CK2             | 107 | V <sub>ss</sub> | 135 | NC              | 163 | NC              |
| 24  | NC              | 52  | NC              | 80  | NC              | 108 | NC              | 136 | NC              | 164 | NC              |
| 25  | NC              | 53  | NC              | 81  | *WP             | 109 | NC              | 137 | NC              | 165 | **SA0           |
| 26  | V <sub>cc</sub> | 54  | V <sub>ss</sub> | 82  | **SDA           | 110 | V <sub>cc</sub> | 138 | V <sub>ss</sub> | 166 | **SA1           |
| 27  | WE#             | 55  | DQ16            | 83  | **SCL           | 111 | CAS#            | 139 | DQ48            | 167 | **SA2           |
| 28  | DQM0            | 56  | DQ17            | 84  | V <sub>cc</sub> | 112 | DQM4            | 140 | DQ49            | 168 | V <sub>cc</sub> |

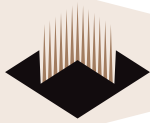
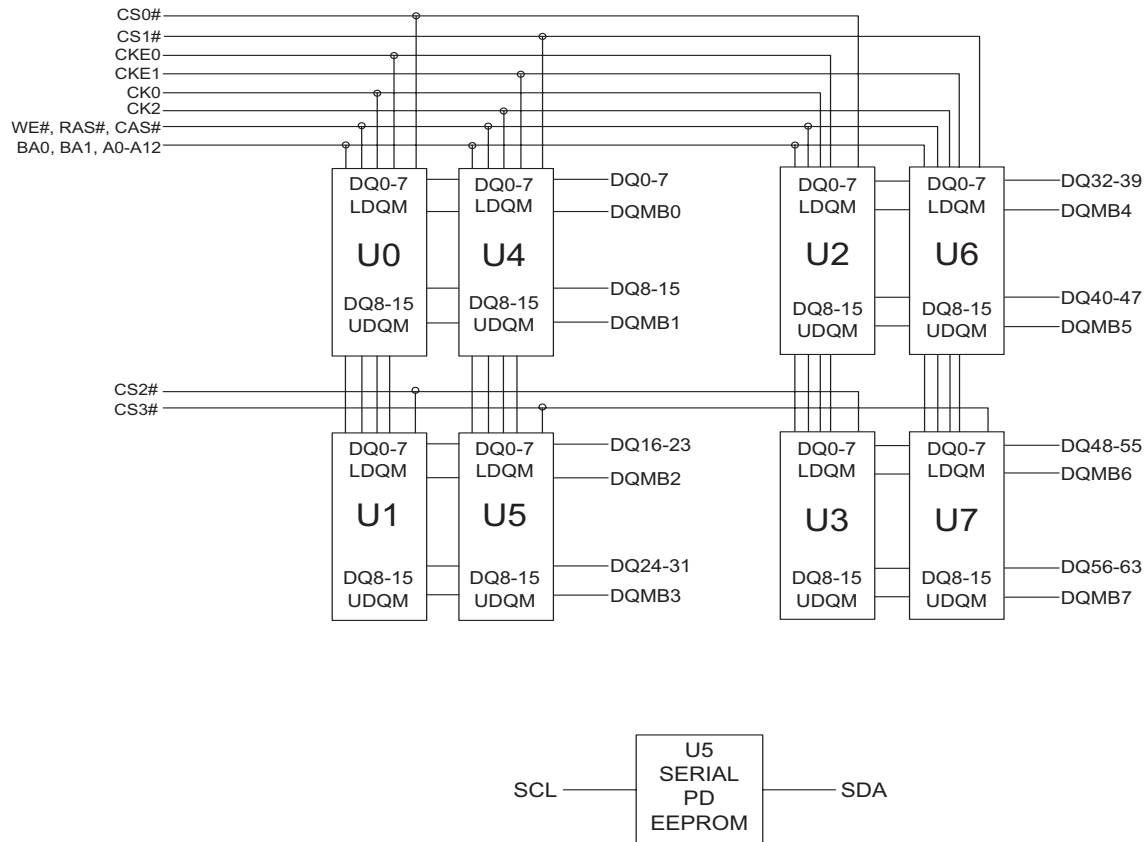
#### PIN NAMES

|                 |                             |
|-----------------|-----------------------------|
| A0 – A12        | Address input (Multiplexed) |
| BA0-1           | Select Bank                 |
| DQ0-63          | Data Input/Output           |
| CK0,CK2         | Clock input                 |
| CKE0,CKE1       | Clock Enable input          |
| CS0#-CS3#       | Chip select Input           |
| RAS#            | Row Address Strobe          |
| CAS#            | Column Address Strobe       |
| WE#             | Write Enable                |
| DQM0-7          | DQM                         |
| V <sub>cc</sub> | Power Supply (3.3V)         |
| V <sub>ss</sub> | Ground                      |
| SDA             | Serial data I/O             |
| SCL             | Serial clock                |
| DNU             | Do not use                  |
| NC              | No Connect                  |

- \* WP (write protect) option available on pin 81, see ordering information on page 5.
- \*\* These pins should be NC in the system which does not support SPD.

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**FUNCTIONAL BLOCK DIAGRAM**

**Absolute Maximum Ratings**

| Parameter                                                     | Symbol                             | Value      | Units |
|---------------------------------------------------------------|------------------------------------|------------|-------|
| Voltage on any pin relative to V <sub>SS</sub>                | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6 | V     |
| Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub> | V <sub>CC</sub> , V <sub>CCQ</sub> | -1.0 ~ 4.6 | V     |
| Storage Temperature                                           | T <sub>STG</sub>                   | -55 ~ +150 | °C    |
| Power Dissipation                                             | P <sub>D</sub>                     | 8          | W     |
| Short Circuit Current                                         | I <sub>OS</sub>                    | 50         | mA    |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(Voltage Referenced to: V<sub>SS</sub> = 0V, 0°C ≤ T<sub>A</sub> ≤ 70°C)

| Parameter             | Symbol          | Min  | Typ | Max                   | Unit | Note                   |
|-----------------------|-----------------|------|-----|-----------------------|------|------------------------|
| Supply Voltage        | V <sub>CC</sub> | 3.0  | 3.3 | 3.6                   | V    |                        |
| Input High Voltage    | V <sub>IH</sub> | 2.0  | 3.0 | V <sub>CCQ</sub> +0.3 | V    | 1                      |
| Input Low Voltage     | V <sub>IL</sub> | -0.3 | —   | 0.8                   | V    | 2                      |
| Output High Voltage   | V <sub>OH</sub> | 2.4  | —   | —                     | V    | I <sub>OH</sub> = -2mA |
| Output Low Voltage    | V <sub>OL</sub> | —    | —   | 0.4                   | V    | I <sub>OL</sub> = -2mA |
| Input Leakage Current | I <sub>LI</sub> | -10  | —   | 10                    | A    | 3                      |

Note: 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>CCQ</sub>  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

**Capacitance**(T<sub>A</sub> = 23°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub> = 1.4V ± 200mV)

| Parameter                                | Symbol           | Min | Max | Unit |
|------------------------------------------|------------------|-----|-----|------|
| Input Capacitance (A0-A12)               | C <sub>IN1</sub> | -   | 45  | pF   |
| Input Capacitance (RAS#,CAS#,WE#)        | C <sub>IN2</sub> | -   | 45  | pF   |
| Input Capacitance (CKE0)                 | C <sub>IN3</sub> | -   | 25  | pF   |
| Input Capacitance (CK0,CK2)              | C <sub>IN4</sub> | -   | 13  | pF   |
| Input Capacitance (CS0#,CS2#)            | C <sub>IN5</sub> | -   | 15  | pF   |
| Input Capacitance (DQM0-DQM7)            | C <sub>IN6</sub> | -   | 10  | pF   |
| Input Capacitance (BA0-BA1)              | C <sub>IN7</sub> | -   | 45  | pF   |
| Data input/output capacitance (DQ0-DQ63) | C <sub>OUT</sub> | -   | 12  | pF   |

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**OPERATING CURRENT CHARACTERISTICS**(V<sub>CC</sub> = 3.3V, 0°C ≤ T<sub>A</sub> ≤ 70°C)

| Parameters                                          | Symbol             | Conditions                                                                                                                        | Versions |     | Units | Note |
|-----------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------|----------|-----|-------|------|
|                                                     |                    |                                                                                                                                   | 133      | 100 |       |      |
| Operating Current<br>(One bank active)              | I <sub>CC1</sub>   | Burst Length = 1<br>t <sub>RC</sub> ≥ t <sub>RC(min)</sub><br>I <sub>OL</sub> = 0mA                                               | 740      | 700 | mA    | 1    |
| Precharge Standby Current<br>in Power Down Mode     | I <sub>CC2P</sub>  | CKE ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns                                                                               | 20       |     | mA    |      |
|                                                     | I <sub>CC2PS</sub> | CKE & CK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞                                                                             | 20       |     | mA    |      |
| Precharge Standby Current<br>in Non-Power Down Mode | I <sub>CC2N</sub>  | CKE ≥ V <sub>IH(min)</sub> , CS ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns<br>Input signals are charged one time during 20   | 130      |     | mA    |      |
|                                                     | I <sub>CC2NS</sub> | CKE ≥ V <sub>IH(min)</sub> , CK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞<br>Input signals are stable                          | 115      |     | mA    |      |
| Active standby current in power-<br>down mode       | I <sub>CC3P</sub>  | CKE ≥ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns                                                                               | 50       |     | mA    |      |
|                                                     | I <sub>CC3PS</sub> | CKE & CK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞                                                                             | 50       |     |       |      |
| Active standby in current non<br>power-down mode    | I <sub>CC3N</sub>  | CKE ≥ V <sub>IH(min)</sub> , CS ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns<br>Input signals are charged one time during 20ns | 280      |     | mA    |      |
|                                                     | I <sub>CC3NS</sub> | CKE ≥ V <sub>IH(min)</sub> , CK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞<br>input signals are stable                          | 240      |     | mA    |      |
| Operating current (Burst mode)                      | I <sub>CC4</sub>   | I <sub>O</sub> = mA<br>Page burst<br>4 Banks activated<br>t <sub>CCD</sub> = 2CK                                                  | 860      | 720 | mA    | 1    |
| Refresh current                                     | I <sub>CC5</sub>   | t <sub>RC</sub> ≥ t <sub>RC(min)</sub>                                                                                            | 980      | 940 | mA    | 2    |
| Self refresh current                                | I <sub>CC6</sub>   | CKE ≤ 0.2V                                                                                                                        | 40       |     | mA    |      |

Notes: 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Unless otherwise noticed, input swing level is CMOS (V<sub>IH</sub>/V<sub>IL</sub> = V<sub>CC</sub>/V<sub>SSQ</sub>)

