



## 256MB - 32M x 64 BUFFERED SDRAM MODULE

### FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V  $\pm$  0.3V Power Supply
- 168 pin DIMM JEDEC

### DESCRIPTION

The W3DG6430V is a 32M x 64 synchronous DRAM module which consists of sixteen 32Mx4 SDRAM components in TSOP II package, three very high speed buffers for reduced input capacitance, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 pin DIMM multilayer FR4 Substrate.

\* This product is not fully qualified or characterized and is subject to change without notice.

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### PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

| Pin | Front | Pin | Front  | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|-------|-----|--------|-----|-------|-----|------|-----|------|-----|------|
| 1   | Vss   | 29  | DQM1   | 57  | DQ18  | 85  | Vss  | 113 | DQM5 | 141 | DQ50 |
| 2   | DQ0   | 30  | CS0#   | 58  | DQ19  | 86  | DQ32 | 114 | NC   | 142 | DQ51 |
| 3   | DQ1   | 31  | DNU    | 59  | Vcc   | 87  | DQ33 | 115 | RAS# | 143 | Vcc  |
| 4   | DQ2   | 32  | Vss    | 60  | DQ20  | 88  | DQ34 | 116 | Vss  | 144 | DQ52 |
| 5   | DQ3   | 33  | A0     | 61  | NC    | 89  | DQ35 | 117 | A1   | 145 | NC   |
| 6   | Vcc   | 34  | A2     | 62  | NC    | 90  | Vcc  | 118 | A3   | 146 | NC   |
| 7   | DQ4   | 35  | A4     | 63  | NC    | 91  | DQ36 | 119 | A5   | 147 | NC   |
| 8   | DQ5   | 36  | A6     | 64  | Vss   | 92  | DQ37 | 120 | A7   | 148 | Vss  |
| 9   | DQ6   | 37  | A8     | 65  | DQ21  | 93  | DQ38 | 121 | A9   | 149 | DQ53 |
| 10  | DQ7   | 38  | A10/AP | 66  | DQ22  | 94  | DQ39 | 122 | BA0  | 150 | DQ54 |
| 11  | DQ8   | 39  | BA1    | 67  | DQ23  | 95  | DQ40 | 123 | A11  | 151 | DQ55 |
| 12  | Vss   | 40  | Vcc    | 68  | Vss   | 96  | Vss  | 124 | Vcc  | 152 | Vss  |
| 13  | DQ9   | 41  | Vcc    | 69  | DQ24  | 97  | DQ41 | 125 | CLK1 | 153 | DQ56 |
| 14  | DQ10  | 42  | CLK0   | 70  | DQ25  | 98  | DQ42 | 126 | NC   | 154 | DQ57 |
| 15  | DQ11  | 43  | Vss    | 71  | DQ26  | 99  | DQ43 | 127 | Vss  | 155 | DQ58 |
| 16  | DQ12  | 44  | DNU    | 72  | DQ27  | 100 | DQ44 | 128 | CKE0 | 156 | DQ59 |
| 17  | DQ13  | 45  | CS2#   | 73  | Vcc   | 101 | DQ45 | 129 | NC   | 157 | Vcc  |
| 18  | Vcc   | 46  | DQM2   | 74  | DQ28  | 102 | Vcc  | 130 | DQM6 | 158 | DQ60 |
| 19  | DQ14  | 47  | DQM3   | 75  | DQ29  | 103 | DQ46 | 131 | DQM7 | 159 | DQ61 |
| 20  | DQ15  | 48  | DNU    | 76  | DQ30  | 104 | DQ47 | 132 | NC   | 160 | DQ62 |
| 21  | NC    | 49  | Vcc    | 77  | DQ31  | 105 | NC   | 133 | Vcc  | 161 | DQ63 |
| 22  | NC    | 50  | NC     | 78  | Vss   | 106 | NC   | 134 | NC   | 162 | Vss  |
| 23  | Vss   | 51  | NC     | 79  | CK2   | 107 | Vss  | 135 | NC   | 163 | CLK3 |
| 24  | NC    | 52  | NC     | 80  | NC    | 108 | NC   | 136 | NC   | 164 | NC   |
| 25  | NC    | 53  | NC     | 81  | NC    | 109 | NC   | 137 | NC   | 165 | SA0  |
| 26  | Vcc   | 54  | Vss    | 82  | **SDA | 110 | Vcc  | 138 | Vss  | 166 | SA1  |
| 27  | WE#   | 55  | DQ16   | 83  | **SCL | 111 | CAS# | 139 | DQ48 | 167 | SA2  |
| 28  | DQM0  | 56  | DQ17   | 84  | Vcc   | 112 | DQM4 | 140 | DQ49 | 168 | Vcc  |

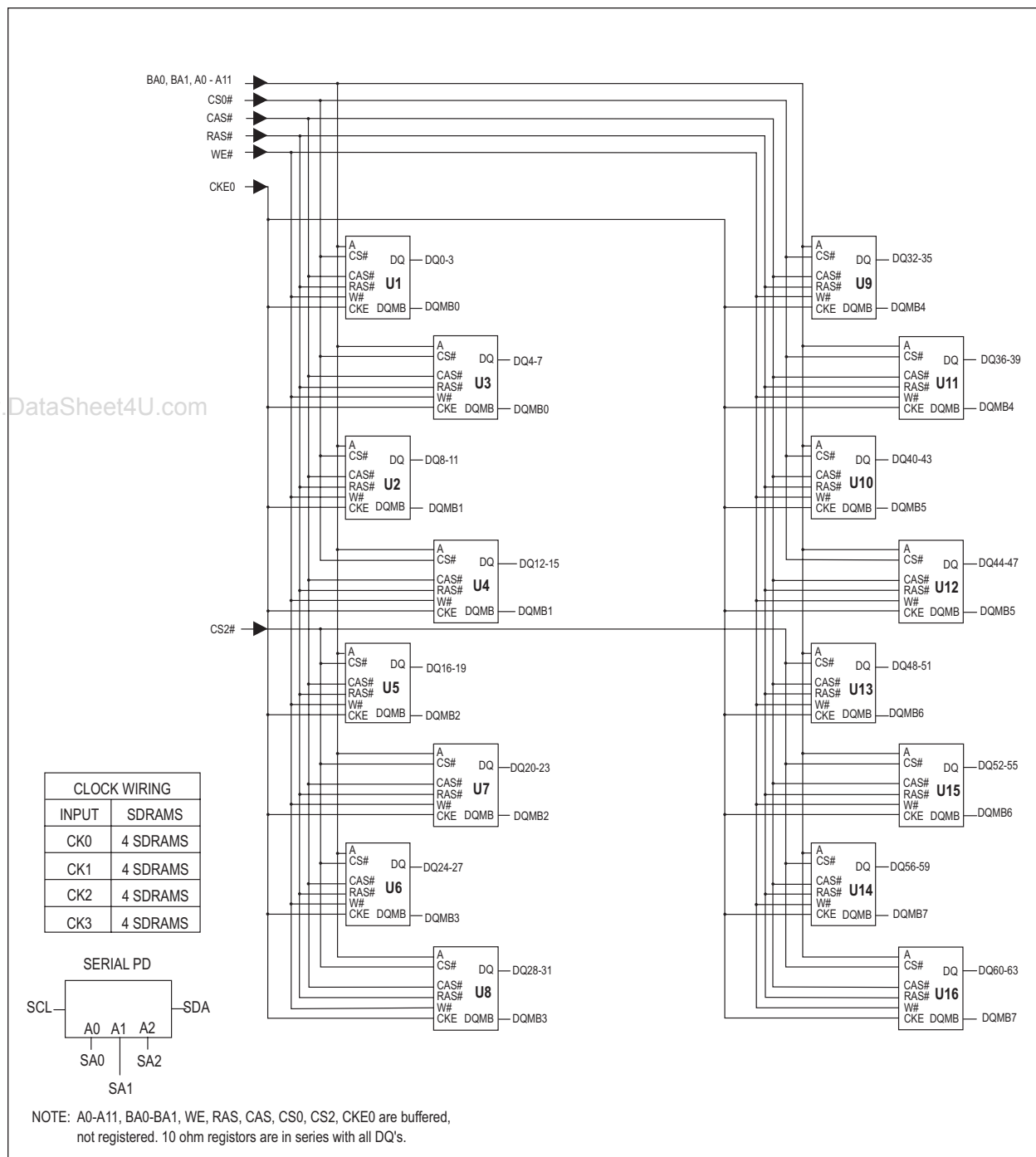
### PIN NAMES

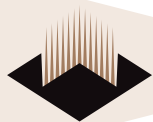
|           |                             |
|-----------|-----------------------------|
| A0 – A11  | Address input (Multiplexed) |
| BA0-1     | Select Bank                 |
| DQ0-63    | Data Input/Output           |
| CLK0,CLK3 | Clock input                 |
| CKE0      | Clock Enable input          |
| CS0#-CS2# | Chip select Input           |
| RAS#      | Row Address Strobe          |
| CAS#      | Column Address Strobe       |
| WE#       | Write Enable                |
| DQM0-7    | DQM                         |
| Vcc       | Power Supply (3.3V)         |
| Vss       | Ground                      |
| SDA       | Serial data I/O             |
| SCL       | Serial clock                |
| DNU       | Do not use                  |
| NC        | No Connect                  |
| SA0-SA2   | Address in EEPROM           |

\*\* These pins should be NC in the system which does not support SPD.



## FUNCTIONAL BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

| Parameter                                                     | Symbol                             | Value      | Units |
|---------------------------------------------------------------|------------------------------------|------------|-------|
| Voltage on any pin relative to V <sub>SS</sub>                | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6 | V     |
| Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub> | V <sub>CC</sub> , V <sub>CCQ</sub> | -1.0 ~ 4.6 | V     |
| Storage Temperature                                           | T <sub>STG</sub>                   | -55 ~ +150 | °C    |
| Power Dissipation                                             | P <sub>D</sub>                     | 8          | W     |
| Short Circuit Current                                         | I <sub>OS</sub>                    | 50         | mA    |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V<sub>SS</sub> = 0V, 0°C ≤ T<sub>A</sub> ≤ 70°C

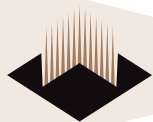
| Parameter             | Symbol          | Min  | Typ | Max                  | Unit | Note                   |
|-----------------------|-----------------|------|-----|----------------------|------|------------------------|
| Supply Voltage        | V <sub>CC</sub> | 3.0  | 3.3 | 3.6                  | V    |                        |
| Input High Voltage    | V <sub>IH</sub> | 2.0  | 3.0 | V <sub>CC</sub> +0.3 | V    |                        |
| Input Low Voltage     | V <sub>IL</sub> | -0.3 | —   | 0.8                  | V    |                        |
| Output High Voltage   | V <sub>OH</sub> | 2.4  | —   | —                    | V    | I <sub>OH</sub> = -2mA |
| Output Low Voltage    | V <sub>OL</sub> | —    | —   | 0.4                  | V    | I <sub>OL</sub> = -2mA |
| Input Leakage Current | I <sub>LI</sub> | -20  | —   | 20                   | A    | 1                      |

Note: 1. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>CC</sub> Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

T<sub>A</sub> = 23°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub>=1.4V ± 200mV

| Parameter                                | Symbol           | Max | Unit |
|------------------------------------------|------------------|-----|------|
| Input Capacitance (A0-A11)               | C <sub>IN1</sub> | 20  | pF   |
| Input Capacitance (RAS#,CAS#,WE#)        | C <sub>IN2</sub> | 20  | pF   |
| Input Capacitance (CKE0)                 | C <sub>IN3</sub> | 20  | pF   |
| Input Capacitance (CLK0,CLK2)            | C <sub>IN4</sub> | 13  | pF   |
| Input Capacitance (CS0#,CS2#)            | C <sub>IN5</sub> | 15  | pF   |
| Input Capacitance (DQM0-DQM7)            | C <sub>IN6</sub> | 10  | pF   |
| Input Capacitance (BA0-BA1)              | C <sub>IN7</sub> | 20  | pF   |
| Data input/output capacitance (DQ0-DQ63) | C <sub>OUT</sub> | 12  | pF   |



## OPERATING CURRENT CHARACTERISTICS

$$V_{CC} = 3.3V, 0^{\circ}C \leq T_A \leq 70^{\circ}C$$

| Parameters                                          | Symbol             | Conditions                                                                                                         | Versions | Units | Note |
|-----------------------------------------------------|--------------------|--------------------------------------------------------------------------------------------------------------------|----------|-------|------|
|                                                     |                    |                                                                                                                    | 100      |       |      |
| Operating Current<br>(One bank active)              | I <sub>CC1</sub>   | Burst Length = 1<br>$t_{RC} \geq t_{RC(min)}$<br>$I_{OL} = 0mA$                                                    | 1700     | mA    | 1    |
| Precharge Standby Current<br>in Power Down Mode     | I <sub>CC2P</sub>  | $CKE \leq V_{IL(max)}$ , $t_{CC} = 10ns$                                                                           | 40       | mA    |      |
|                                                     | I <sub>CC2PS</sub> | $CKE \& CK \leq V_{IL(max)}$ , $t_{CC} = \infty$                                                                   | 40       | mA    |      |
| Precharge Standby Current<br>in Non-Power Down Mode | I <sub>CC2N</sub>  | $CKE \geq V_{IH(min)}$ , $CS \geq V_{IH(min)}$ , $t_{CC} = 10ns$<br>Input signals are charged one time during 20   | 350      | mA    |      |
|                                                     | I <sub>CC2NS</sub> | $CKE \geq V_{IH(min)}$ , $CK \leq V_{IL(max)}$ , $t_{CC} = \infty$<br>Input signals are stable                     | 180      | mA    |      |
| Active standby current in power-<br>down mode       | I <sub>CC3P</sub>  | $CKE \geq V_{IL(max)}$ , $t_{CC} = 10ns$                                                                           | 90       | mA    |      |
|                                                     | I <sub>CC3PS</sub> | $CKE \& CK \leq V_{IL(max)}$ , $t_{CC} = \infty$                                                                   | 90       |       |      |
| Active standby in current non power-<br>down mode   | I <sub>CC3N</sub>  | $CKE \geq V_{IH(min)}$ , $CS \geq V_{IH(min)}$ , $t_{CC} = 10ns$<br>Input signals are charged one time during 20ns | 500      | mA    |      |
|                                                     | I <sub>CC3NS</sub> | $CKE \geq V_{IH(min)}$ , $CK \leq V_{IL(max)}$ , $t_{CC} = \infty$<br>input signals are stable                     | 500      | mA    |      |
| Operating current (Burst mode)                      | I <sub>CC4</sub>   | $I_O = mA$<br>Page burst<br>4 Banks activated<br>$t_{CCD} = 2CK$                                                   | 1700     | mA    | 1    |
| Refresh current                                     | I <sub>CC5</sub>   | $t_{RC} \geq t_{RC(min)}$                                                                                          | 3300     | mA    | 2    |
| Self refresh current                                | I <sub>CC6</sub>   | $CKE \leq 0.2V$                                                                                                    | 40       | mA    |      |

Notes: 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Unless otherwise noticed, input swing level is CMOS ( $V_{IH}/V_{IL} = V_{CC}/V_{SSQ}$ )



### AC CHARACTERISTICS

|                                        |        |                  | 133MHz component timing |         |       |       |
|----------------------------------------|--------|------------------|-------------------------|---------|-------|-------|
| Paramater                              |        | Symbol           | Min                     | Max     | Units | Notes |
| Access time from CLK                   | CL = 2 | t <sub>AC</sub>  |                         | 5.4     | ns    |       |
| Address hold time                      |        | t <sub>AH</sub>  | 0.8                     |         | ns    |       |
| Address setup time                     |        | t <sub>AS</sub>  | 1.5                     |         | ns    |       |
| CLK high level width                   |        | t <sub>CH</sub>  | 2.5                     |         | ns    |       |
| CLK low level width                    |        | t <sub>CL</sub>  | 2.5                     |         | ns    |       |
| Clock cycle time                       | CL = 2 | t <sub>CK</sub>  | 7.5                     |         | ns    | 1     |
| CKE hold time                          |        | t <sub>CKH</sub> | 0.8                     |         | ns    |       |
| CKE setup time                         |        | t <sub>CKS</sub> | 1.5                     |         | ns    |       |
| CS, RAS, CAS, WE, DQM hold time        |        | t <sub>CMH</sub> | 0.8                     |         | ns    |       |
| CS, RAS, CAS, WE, DQM setup time       |        | t <sub>CMS</sub> | 1.5                     |         | ns    |       |
| Data-in hold time                      |        | t <sub>DH</sub>  | 0.8                     |         | ns    |       |
| Data-in setup time                     |        | t <sub>DS</sub>  | 1.5                     |         | ns    |       |
| Data-out high-impedance time           | CL = 2 | t <sub>HZ</sub>  |                         | 5.4     | ns    | 2     |
| Data-out low-impedance time            |        | t <sub>LZ</sub>  | 1                       |         | ns    |       |
| Data-out hold time (load)              |        | t <sub>OH</sub>  | 3                       |         | ns    |       |
| Data-out hold time (no load)           |        | t <sub>ON</sub>  | 1.8                     |         | ns    | 3     |
| Active to Precharge command            |        | t <sub>RAS</sub> | 37                      | 120,000 | ns    |       |
| Active to Active command period        |        | t <sub>RC</sub>  | 60                      |         | ns    |       |
| Active to Read or Write delay          |        | t <sub>RCD</sub> | 15                      |         | ns    |       |
| Refresh period                         |        | t <sub>REF</sub> |                         | 64      | ms    |       |
| Autot refresh period                   |        | t <sub>RFC</sub> | 66                      |         | ns    |       |
| Precharge command period               |        | t <sub>RP</sub>  | 15                      |         | ns    |       |
| Active bank a to Active bank b command |        | t <sub>RBD</sub> | 14                      |         | ns    |       |
| Transition time                        |        | t <sub>tr</sub>  | 0.3                     | 1.2     | ns    | 4     |
| Write recovery time                    |        | t <sub>WR</sub>  | 1 CLK + 7ns             |         | ns    | 5     |
|                                        |        |                  |                         |         | ns    | 6     |
| Exit Self Refresh to Active command    |        | t <sub>XSR</sub> | 67                      |         | ns    | 7     |

#### Notes:

1. The clock frequency must remain constant ( stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including WR and Precharge commands). CKE may be used to reduce the data rate.
2. t<sub>HZ</sub> defines the time at which the output achieves the open circuit condition; it is not a reference to V<sub>OH</sub> or V<sub>OL</sub>. The last valid data element will meet t<sub>OH</sub> before going High-Z.
3. Paramater guaranteed by design
4. AC characteristics assume t<sub>tr</sub> = 1ns
5. Auto precharge mode only) The precharge timing budget ( t<sub>RP</sub>) begins 7ns after the first clock delay, after the last Write is executed.
6. Precharge mode only.
7. CLK must be toggled a minimum of two times during this period.

### MODULE AC CHARACTERISTIC

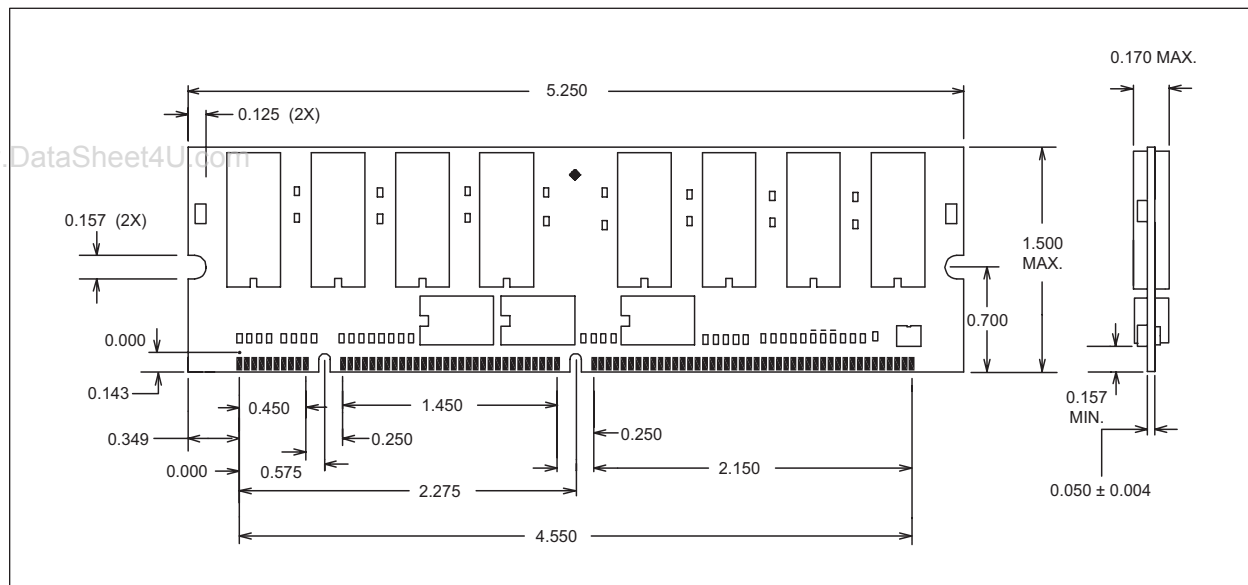
|                                  | Symbol | Min | Max | Units | Notes |
|----------------------------------|--------|-----|-----|-------|-------|
| Address hold time                | AH     | 0   |     | ns    |       |
| Address setup time               | AS     | 4.5 |     | ns    |       |
| CS, RAS, CAS, WE, DQM hold time  | CMH    | 0   |     | ns    |       |
| CS, RAS, CAS, WE, DQM setup time | CMS    | 4.5 |     | ns    |       |



### ORDERING INFORMATION

| Part Number   | Speed  | CAS Latency |
|---------------|--------|-------------|
| W3DG6430V10D2 | 100MHz | CL=2        |

### PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES