1GB – 2x64Mx64 SDRAM, UNBUFFERED w/PLL

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 144 Pin SO-DIMM
  - PBC height: 31.75 (1.25")

DESCRIPTION

The W3DG64128V is a 2x64Mx64 synchronous DRAM module which consists of eight 128Mx8 stack of SDRAM components in TSOP II package, and one 2Kb EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate. This module is structured as 2 Ranks of 64Mx64 SDRAM.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:
- RoHS Products
- Vendor source control options
- Industrial temperature option

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

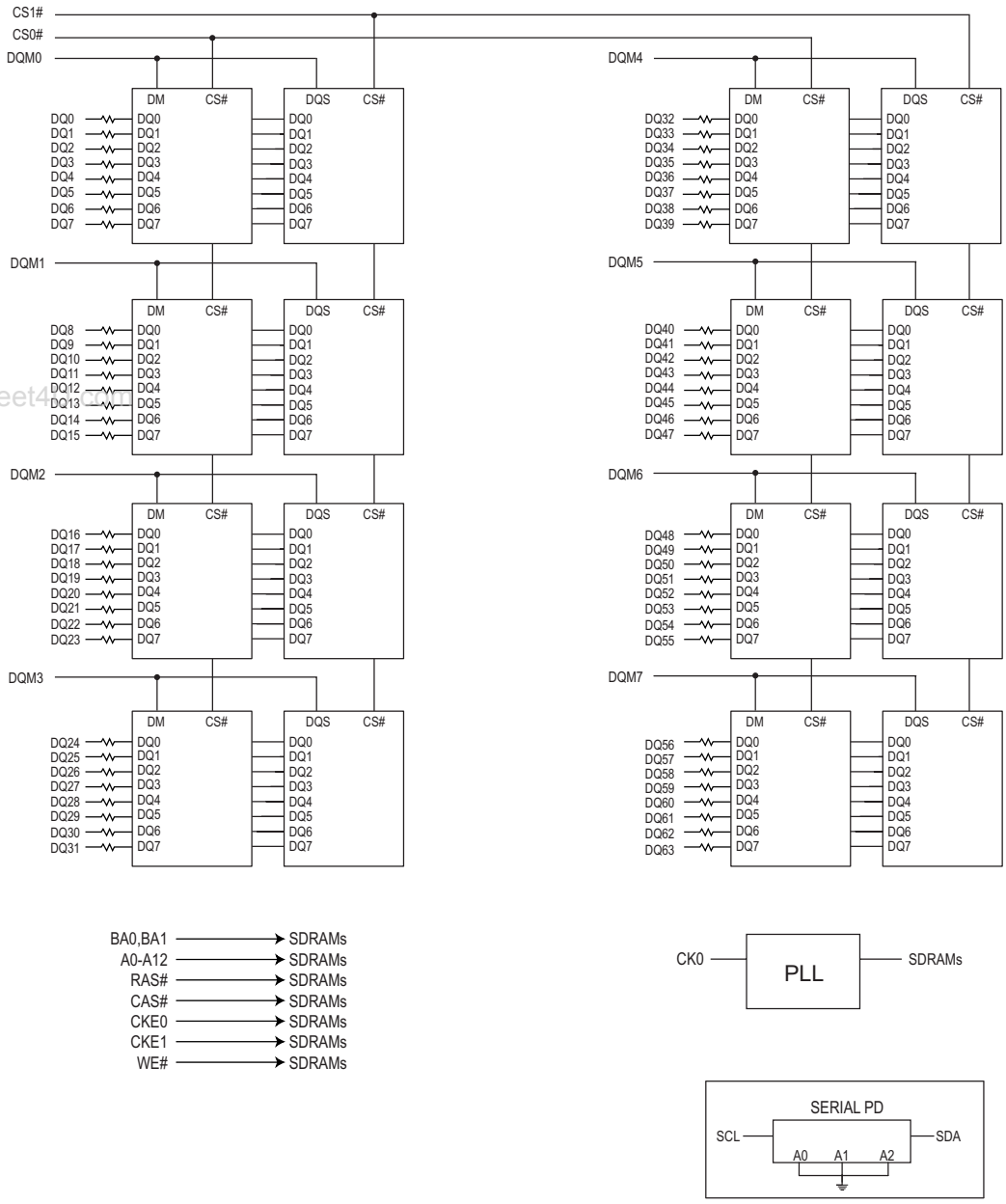
PINOUT											
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	BA0
11	Vcc	12	Vcc	59	NC	60	NC	107	Vss	108	Vss
13	DQ4	14	DQ36	61	CK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS#	66	CAS#	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	WE#	68	CKE1	115	DQMB2	116	DQMB6
21	Vss	22	Vss	69	CS0#	70	A12	117	DQMB3	118	DQMB7
23	DQM0	24	DQM4	71	CS1#	72	NC	119	Vss	120	Vss
25	DQM1	26	DQM5	73	NC	74	NC	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

PIN NAMES

A0 – A12	Address Input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CK0	Clock Input
CKE0, CKE1	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
Vcc	Power Supply (3.3V)
Vss	Ground
SDA	Serial Data I/O
SCL	Serial Clock
DNU	Do Not Use
NC	No Connect

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	18	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS"V are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, T_A = 0°C ≤ +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	$V_{CCQ+0.3}$	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	66	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	66	pF
Input Capacitance (CKE0)	C_{IN3}	35	pF
Input Capacitance (CLK0)	C_{IN4}	5.5	pF
Input Capacitance (CS0#)	C_{IN5}	35	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	11	pF
Input Capacitance (BA0-BA1)	C_{IN7}	66	pF
Data Input/Output Capacitance (DQ0-DQ63)	C_{OUT}	15	pF

OPERATING CURRENT CHARACTERISTICS

V_{CC} = 3.3V, 0°C ≤ T_A ≤ +70°C

			Version		
Parameter	**Symbol**	**Conditions**	**133/100**	**Units**	**Note**
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0mA	1,440	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	32	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	32		
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), tcc =10ns Input signals are charged one time during 20	320	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	160		
Active Standby Current in Power-Down Mode	I_{CC3P}	CKE ≥ V_{IL}(max), t_{CC} = 10ns	96	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	96		
Active Standby Current in Non-Power Down Mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns	480	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable	400	mA	
Operating Current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CLK	1,600	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3,200	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	96	mA	

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

AC TIMING PARAMETERS

Symbol	Parameter		Speed Grade 100MHz Min	Speed Grade 100MHz Max	Speed Grade 133MHz Min	Speed Grade 133MHz Max	Units	Notes
t_{CK}	Clock Period		10		7.5		ns	
t_{CH}	Clock High Time Rated @1.5V		3		2.5		ns	
t_{CL}	Clock Low Time		3		2.5		ns	
t_{IS}	Input Setup Times	Address/ Command & CKE	2		1.5		ns	
		Data	2		1.5		ns	
t_{IH}	Input Hold Times	Address/Command & CKE	1		0.8		ns	
		Data	1		0.8		ns	
t_{AC}	Output Valid From Clock	CAS# Latency = 2 or 3, LVTTL levels, Rated @ 50 pF all outputs switching		6.0 (tco = 5.2)		5.4 (tco = 4.6)	ns	1
t_{OH}	Output Hold From Clock Rated @ 50 pF (1.8 ns @ 0 pf)		3		2.7		ns	
t_{OHZ}	Output Valid to Z		3	9	2.7	7	ns	
t_{CCD}	CAS to CAS Delay		1		1		t_{CK}	
t_{CBD}	CAS Bank Delay		1		1		t_{CK}	
t_{CKE}	CKE to Clock Disable		1		1		t_{CK}	
t_{RP}	RAS Precharge Time		20		20		ns	
t_{RAS}	RAS Active Time		50		45		ns	
t_{RCD}	Activate to Command Delay (RAS to CAS Delay)		20		20		ns	
t_{RRD}	RAS to RAS Bank Activate Delay		20		15		ns	
t_{RC}	RAS Cycle Time		70		67.5		ns	
t_{DQD}	DQM to Input Data Delay		0		0		t_{CK}	
t_{DWD}	Write Cmd. to Input Data Delay		0		0		t_{CK}	
t_{MRD}	Mode Register set to Active delay		3		3		t_{CK}	
t_{ROH}	Precharge to O/P in High Z			CL		CL	t_{CK}	2
t_{DQZ}	DQM to Data in High Z for read		2		2		t_{CK}	
t_{DQM}	DQM to Data mask for write		0		0		t_{CK}	3
t_{DPL}	Data-in to PRE Command Period		20		15		ns	
t_{DAL}	Data-in to ACT (PRE) Command period (Auto precharge)		5		5		t_{CK}	
t_{SB}	Power Down Mode Entry			1		1	t_{CK}	
t_{SRX}	Self Refresh Exit Time		10		10		ns	4
t_{PDE}	Power Down Exit Set up Time		1		1		t_{CK}	5
t_{CKSTP}	Clock Stop During Self Refresh or Power Down		200		200		t_{CK}	6
t_{REF}	Refresh Period			64		64	ms	
t_{RFC}	Row Refresh Cycle Time		80.0		75.0		ns	

1. Access times to be measured w/input signals of 1 V/ns edge rate, 0.8 V to 2.0 V, tCO is clock to output with no load.
2. CL = CAS Latency
3. Data Masked on the same clock
4. Self refresh Exit is asynchronous, requiring 10 ns to ensure initiation. Self refresh exit is complete in 10 ns + tRC.
5. Timing is asynchronous. If tIS is not met by rising edge of CK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.

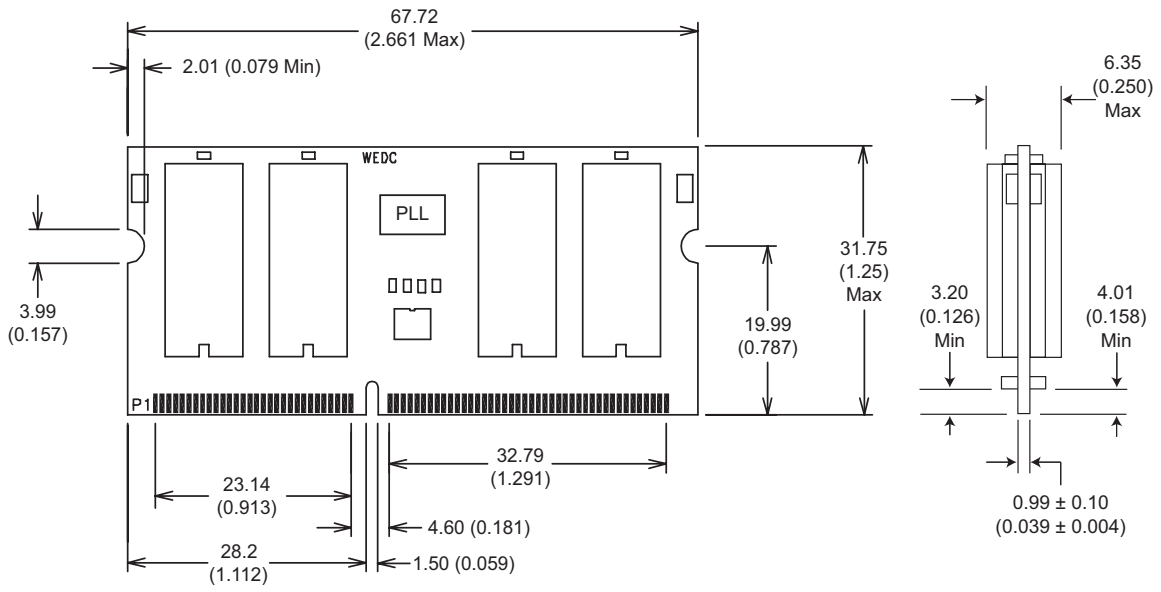
PACKAGE DIMENSIONS FOR D1

Ordering Information	Speed	CAS Latency	Height*
W3DG64128V10D1	100MHz	CL=2	31.75 (1.25")
W3DG64128V7D1	133MHz	CL=2	31.75 (1.25")
W3DG64128V75D1	133MHz	CL=3	31.75 (1.25")

NOTES:

- Consult Factory for availability of RoHS products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D1



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 0	Created Datasheet	6-03	Advanced
Rev 1	1.1 Updated Datasheet 1.2 Removed ED from part marking	5-04	Preliminary
Rev 2	2.1 Added lead-free and RoHS options 2.2 Added source control option 2.3 Added industrial temperature option 2.4 Added AC specs	5-05	Preliminary