

## 128K × 8 CMOS FLASH MEMORY

#### **GENERAL DESCRIPTION**

The W29EE011 is a 1-megabit, 5-volt only CMOS flash memory organized as  $128K \times 8$  bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W29EE011 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

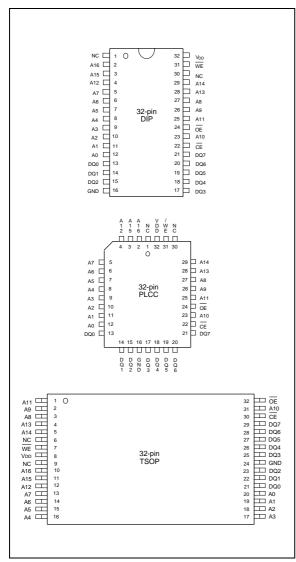
#### **FEATURES**

- Single 5-volt program and erase operations
- · Fast page-write operations
  - 128 bytes per page
  - Page program cycle: 10 mS (max.)
  - Effective byte-program cycle time: 39 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 90/150 nS
- Page program/erase cycles: 1K/10K
- Ten-year data retention
- · Software and hardware data protection

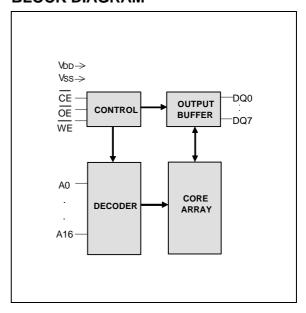
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program timing with internal VPP generation
- End of program detection
  - Toggle bit
  - Data polling
- · Latched address and data
- TTL compatible I/O
- · JEDEC standard byte-wide pinouts
- Available packages: 32-pin 600 mil DIP, TSOP, and PLCC



### **PIN CONFIGURATIONS**



### **BLOCK DIAGRAM**



#### PIN DESCRIPTION

SYMBOL	PIN NAME
A0-A16	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
CE	Chip Enable
ŌĒ	Output Enable
WE	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection



#### **FUNCTIONAL DESCRIPTION**

#### **Read Mode**

The read operation of the W29EE011 is controlled by  $\overline{CE}$  and  $\overline{OE}$ , both of which have to be low for the host to obtain data from the outputs.  $\overline{CE}$  is used for device selection. When  $\overline{CE}$  is high, the chip is de-selected and only standby power will be consumed.  $\overline{OE}$  is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is high. Refer to the timing waveforms for further details.

#### **Page Write Mode**

The W29EE011 is programmed on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing  $\overline{CE}$  and  $\overline{WE}$  low and  $\overline{OE}$  high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ , whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (TBLC) of 200  $\mu$ S, after the initial byte-load cycle, the W29EE011 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is loaded into the page buffer within 300  $\mu$ S (TBLCO) from the last byte-load cycle, i.e., there is no subsequent  $\overline{\text{WE}}$  high-to-low transition after the last rising edge of  $\overline{\text{WE}}$ . A7 to A16 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

#### **Software-protected Data Write**

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-byte program commands (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29EE011 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required. See Table 3 for specific codes and Figure 10 for the timing diagram.

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#### **Hardware Data Protection**

The integrity of the data stored in the W29EE011 is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A WE pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming operation is inhibited when VDD is less than 3.8V.
- (3) Write Inhibit Mode: Forcing OE low, CE high, or WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

#### Data Polling (DQ7)-Write Status Detection

The W29EE011 includes a data polling feature to indicate the end of a programming cycle. When the W29EE011 is in the internal programming cycle, any attempt to read DQ7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the programming cycle is completed. DQ7 will show the true data.

#### Toggle Bit (DQ6)-Write Status Detection

In addition to data polling, the W29EE011 provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

#### 5-Volt-only Software Chip Erase

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

#### **Product Identification**

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (DAh). A read from address 0001H outputs the device code (C1h). The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing CE and  $\overline{\text{OE}}$  low,  $\overline{\text{WE}}$  high, and raising A9 to 12 volts.



## **TABLE OF OPERATING MODES**

## **Operating Mode Selection**

Operating Range = 0 to 70°C (Ambient Temperature), VDD = 5V  $\pm 10\%$ , VSS = 0V, VHH = 12V

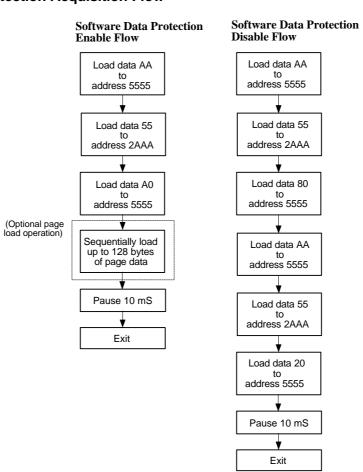
MODE		PINS				
	CE	ŌE	WE	ADDRESS	DQ.	
Read	VIL	VIL	VIH	AIN	Dout	
Write	VIL	VIH	VIL	AIN	Din	
Standby	VIH	Χ	Х	X	High Z	
Write Inhibit	Х	VIL	Х	X	High Z/DOUT	
	X	Χ	VIH	X	High Z/Dout	
Output Disable	X	VIH	Х	X	High Z	
5-Volt Software Chip Erase	VIL	VIH	VIL	AIN	DIN	
Product ID	VIL	VIL	VIH	A0 = VIL; A1-A16 = VIL; A9 = VHH	Manufacturer Code DA (Hex)	
	VIL	VIL	VIH	A0 = VIH; A1-A16 = VIL; A9 = VHH	Device Code C1 (Hex)	



#### **Command Codes for Software Data Protection**

BYTE SEQUENCE	TO ENABLE PROT	ECTION	TO DISABLE PRO	TECTION
	ADDRESS	ADDRESS DATA		DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write	-	-	5555H	AAH
4 Write	-			55H
5 Write	-	-	5555H	20H

### **Sofware Data Protection Acquisition Flow**



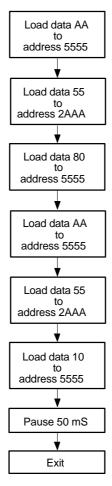
Notes for software program code: Data Format: DQ7–DQ0 (Hex) Address Format: A14–A0 (Hex)



### **Command Codes for Software Chip Erase**

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	ААН
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	ААН
4 Write	2AAAH	55H
5 Write	5555H	10H

## **Sofware Chip Erase Acquisition Flow**



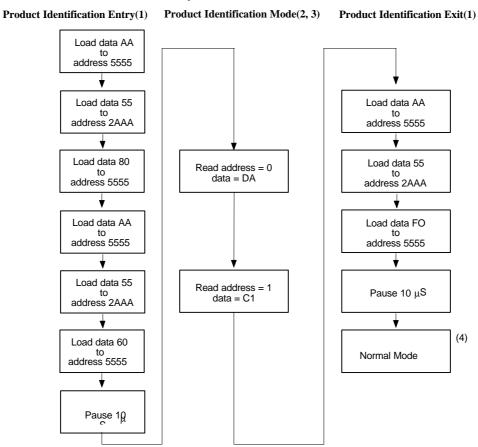
Notes for software chip erase: Data Format: DQ7–DQ0 (Hex) Address Format: A14–A0 (Hex)



#### **Command Codes for Product Identification**

BYTE SEQUENCE	SOFTWARE PRODUCT IDENTIFICATION ENTRY			SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS DATA		ADDRESS	DATA	
0 Write	5555H	AAH	5555H	AAH	
1 Write	2AAAH	55H	2AAAH	55H	
2 Write	5555H	80H	5555H	F0H	
3 Write	5555H	AAH	-	=	
4 Write	2AAAH	55H	-	=	
5 Write	5555H	60H			
	Pause	10 μS	Pause	10 μS	

### **Software Product Identification Acquisition Flow**



Notes for software product identification:

- (1) Data format: DQ7-DQ0 (Hex); address format: A14-A0 (Hex).
- (2) A1-A16 = VIL; manufacture code is read for A0 = VIL; device code is read for A0 = VIH.
- (3) The device does not remain in identification mode if power down.
- (4) The device returns to standard operation mode.



## **DC CHARACTERISTICS**

## **Absolute Maximum Ratings**

PARAMETER	RATING	UNIT
Power Supply Voltage to Vss Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except OE	-0.5 to VDD +1.0	V
Transient Voltage (< 20 nS ) on Any Pin to Ground Potential	-1.0 to VDD +1.0	V
Voltage on OE Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## **Operating Characteristics**

(VDD =  $5.0V \pm 10\%$ , Vss = 0V, Ta = 0 to  $70^{\circ}$  C)

PARAMETER	SYM.	TEST CONDITIONS		LIMITS		UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	ICC	CE = OE = VIL, WE = VIH, all I/Os open	-	-	50	mA
		Address inputs = VIL/VIH, at f = 5 MHz				
Standby VDD	ISB1	CE = VIH, all I/Os open	-	2	3	mA
Current (TTL input)		Other inputs = VIL/VIH				
Standby VDD Current	ISB2	CE = VDD -0.3V, all I/Os open	-	20	100	μΑ
(CMOS input)		Other inputs = VDD -0.3V/GND				
Input Leakage Current	ļLI	VIN = GND to VDD	-	-	1	μΑ
Output Leakage Current	<b>I</b> LO	VIN = GND to VDD	-	-	10	μА
Input Low Voltage	VIL	-	-0.3	-	8.0	V
Input High Voltage	VIH	-	2.0	-	VDD +0.5	V
Output Low Voltage	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage	Voн	IOH = -0.4 mA	2.4	-	-	V

### **Power-up Timing**

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU.READ	100	μS
Power-up to Write Operation	TPU.WRITE	5	mS

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### **CAPACITANCE**

 $(VDD = 5.0V, TA = 25^{\circ} C, f = 1 MHz)$ 

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	CI/O	VI/O = 0V	12	pF
Input Capacitance	CIN	VIN = 0V	6	pF

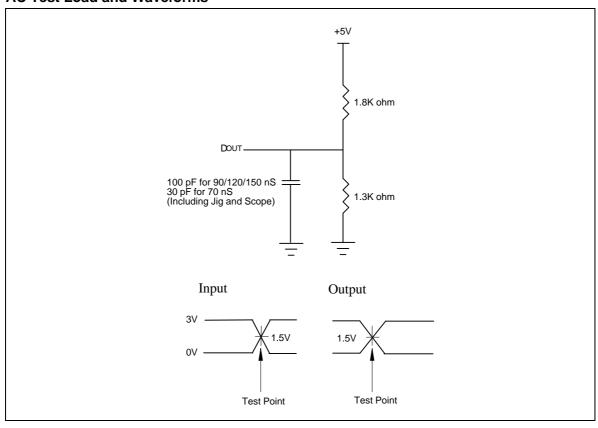
## **AC CHARACTERISTICS**

### **AC Test Conditions**

 $(VDD = 5V \pm 10\%)$ 

PARAMETER	CONDITIONS
Input Pulse Levels	OV to 3V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and CL = 30 pF for 70 nS and 100 pF for others.

### **AC Test Load and Waveforms**





### **Read Cycle Timing Parameters**

 $(Vcc = 5.0V \pm 10\%, Vcc = 5.0 \pm 5\% \text{ for 70 nS}, Vss = 0V, Ta = 0 \text{ to } 70^{\circ} \text{ C})$ 

PARAMETER	SYM.	W29EE011-90		W29EE011-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	Trc	90	-	150	-	nS
Chip Enable Access Time	TCE	-	90	-	150	nS
Address Access Time	TAA	-	90	-	150	nS
Output Enable Access Time	Toe	-	45	-	70	nS
CE Low to Active Output	Tclz	0	-	0	-	nS
OE Low to Active Output	Tolz	0	-	0	-	nS
CE High to High-Z Output	Тснz	-	45	-	45	nS
OE High to High-Z Output	Тонz	-	45	-	45	nS
Output Hold from Address Change	Тон	0	-	0	-	nS

## **Byte/Page-write Cycle Timing Parameters**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (Erase and Program)	Twc	-	-	10	mS
Address Setup Time	Tas	0	-	-	nS
Address Hold Time	Тан	50	-	-	nS
WE and CE Setup Time	Tcs	0	-	-	nS
WE and CE Hold Time	Тсн	0	-	-	nS
OE High Setup Time	Toes	10	-	-	nS
OE High Hold Time	Тоен	10	-	-	nS
CE Pulse Width	Тср	70	-	-	nS
WE Pulse Width	Twp	70	-	-	nS
WE High Width	Twph	150	-	-	nS
Data Setup Time	Tos	50	-	-	nS
Data Hold Time	TdH	10	-	-	nS
Byte Load Cycle Time	TBLC	0.22	-	200	μS
Byte Load Cycle Time-out	Твьсо	300	-	-	μS

Note: All AC timing signals observe the following guidelines for determining setup and hold times: (a) High level signal's reference level is VIH and (b) low level signal's reference level is VIL.

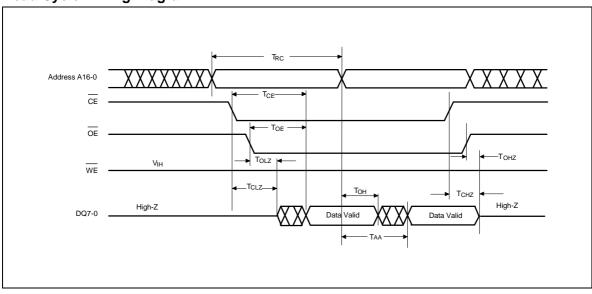


## **Data Polling and Toggle Bit Timing Parameters**

PARAMETER	SYM.	W29EE011-90		W29EE011-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
OE to Data Polling Output Delay	TOEP	-	45	-	70	nS
CE to Data Polling Output Delay	ТСЕР	-	90	-	150	nS
OE to Toggle Bit Output Delay	ТОЕТ	-	45	-	70	nS
CE to Toggle Bit Output Delay	ТСЕТ	-	90	-	150	nS

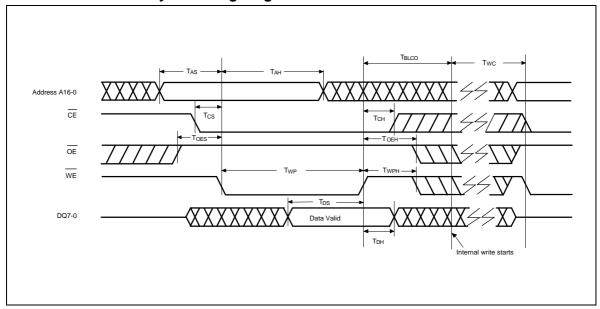
## **TIMING WAVEFORMS**

## **Read Cycle Timing Diagram**

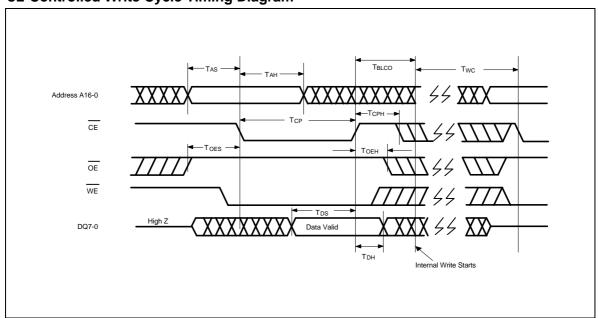




# WE Controlled Write Cycle Timing Diagram

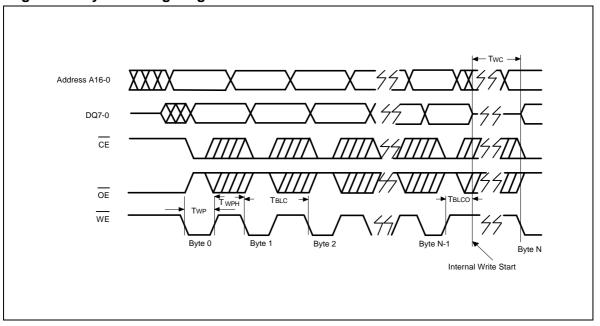


## **CE** Controlled Write Cycle Timing Diagram

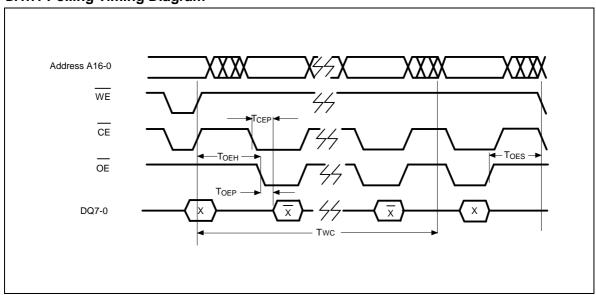




## **Page Write Cycle Timing Diagram**

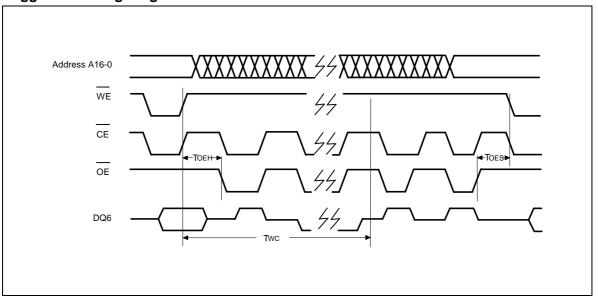


## **DATA** Polling Timing Diagram

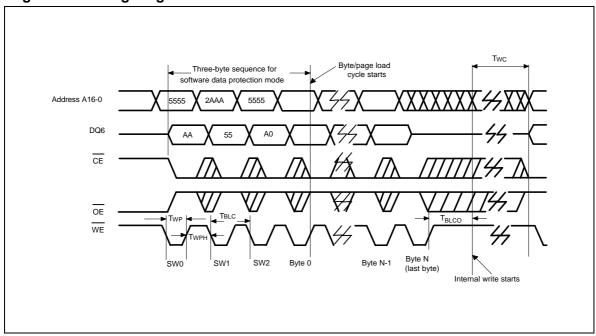




## **Toggle Bit Timing Diagram**

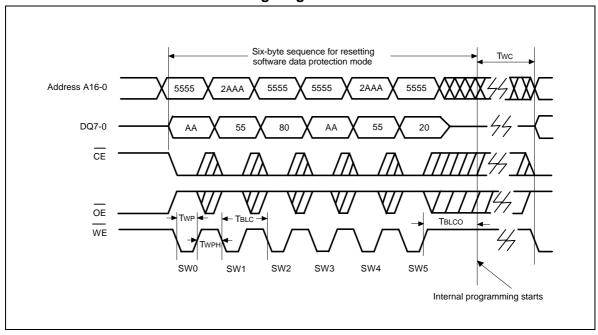


# Page Write Timing Diagram Software Data Protection Mode

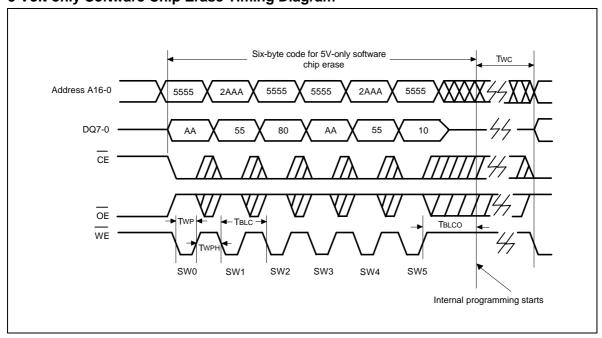




### **Reset Software Data Protection Timing Diagram**



## 5 Volt-only Software Chip Erase Timing Diagram



# **W29EE011**



### **ORDERING INFORMATION**

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (mA)	PACKAGE	CYCLING
W29EE011-90	90	50	100	600 mil DIP	1K
W29EE011-15	150	50	100	600 mil DIP	1K
W29EE011T-90	90	50	100	Type one TSOP	1K
W29EE011T-15	150	50	100	Type one TSOP	1K
W29EE011P-90	90	50	100	32-pin PLCC	1K
W29EE011P-15	150	50	100	32-pin PLCC	1K
W29EE01190B	90	50	100	600 mil DIP	10K
W29EE01115B	150	50	100	600 mil DIP	10K
W29EE011T90B	90	50	100	Type one TSOP	10K
W29EE011T15B	150	50	100	Type one TSOP	10K
W29EE011P90B	90	50	100	32-pin PLCC	10K
W29EE011P15B	150	50	100	32-pin PLCC	10K

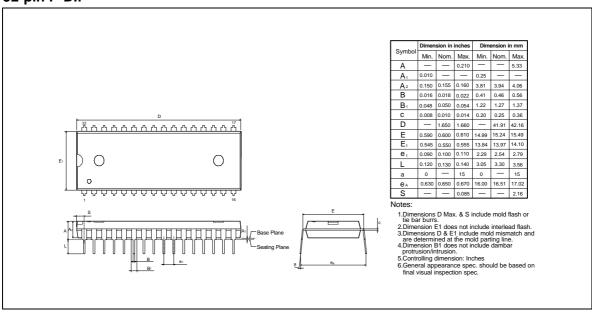
#### Notes:

- 1. Winbond reserves the right to make changes to its products without prior notice.
- 2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

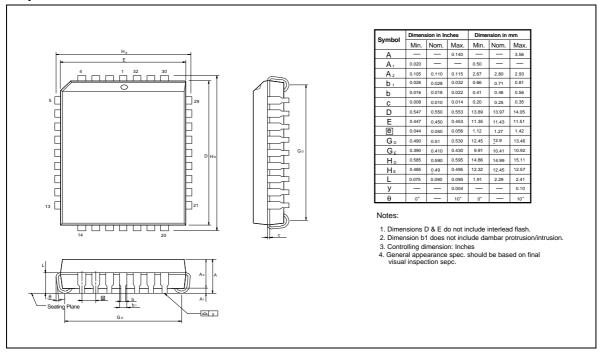


### **PACKAGE DIMENSIONS**

### 32-pin P-DIP



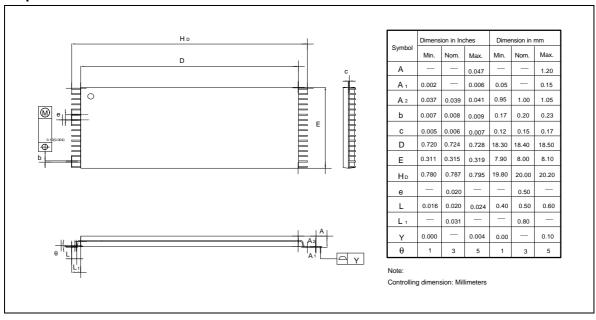
### 32-pin PLCC





Package Dimensions, continued

### 32-pin TSOP





### **VERSION HISTORY**

VERSION	DATE	PAGE	DESCRIPTION
A9	Feb. 1998	6	Add pause 10 mS
		7	Add pause 50 mS
		8	Correct the time 10 mS to 10 μS
		1, 17	Add cycing 100 item
A10	Jun. 1998	1, 10, 11, 12, 17	Add 70 nS bining
A11	Aug. 1998	1, 2, 17, 19	Add TSOP package
A12	Jul. 1999	1, 17	Change endurance cycles as 1K/10K
		1, 11, 12, 17	Delete 70,120 nS bining
		1, 17, 18	Delete SOP package



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Note: All data and specifications are subject to change without notice.