8M-BIT
SERIAL FLASH MEMORY WITH
DUAL AND QUAD SPI

For Automotive & Industrial Plus Grades

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1. GENERAL DESCRIPTION

The W25Q80BV (8M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down.

The W25Q80BV array is organized into 4,096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q80BV has 256 erasable sectors and 16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q80BV supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz (80MHz x 2) for Dual I/O and 320MHz (80MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - W25Q80BV: 8M-bit/1M-byte (1,048,576)
  - 256-byte per programmable page
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- **Highest Performance Serial Flash**
  - 80MHz Dual/Quad SPI clocks
  - 160/320MHz equivalent Dual/Quad SPI
  - 40MB/S continuous data transfer rate
  - Up to 8X that of ordinary Serial Flash
  - More than 100,000 erase/program cycles(1)
  - More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down current
  - -40°C to +85/105/125°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4/32/64K-bytes)
  - Program one to 256 bytes
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB complement array protection
  - Lock-Down and OTP array protection
  - 64-Bit Unique Serial Number for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging(2)**
  - 8-pin SOIC 150/208-mil
  - 8-pad USON 2x3-mm
  - 8-pad WSON 6x5-mm
  - Contact Winbond for KGD and other options

Note:

1. More than 100,000 Block Erase/Program cycles for Industrial temperature; more than 10,000 Erase/Program cycles tested in compliance with AEC-Q100(Please refer to reliability report).
2. Data retention time will reduce significantly after extensive Program/Erase cycling at high temperature.
3. Not all package types are available for ordering, please contact Winbond sales for detail information.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25Q80BV is offered in an 8-pin SOIC 150-mil or 208-mil (package code SN & SS), an 8-pad WSON 6x5-mm (package code ZP), an 8-pad USON 2x3-mm (package code UX) as shown in Figure 1a-b respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pin Configuration SOIC 150 / 208-mil

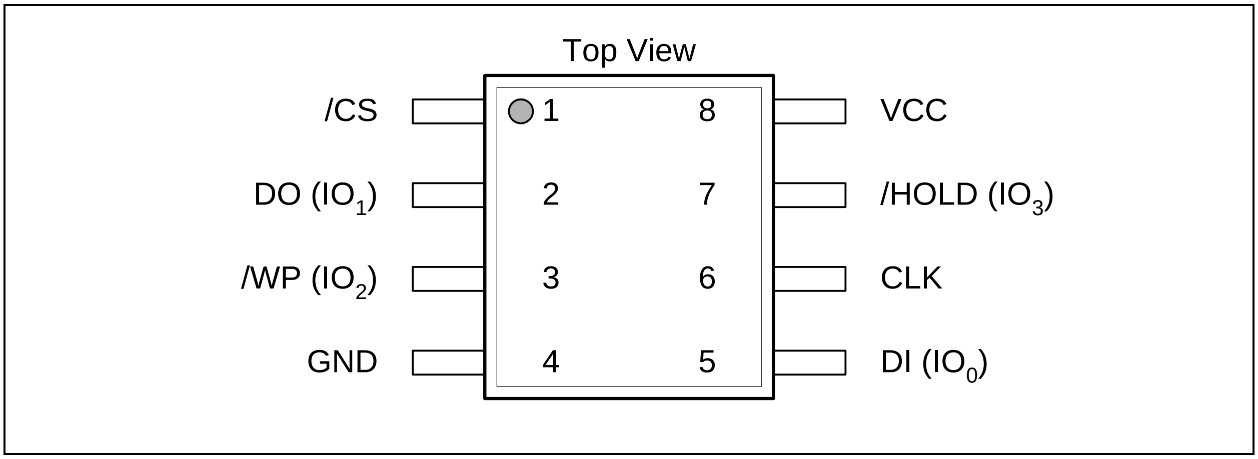


Figure 1a. W25Q80BV Pin Assignments, 8-pin SOIC / VSOP 150 / 208-mil (Package Code SN, SS, SV, ST)

3.2 Pad Configuration WSON 6x5-mm / USON 2x3-mm

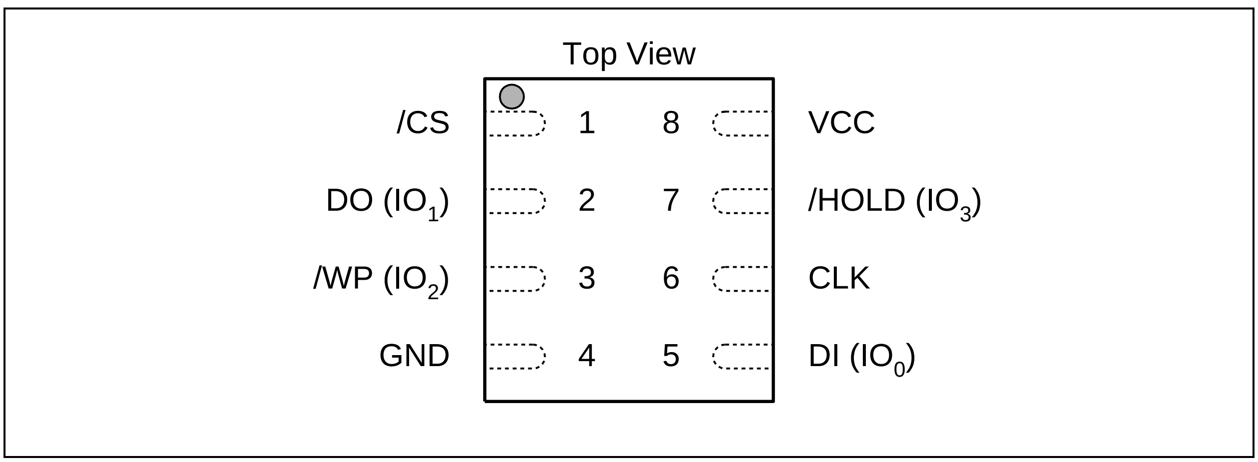


Figure 1b. W25Q80BV Pad Assignments, 8-pad WSON 6x5-mm, USON 2x3-mm (Package Code ZP, UX)

3.3 Pin Description SOIC, WSON, USON.

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 35a). If needed a pull-up resister on /CS can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q80BV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See figure 1a-b for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a-b for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. BLOCK DIAGRAM

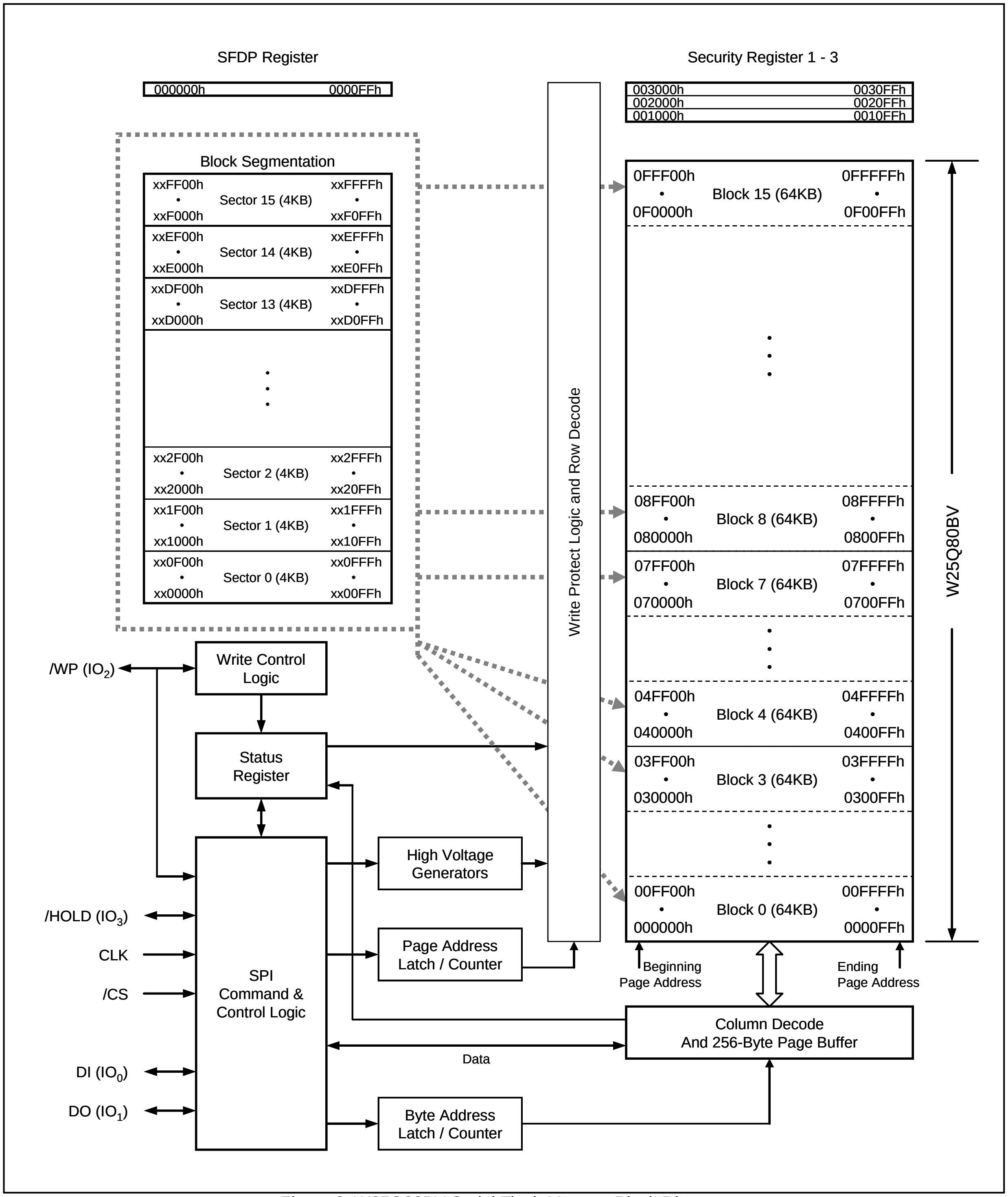


Figure 2. W25Q80BV Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTION

6.1 SPI OPERATIONS

6.1.1 Standard SPI Instructions

The W25Q80BV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25Q80BV supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25Q80BV supports Quad SPI operation when using the “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” instructions. These instructions allow data to be transferred to or from the device six to eight times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q80BV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active low for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q80BV provides several means to protect the data from inadvertent writes.

6.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection*

* Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q80BV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 35a). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

7. CONTROL AND STATUS REGISTERS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status and Erase/Program Suspend status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Register OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1 STATUS REGISTER

7.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

7.1.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top

4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program(2)	Status Register is permanently protected and can not be written to.

Notes:
1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available upon special order. Please contact Winbond for details.

7.1.8 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB3, LB2, LB1)

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers are unlocked. LB[3:1] can be set to 1 individually using the Write Status Register instruction. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.10 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

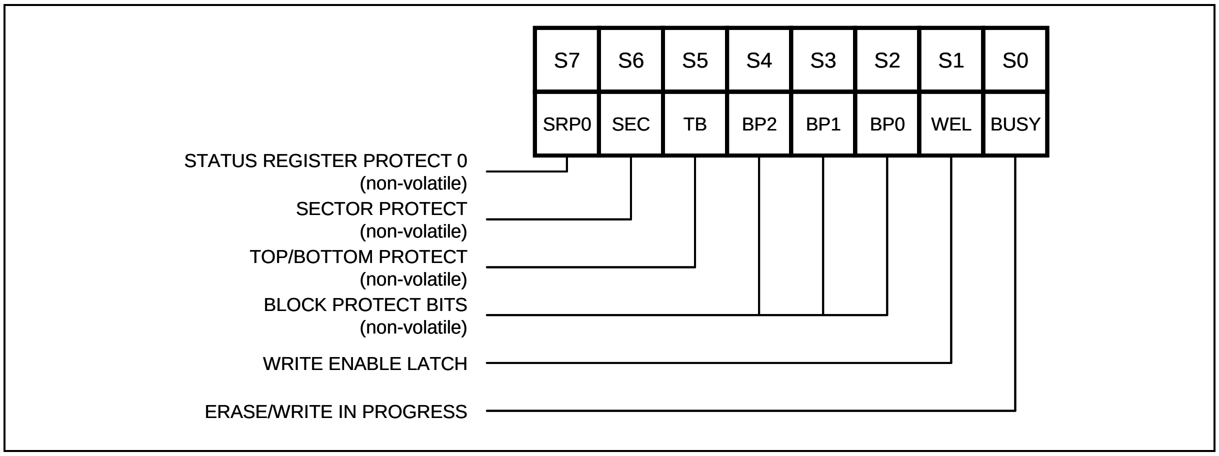


Figure 3a. Status Register-1

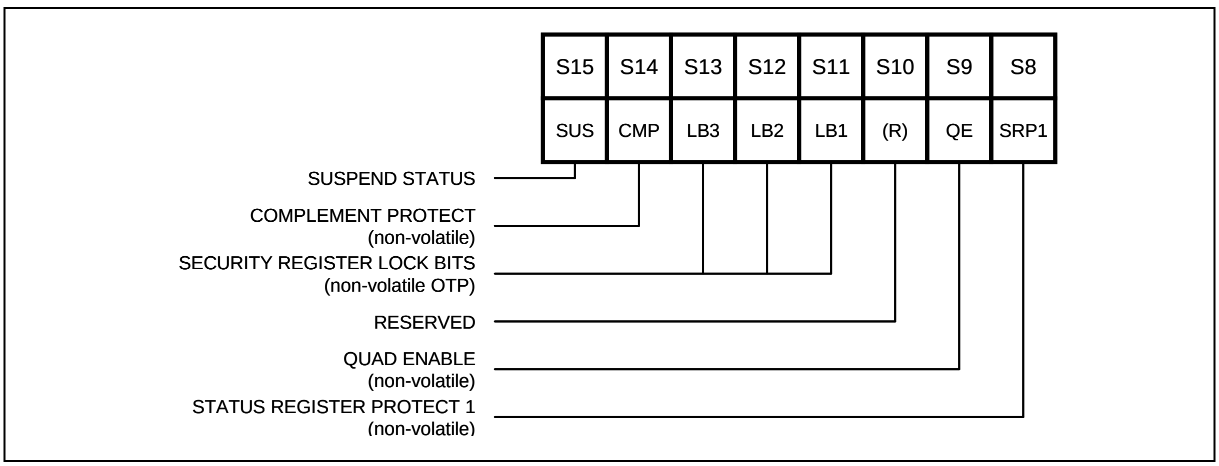


Figure 3b. Status Register-2

7.1.11 Status Register Memory Protection (CMP = 0)

STATUS REGISTER[1]					W25Q80BV (8M-BIT) MEMORY PROTECTION[2]			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000h – 0FFFFFh	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h – 0FFFFFh	128KB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h – 0FFFFFh	256KB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h – 0FFFFFh	512KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/4
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	X	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	ALL
X	X	1	1	X	0 thru 15	000000h – 0FFFFFh	1MB	ALL
1	0	0	0	1	15	0FF000h – 0FFFFFh	4KB	Upper 1/256
1	0	0	1	0	15	0FE000h – 0FFFFFh	8KB	Upper 1/128
1	0	0	1	1	15	0FC000h – 0FFFFFh	16KB	Upper 1/64
1	0	1	0	X	15	0F8000h – 0FFFFFh	32KB	Upper 1/32
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/256
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/128
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/64
1	1	1	0	X	0	000000h – 007FFFh	32KB	Lower 1/32

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.12 Status Register Memory Protection (CMP = 1)

STATUS REGISTER[1]					W25Q80BV (8M-BIT) MEMORY PROTECTION[2]			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 15	000000h – 0FFFFFh	1MB	ALL
0	0	0	0	1	0 thru 14	000000h – 0EFFFFh	960KB	Lower 15/16
0	0	0	1	0	0 thru 13	000000h – 0DFFFFh	896KB	Lower 7/8
0	0	0	1	1	0 thru 11	000000h – 0BFFFFh	768KB	Lower 3/4
0	0	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	1	0	0	1	1 thru 15	010000h – 0FFFFFh	960KB	Upper 15/16
0	1	0	1	0	2 thru 15	020000h – 0FFFFFh	896KB	Upper 7/8
0	1	0	1	1	4 thru 15	040000h – 0FFFFFh	768KB	Upper 3/4
0	1	1	0	0	8 thru 15	080000h – 0FFFFFh	512KB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 15	000000h – 0FEFFFh	1,020KB	Lower 255/256
1	0	0	1	0	0 thru 15	000000h – 0FDFFFh	1,016KB	Lower 127/128
1	0	0	1	1	0 thru 15	000000h – 0FBFFFh	1,008KB	Lower 63/64
1	0	1	0	X	0 thru 15	000000h – 0F7FFFh	992KB	Lower 31/32
1	1	0	0	1	0 thru 15	001000h – 0FFFFFh	1,020KB	Upper 255/256
1	1	0	1	0	0 thru 15	002000h – 0FFFFFh	1,016KB	Upper 127/128
1	1	0	1	1	0 thru 15	004000h – 0FFFFFh	1,008KB	Upper 63/64
1	1	1	0	X	0 thru 15	008000h – 0FFFFFh	992KB	Upper 31/32

Notes:

1. X = don’t care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.2 INSTRUCTIONS

The instruction set of the W25Q80BV consists of thirty two basic instructions that are fully controlled through the SPI bus (see Instruction Set table1-3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 34. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

7.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7-MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q80BV	13h	4014h

7.2.2 Instruction Set Table 1 (Erase, Program Instructions)[1]

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	**06h**					
Write Enable for Volatile Status Register	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7–S0) [2]				
Read Status Register-2	**35h**	(S15–S8) [2]				
Write Status Register	**01h**	S7–S0	S15-S8			
Page Program	**02h**	A23–A16	A15–A8	A7–A0	D7–D0	
Quad Page Program	**32h**	A23–A16	A15–A8	A7–A0	D7–D0, …[3]	
Sector Erase (4KB)	**20h**	A23–A16	A15–A8	A7–A0		
Block Erase (32KB)	**52h**	A23–A16	A15–A8	A7–A0		
Block Erase (64KB)	**D8h**	A23–A16	A15–A8	A7–A0		
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. Quad Page Program Input Data:

IO0 = D4, D0, ……
IO1 = D5, D1, ……
IO2 = D6, D2, ……
IO3 = D7, D3, ……

7.2.3 Instruction Set Table 2 (Read Instructions)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)[1]
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)[3]
Fast Read Dual I/O	**BBh**	A23-A8[2]	A7-A0, M7-M0[2]	(D7-D0, …)[1]		
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0[4]	(x,x,x,x, D7-D0, …)[5]	(D7-D0, …)[3]		
Set Burst with Wrap	**77h**	xxxxxx, W6-W4[4]				

Notes:

1. Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

2. Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data
IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

4. Quad Input Address
IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap Input
IO0 = x, x, x, x, x, x, W4, x
IO1 = x, x, x, x, x, x, W5, x
IO2 = x, x, x, x, x, x, W6, x
IO3 = x, x, x, x, x, x, x, x

5. Fast Read Quad I/O Data
IO0 = (x, x, x, x, D4, D0, …..)
IO1 = (x, x, x, x, D5, D1, …..)
IO2 = (x, x, x, x, D6, D2, …..)
IO3 = (x, x, x, x, D7, D3, …..)

7. M[7:0] should be set to FFh.

7.2.4 Instruction Set Table 3 (ID, Security Instructions)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Release Power down/ Device ID	**ABh**	dummy	dummy	dummy	(ID7-ID0)[1]	
Manufacturer/ Device ID[2]	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
Manufacturer/Device ID by Dual I/O	**92h**	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])		
Manufacture/Device ID by Quad I/O	**94h**	A23-A0, M[7:0]	xxxx, (MF[7:0], ID[7:0])	(MF[7:0], ID[7:0], …)		
JEDEC ID	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read Unique ID	**4Bh**	dummy	dummy	dummy	dummy	(ID63-ID0)
Read SFDP Register	**5Ah**	00h	00h	A7–A0	dummy	(D7-0)
Erase Security Registers[3]	**44h**	A23–A16	A15–A8	A7–A0		
Program Security Registers[3]	**42h**	A23–A16	A15–A8	A7–A0	D7-D0	D7-D0
Read Security Registers[3]	**48h**	A23–A16	A15–A8	A7–A0	dummy	(D7-0)

Notes:

1. The Device ID will repeat continuously until /CS terminates the instruction.
2. See Manufacturer and Device Identification table for Device ID information.
3. Security Register Address:

   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

7.2.5 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

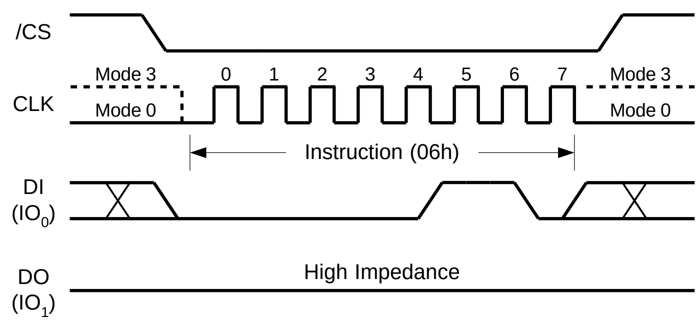


Figure 4. Write Enable Instruction Sequence Diagram

7.2.6 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

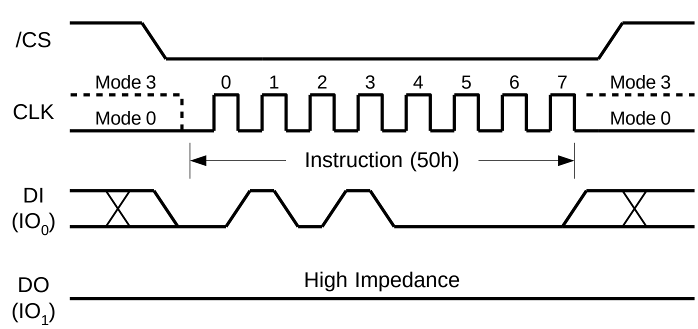


Figure 5. Write Enable for Volatile Status Register Instruction Sequence Diagram

7.2.7 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase and Chip Erase instructions.

Write Disable instruction can also be used to invalidate the Write Enable for Volatile Status Register instruction.

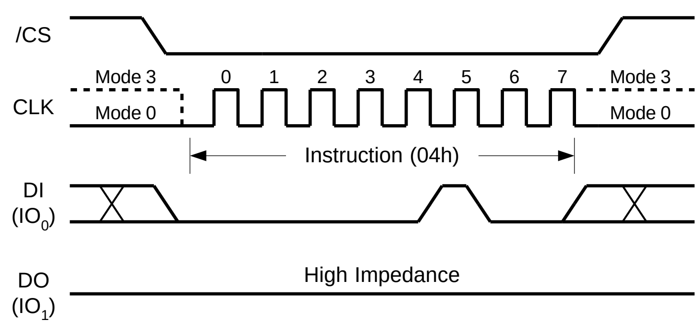


Figure 6. Write Disable Instruction Sequence Diagram

7.2.8 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code "05h" for Status Register-1 or "35h" for Status Register-2 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 7. The Status Register bits are shown in figure 3a and 3b and include the BUSY, WEL, BP2-BP0, TB, SEC, SRP0, SRP1, QE, LB[3:1], CMP and SUS bits (see Status Register section earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

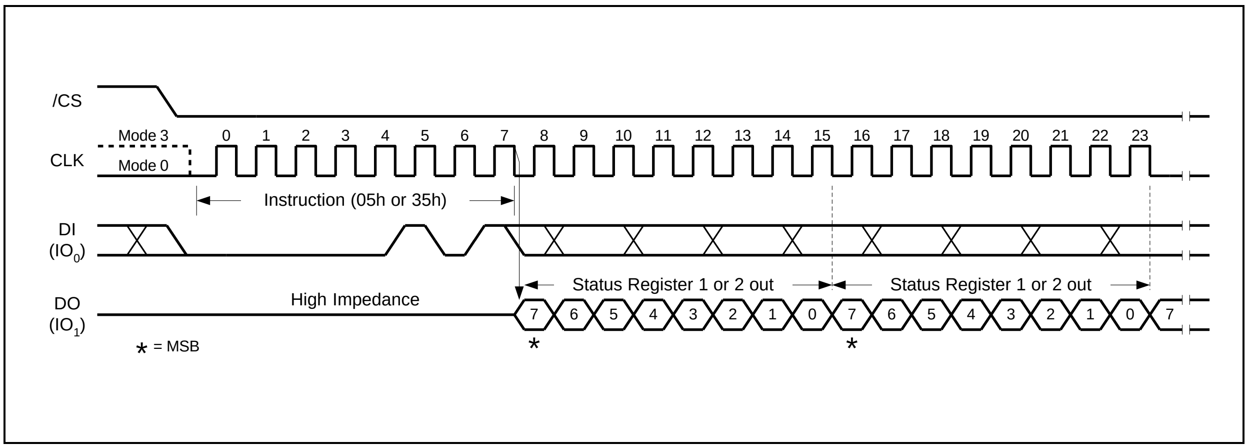


Figure 7. Read Status Register Instruction Sequence Diagram

7.2.9 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 thru 2 of Status Register-1) and CMP, LB3, LB2, LB1, QE, SRP1 (bits 14 thru 8 of Status Register-2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it can not be cleared to 0. The Status Register bits are shown in figure 3a and 3b and described in 7.1.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h", and then writing the status register data byte as illustrated in figure 8.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB3, LB2, LB1 can not be changed from "1" to "0" because of the OTP protection for these bits. Upon power off, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored when power on again.

To complete the Write Status Register instruction, the /CS pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If /CS is driven high after the eighth clock (compatible with the 25X series) the CMP and QE bits will be cleared to 0.

During non-volatile Status Register write operation (06h combined with 01h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

Please refer to 7.1 for detailed Status Register Bit descriptions. Factory default for all status Register bits are 0.

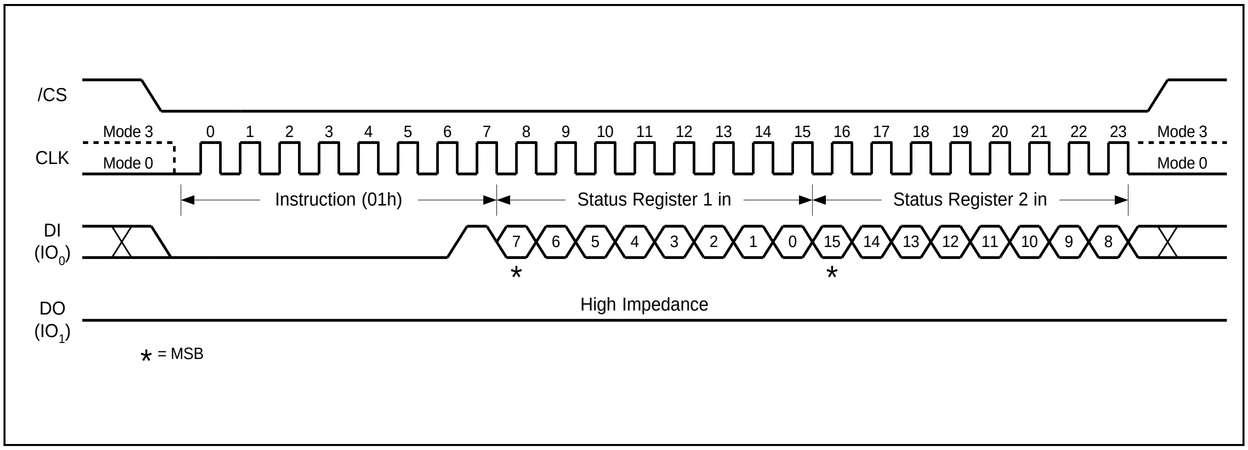


Figure 8. Write Status Register Instruction Sequence Diagram

7.2.10 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

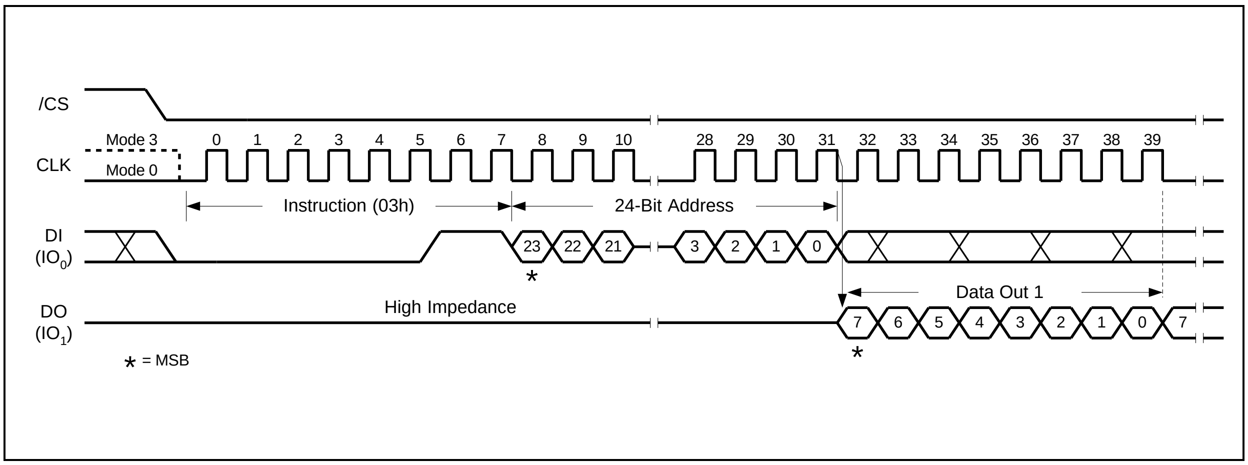


Figure 9. Read Data Instruction Sequence Diagram

7.2.11 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

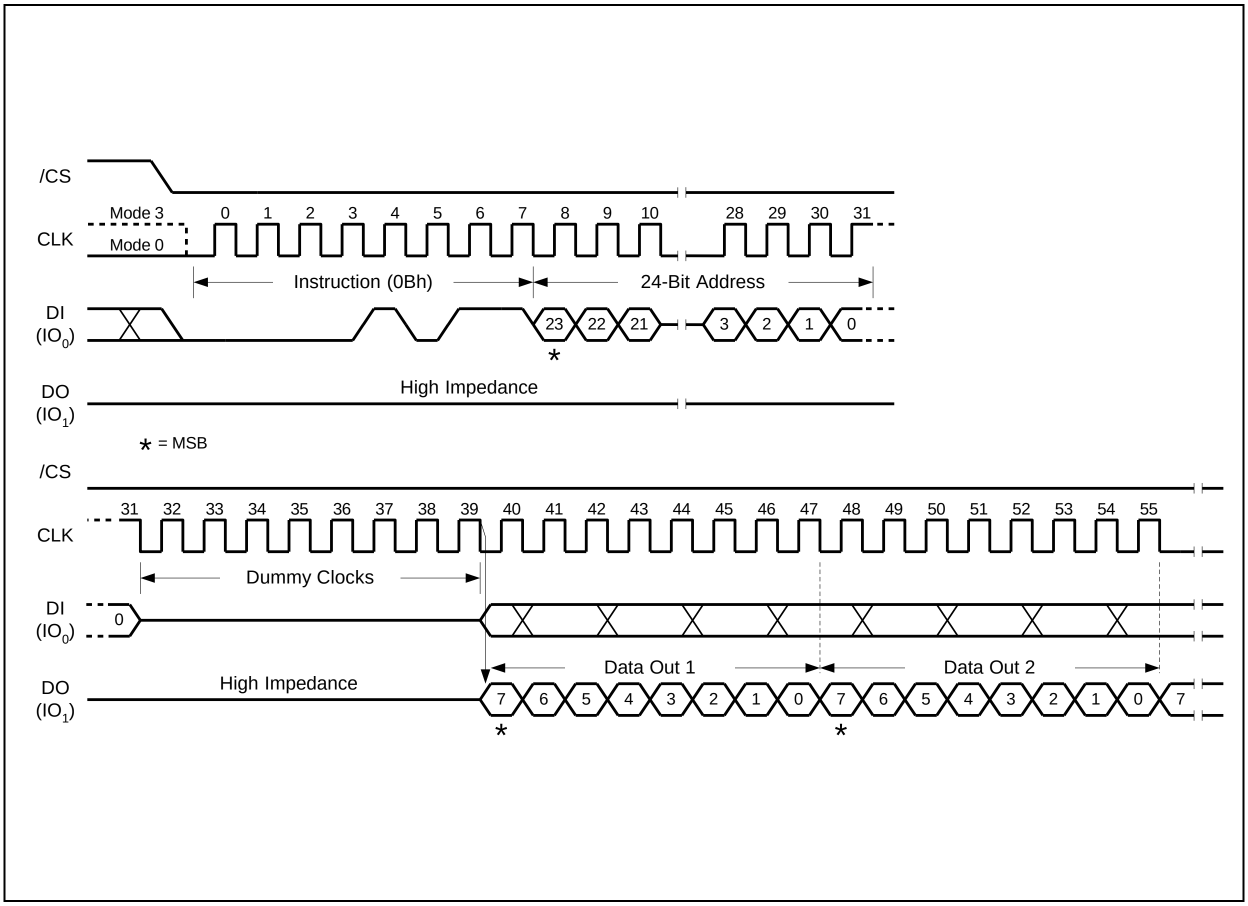


Figure 10. Fast Read Instruction Sequence Diagram

7.2.12 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred from the W25Q80BV at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

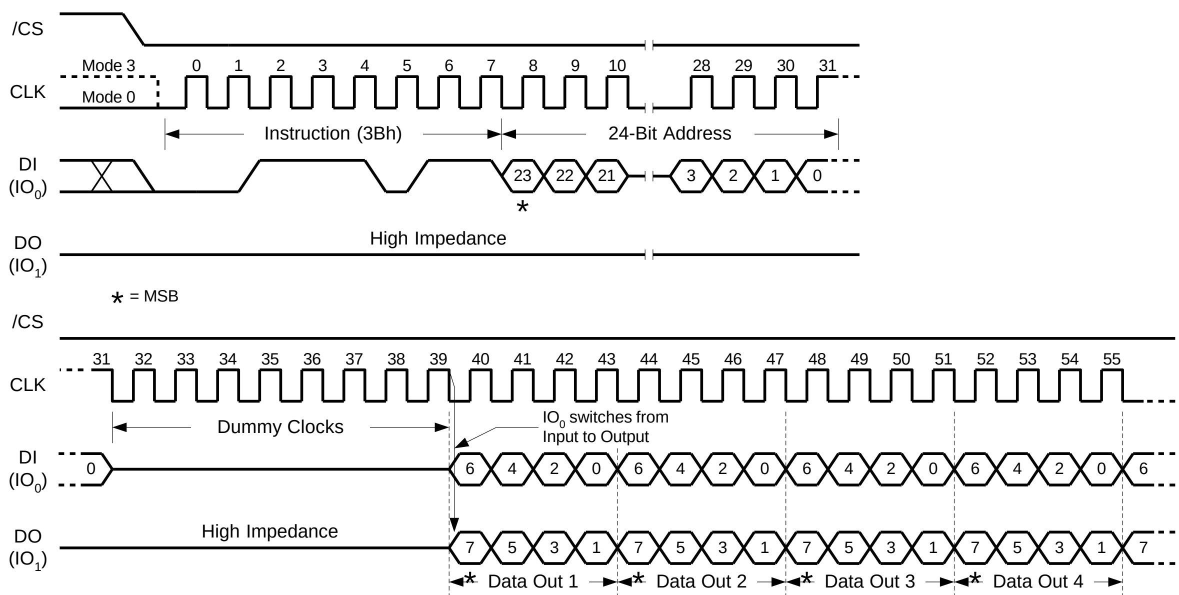


Figure 11. Fast Read Dual Output Instruction Sequence Diagram

7.2.13 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1). The Fast Read Quad Output Instruction allows data to be transferred from the W25Q80BV at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

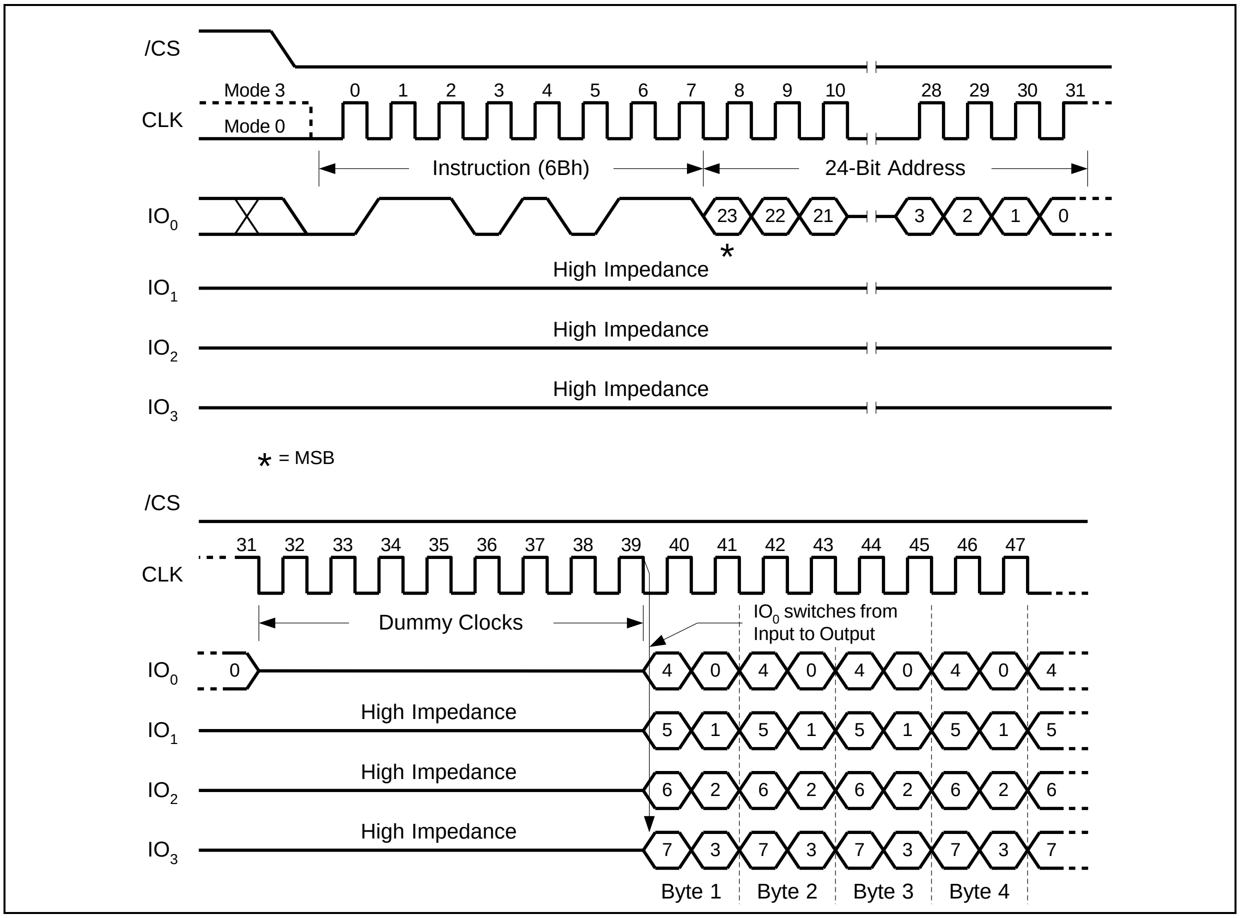


Figure 12. Fast Read Quad Output Instruction Sequence Diagram

7.2.14 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications. After the input Address bits (A23-A0), as shown in Figure 13, M7-M0 should be set to FFh.

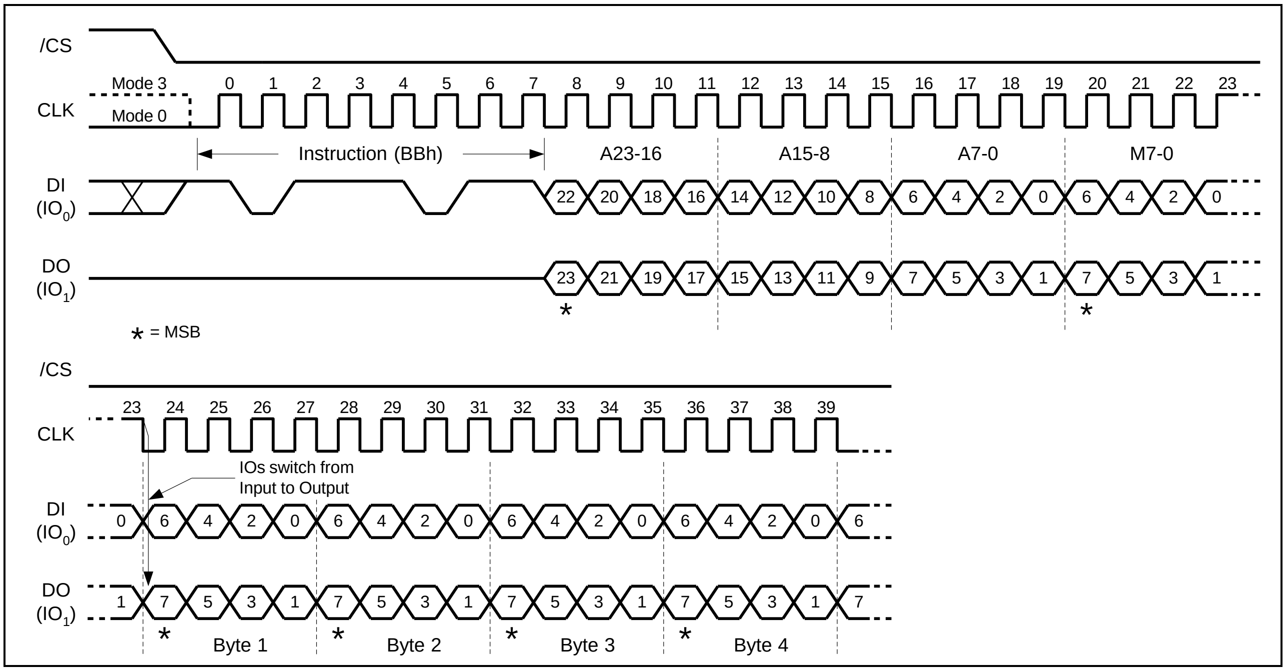


Figure 13. Fast Read Dual I/O Instruction Sequence Diagram

Note: M[7:0] should be set to FFh.

7.2.15 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction. After the input Address bits (A23-A0), as shown in Figure 14, M7-M0 should be set to FFh.

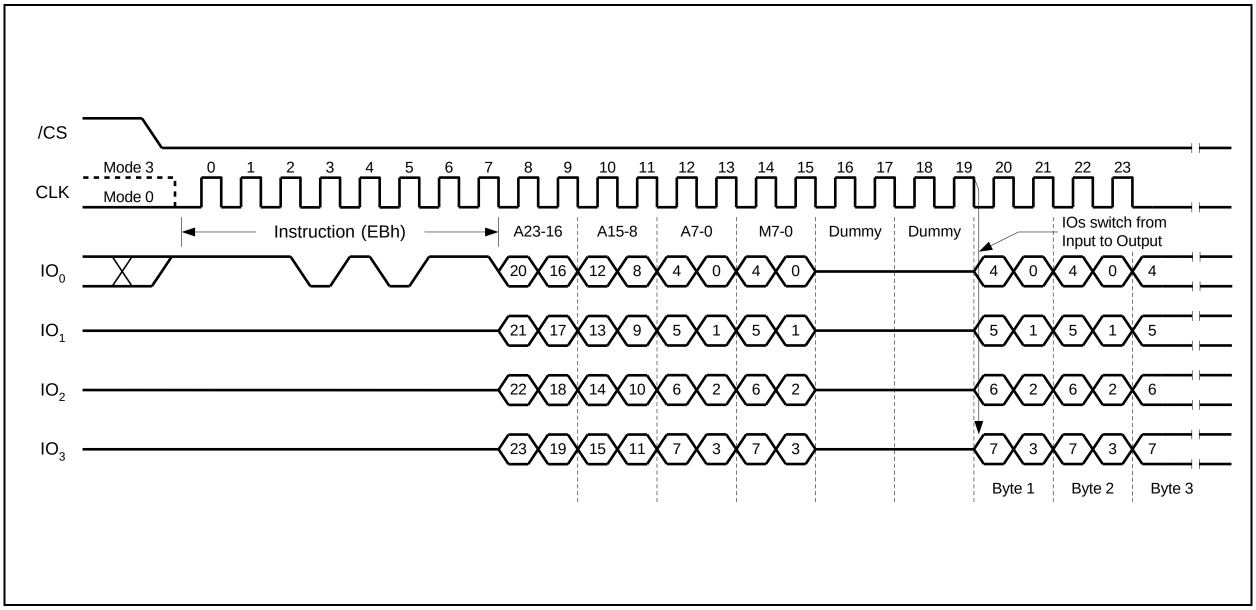


Figure 14. Fast Read Quad I/O Instruction Sequence Diagram

Note: M[7:0] should be set to FFh.

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around"

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" command prior to EBh. The "Set Burst with Wrap" command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See 7.2.16 for detail descriptions.

7.2.16 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" instruction to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in figure 15. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	**Wrap Length**	**Wrap Around**	**Wrap Length**
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" instruction will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since W25Q80BV does not have a hardware Reset Pin.

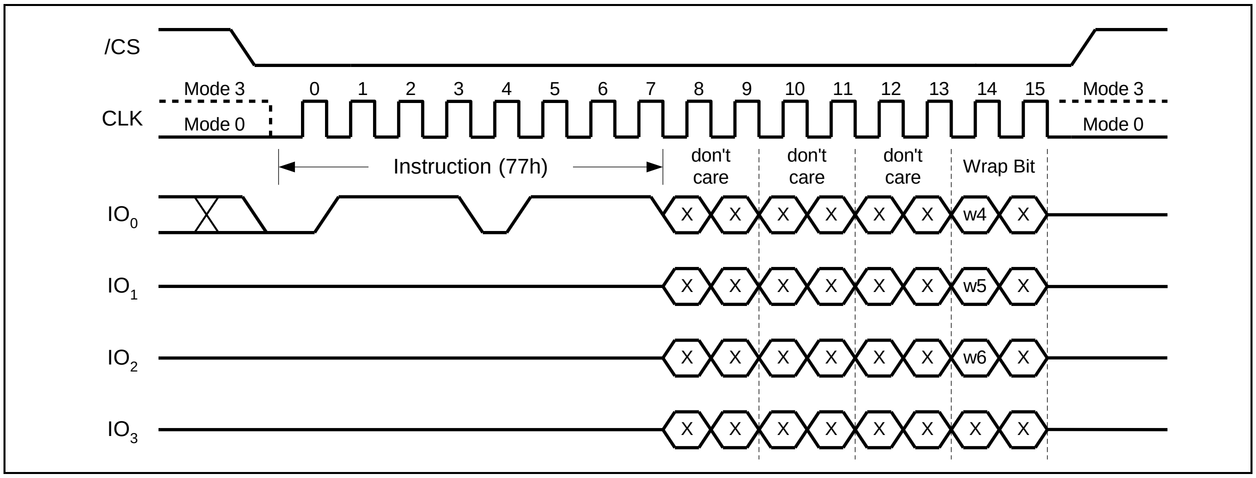


Figure 15. Set Burst with Wrap Instruction Sequence

7.2.17 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 16.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

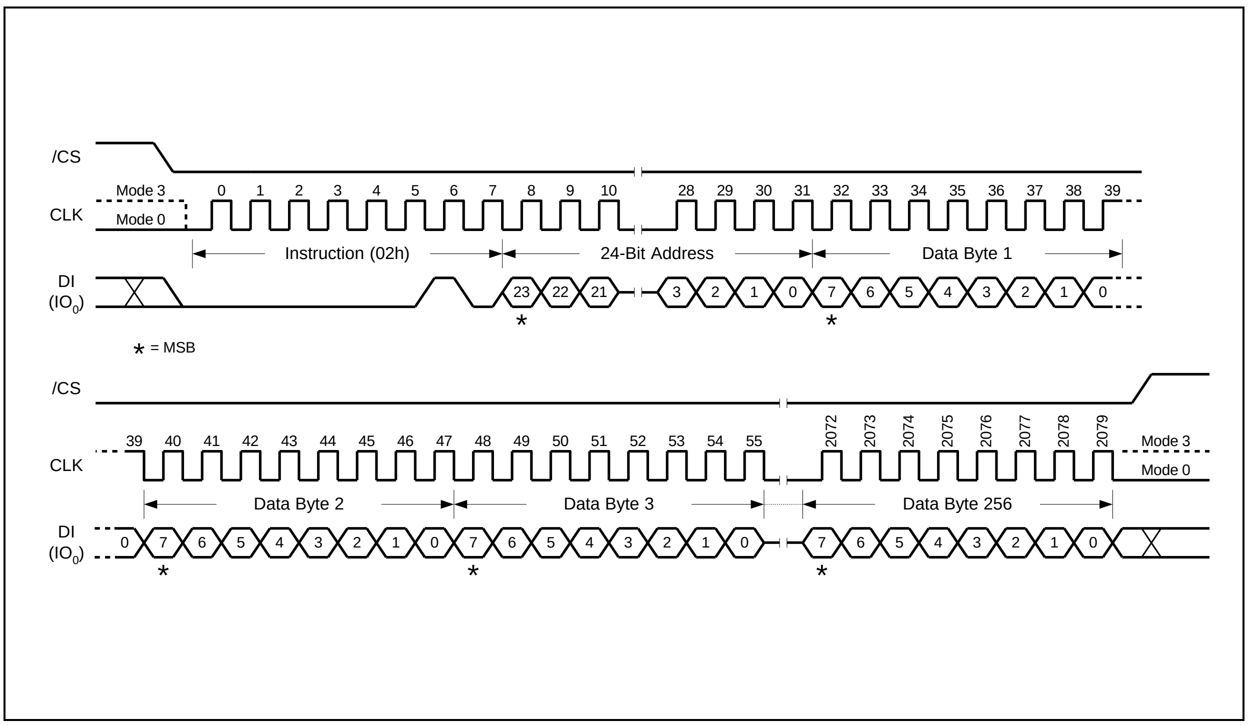


Figure 16. Page Program Instruction Sequence Diagram

7.2.18 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in figure 17.

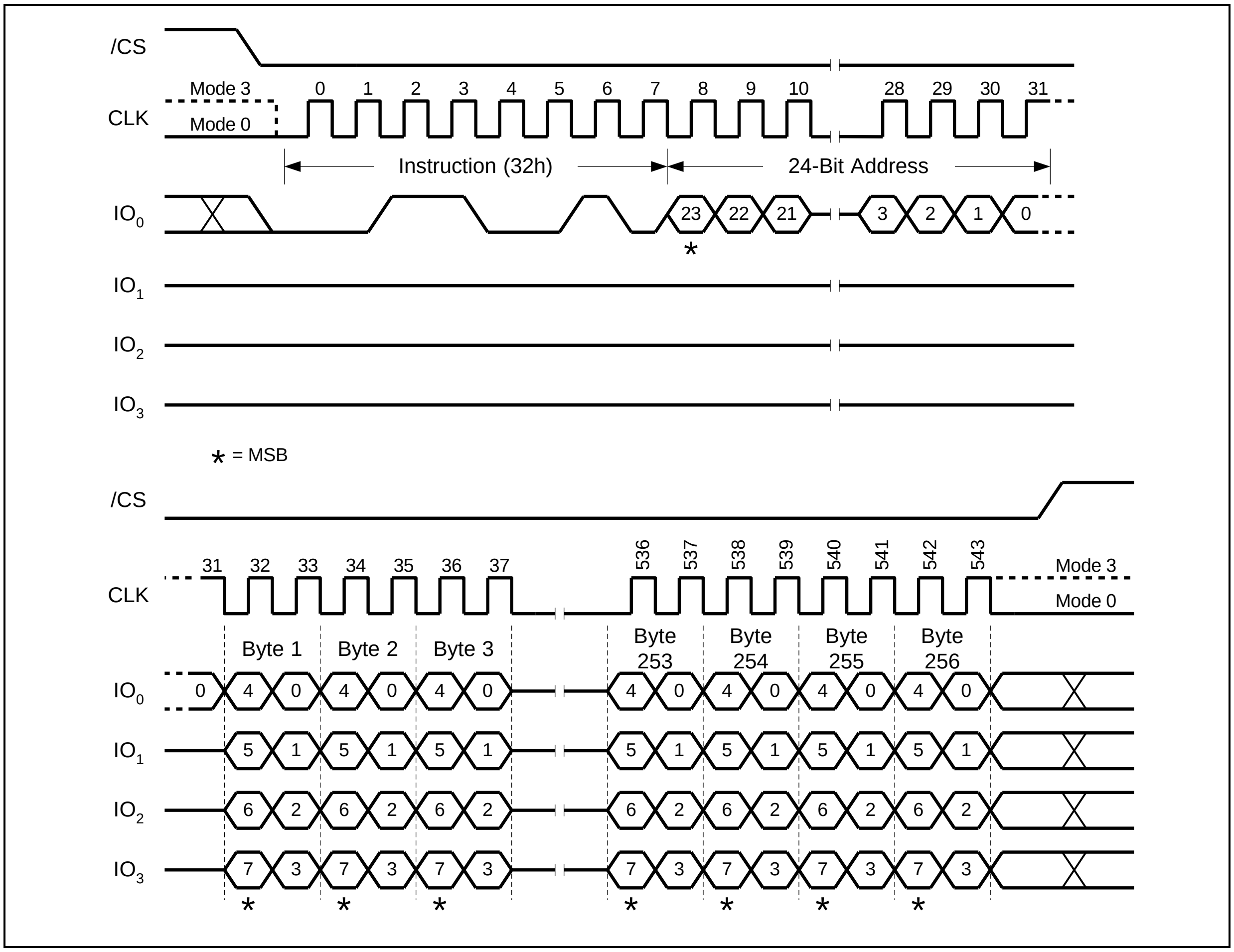


Figure 17. Quad Input Page Program Instruction Sequence Diagram

7.2.19 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 18.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

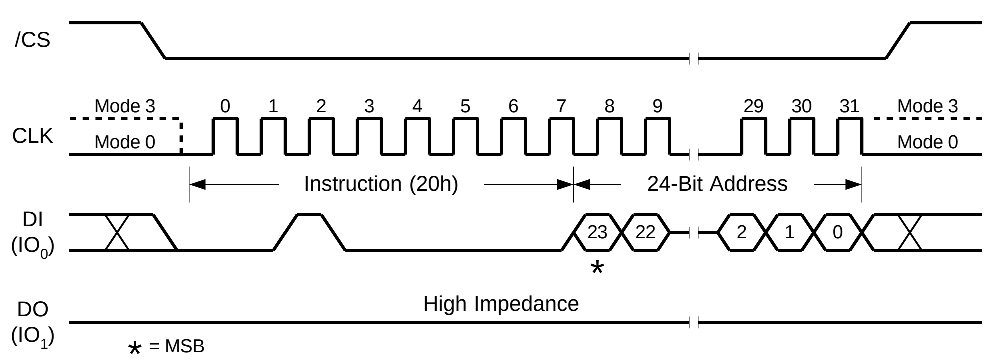


Figure 18. Sector Erase Instruction Sequence Diagram

7.2.20 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 19.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

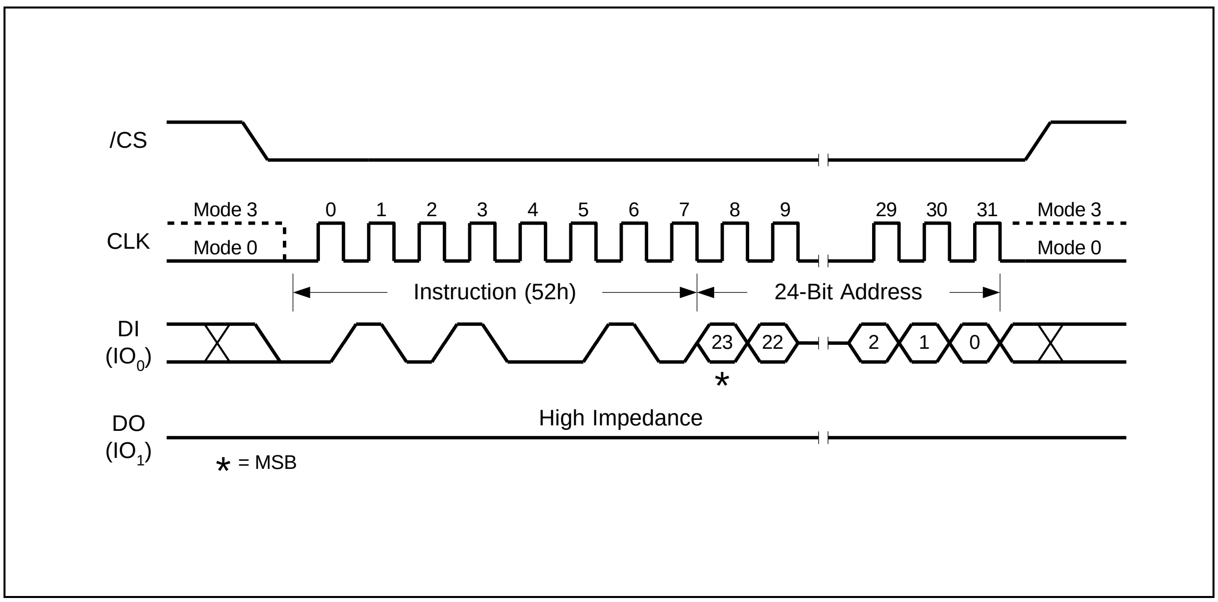


Figure 19. 32KB Block Erase Instruction Sequence Diagram

7.2.21 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 20.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

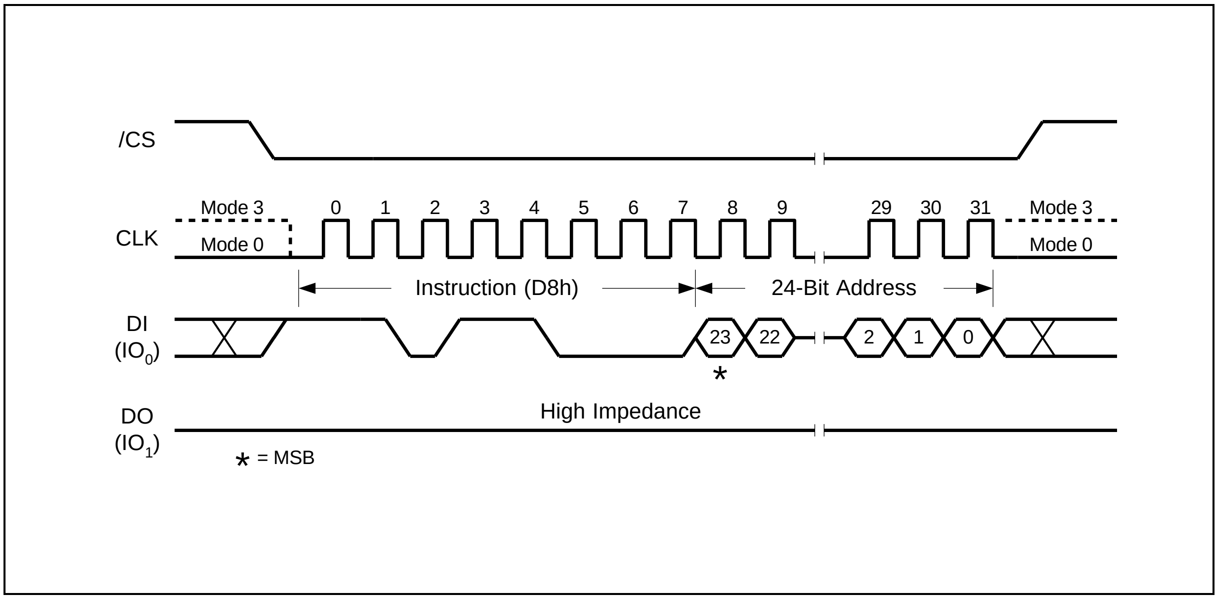


Figure 20. 64KB Block Erase Instruction Sequence Diagram

7.2.22 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 21.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

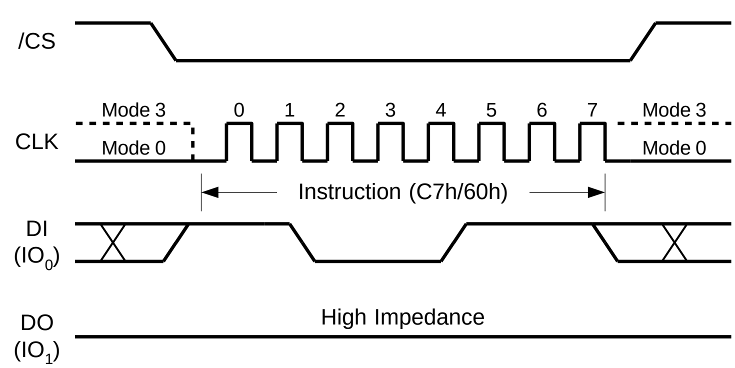


Figure 21. Chip Erase Instruction Sequence Diagram

7.2.23 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in figure 22.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “t_{SUS}” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{RSM}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. When the device is powered up again, it is recommended for the user to repeat the same Erase or Program operation that was interrupted, at the same address location, to avoid the potention data corruption.

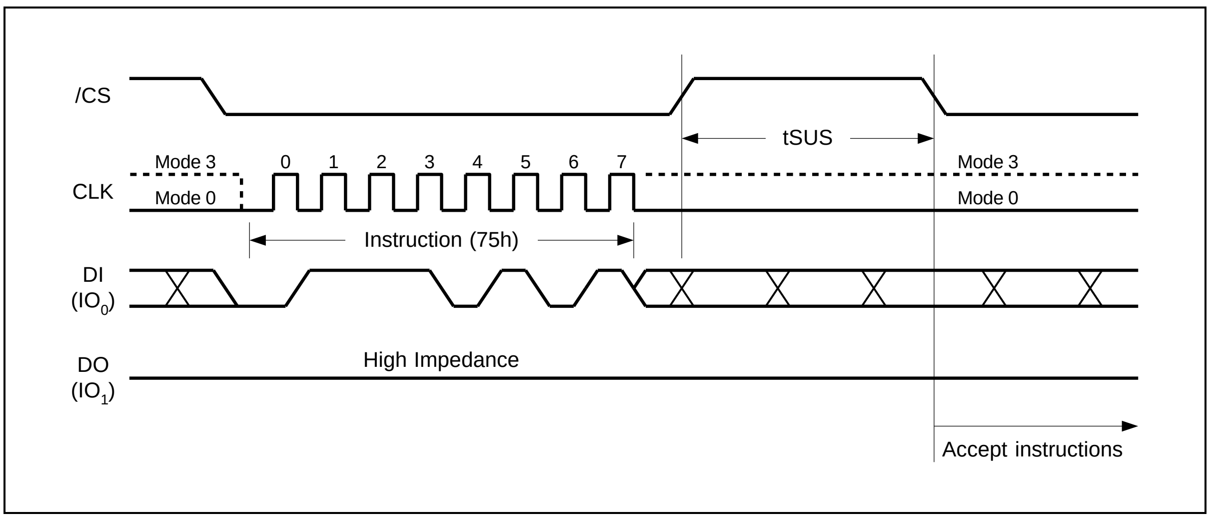


Figure 22. Erase/Program Suspend Instruction Sequence

7.2.24 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in figure 23.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

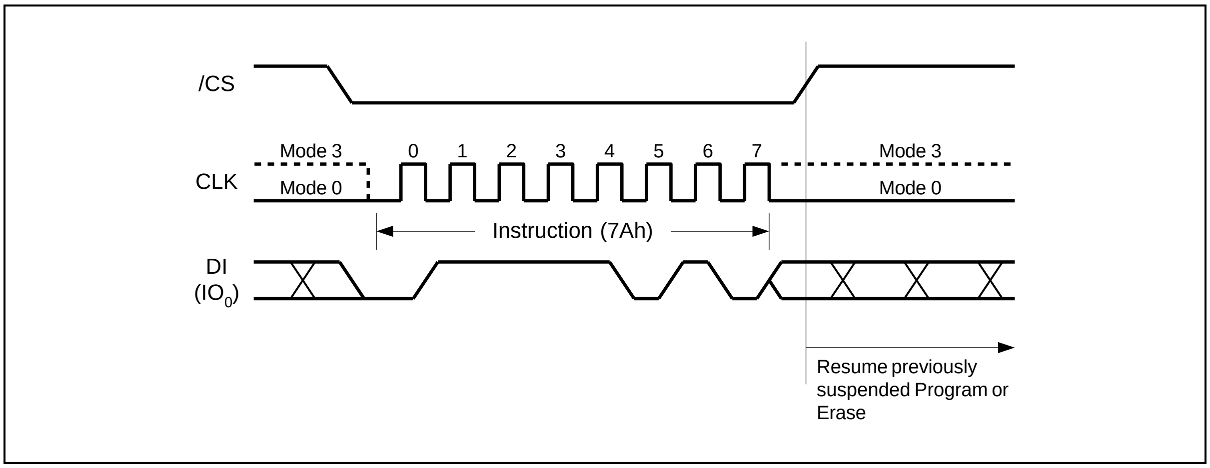


Figure 23. Erase/Program Resume Instruction Sequence

7.2.25 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in figure 24.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

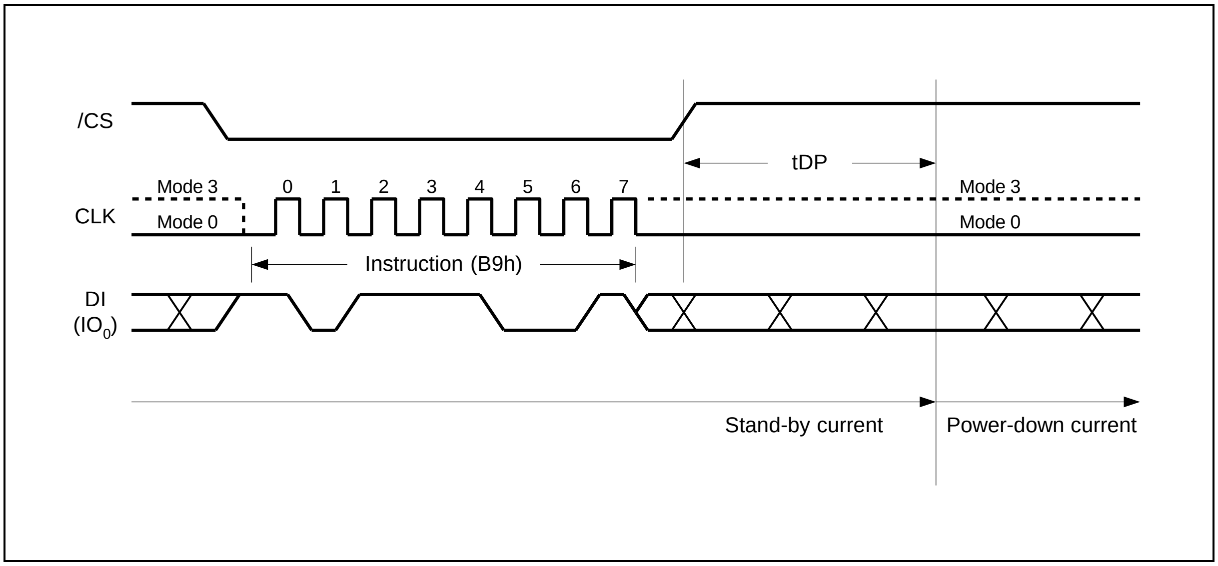


Figure 24. Deep Power-down Instruction Sequence Diagram

7.2.26 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 25a. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 25a. The Device ID values for the W25Q80BV is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 25b, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

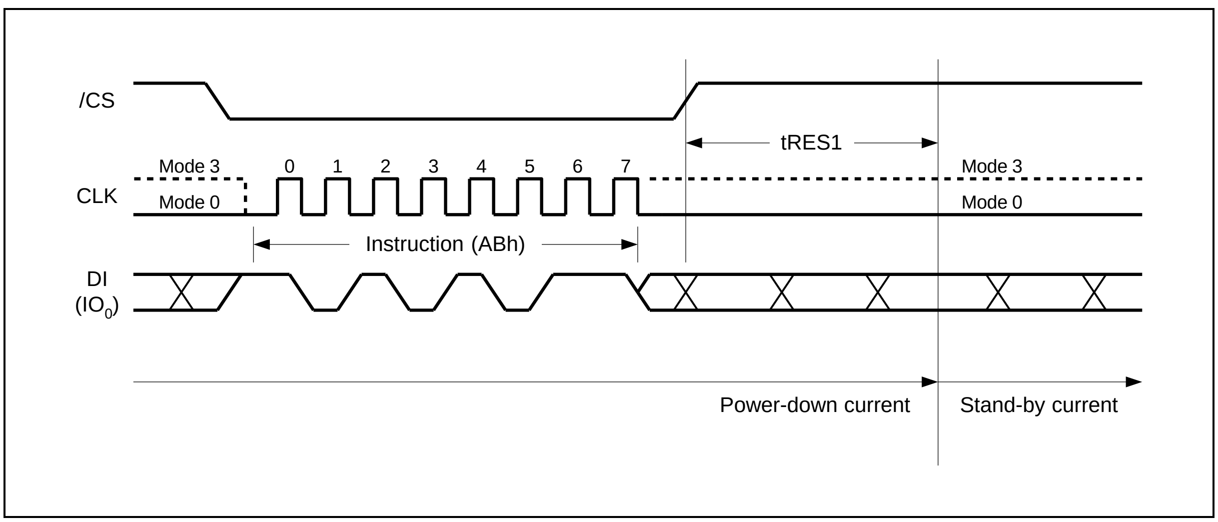


Figure 25a. Release Power-down Instruction Sequence

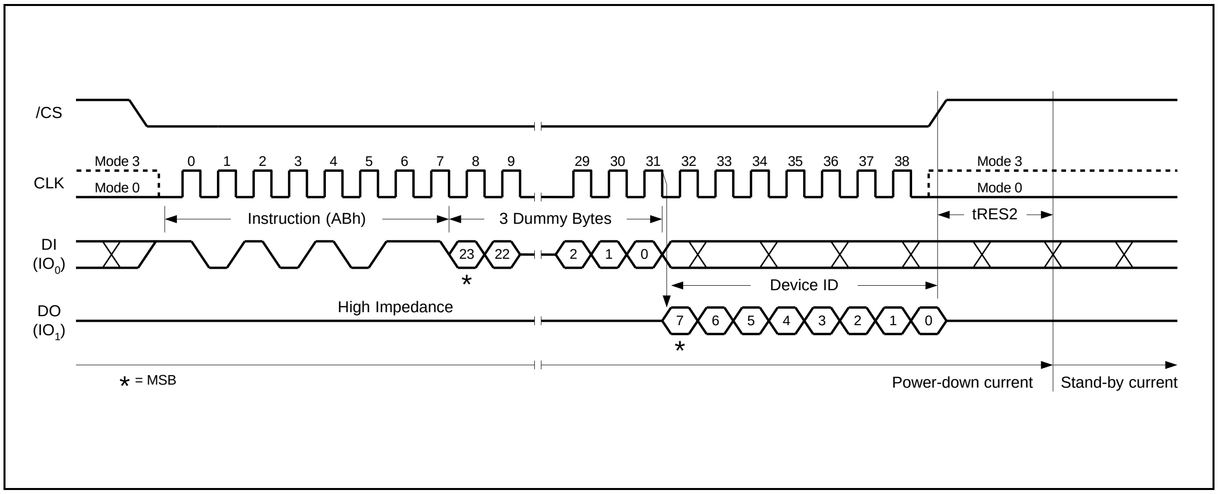


Figure 25b. Release Power-down / Device ID Instruction Sequence Diagram

7.2.27 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 26. The Device ID values for the W25Q80BV is listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

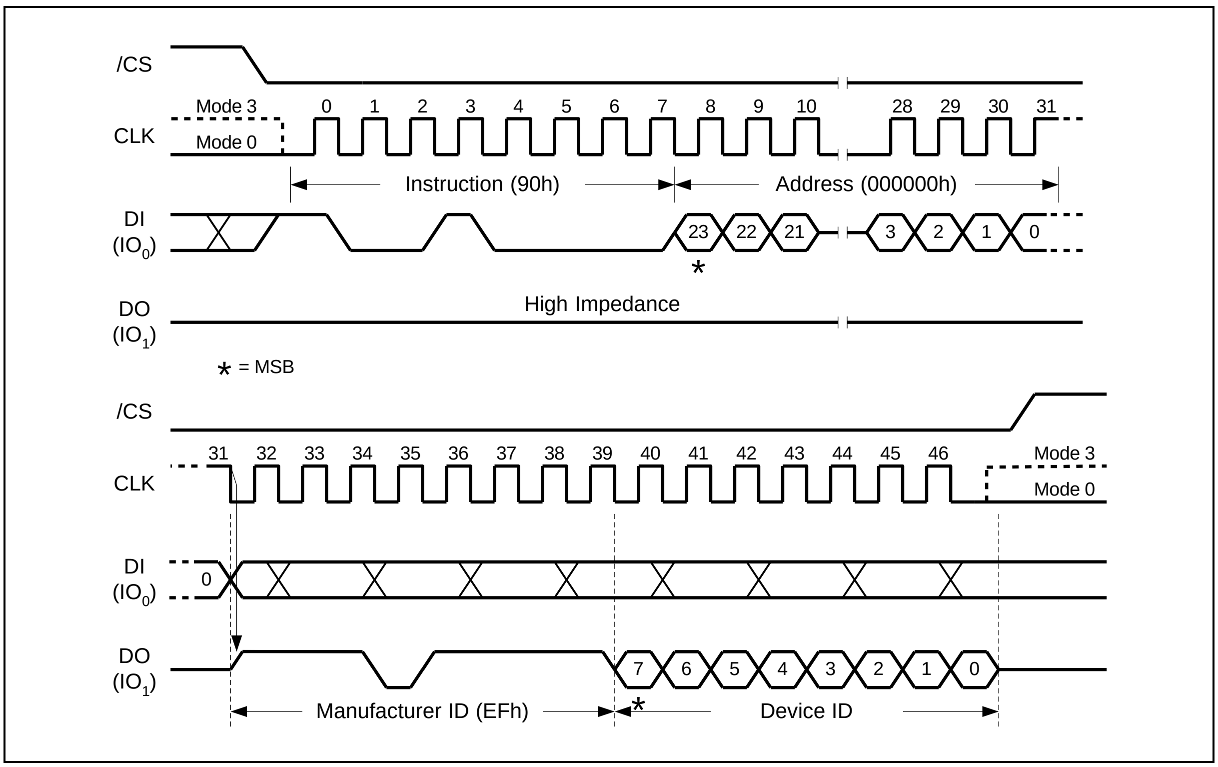


Figure 26. Read Manufacturer / Device ID Diagram

7.2.28 Read Manufacturer / Device ID Dual I/O (92h)

The Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in figure 27. The Device ID values for the W25Q80BV is listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

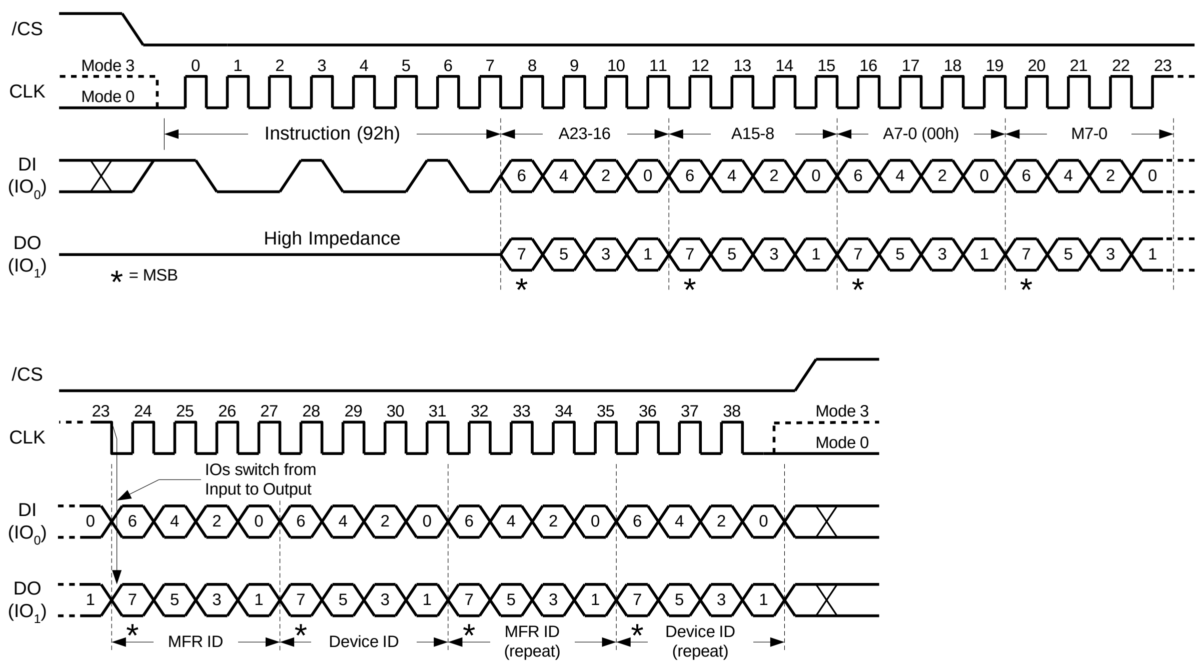


Figure 27. Read Manufacturer / Device ID Dual I/O Diagram

Note:

M[7:0] bits must be set to FFh to be compatible with Fast Read Dual I/O instruction.

7.2.29 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a 24-bit address (A23-A0) of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in figure 28. The Device ID values for the W25Q80BV is listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

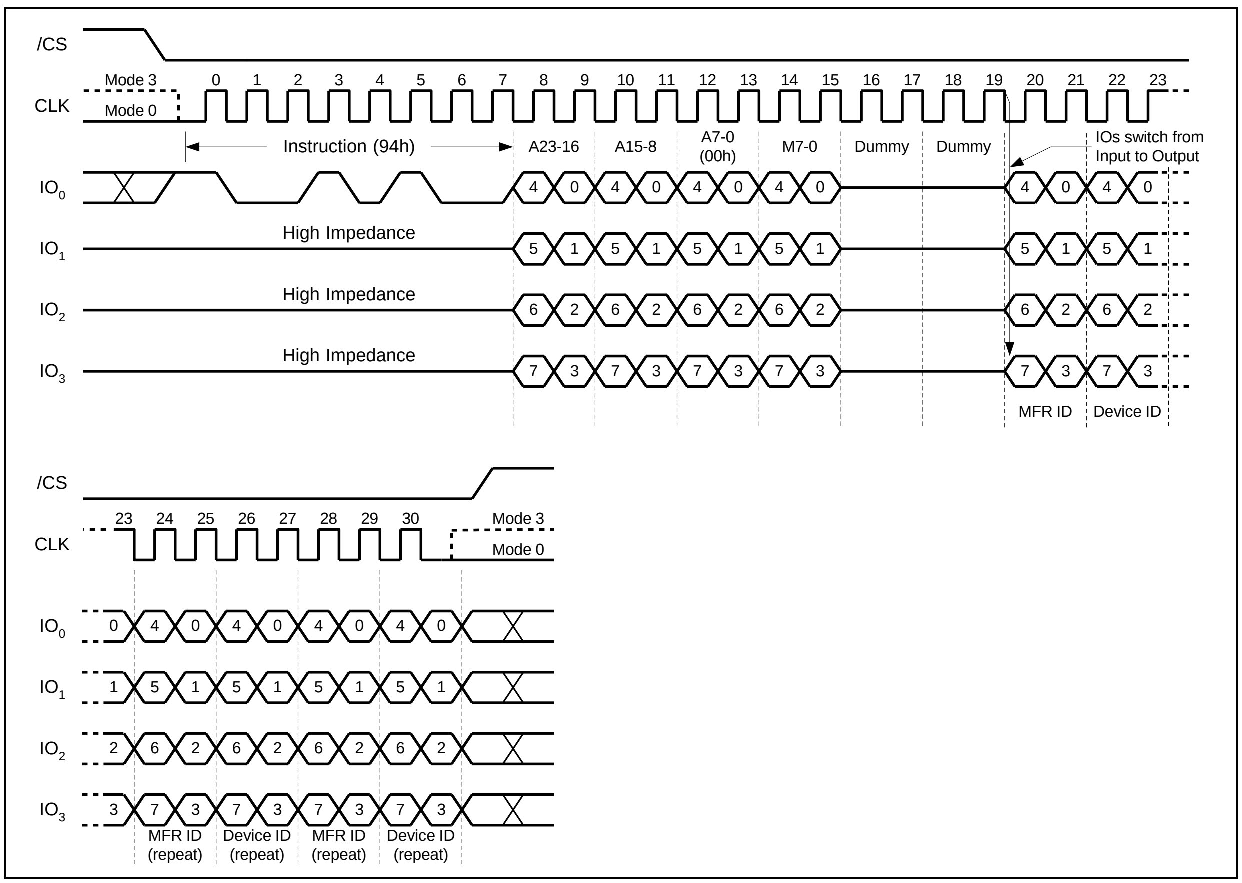


Figure 28. Read Manufacturer / Device ID Quad I/O Diagram

Note:

M[7:0] bits must be set to FFh to be compatible with Fast Read Dual I/O instruction.

7.2.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q80BV device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in figure 29.

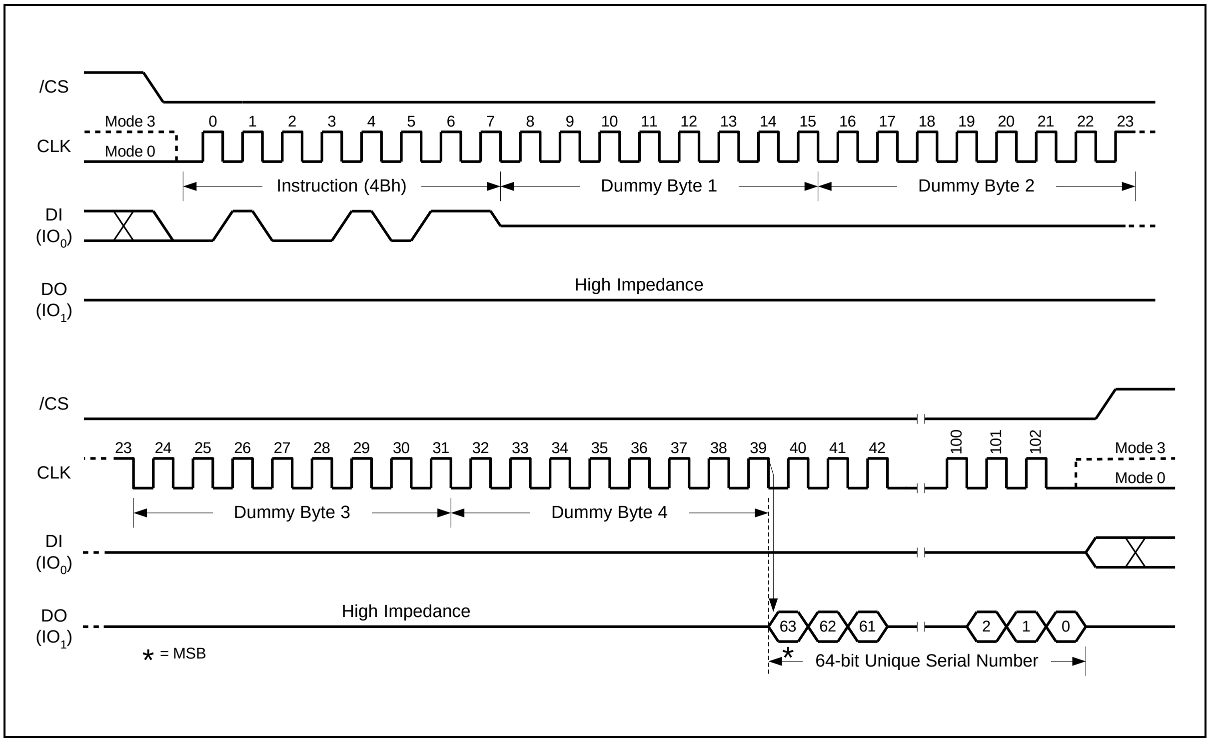


Figure 29. Read Unique ID Number Instruction Sequence

7.2.31 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q80BV provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 30. For memory type and capacity values refer to Manufacturer and Device Identification table.

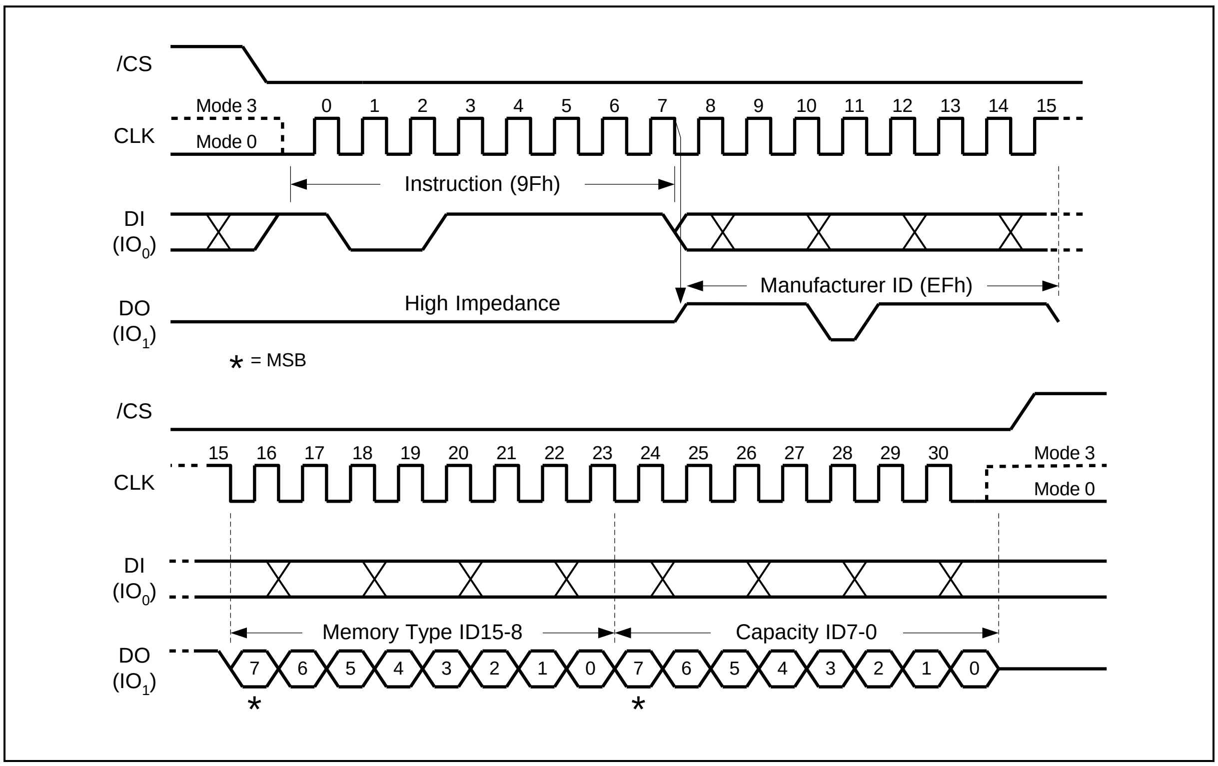


Figure 30. Read JEDEC ID Instruction Sequence

7.2.32 Read SFDP Register (5Ah)

The W25Q80BV features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about devices operational capability such as available commands, timing and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications. Most Winbond SpiFlash Memories shipped after June 2010 (date code 1023 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in figure 31. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

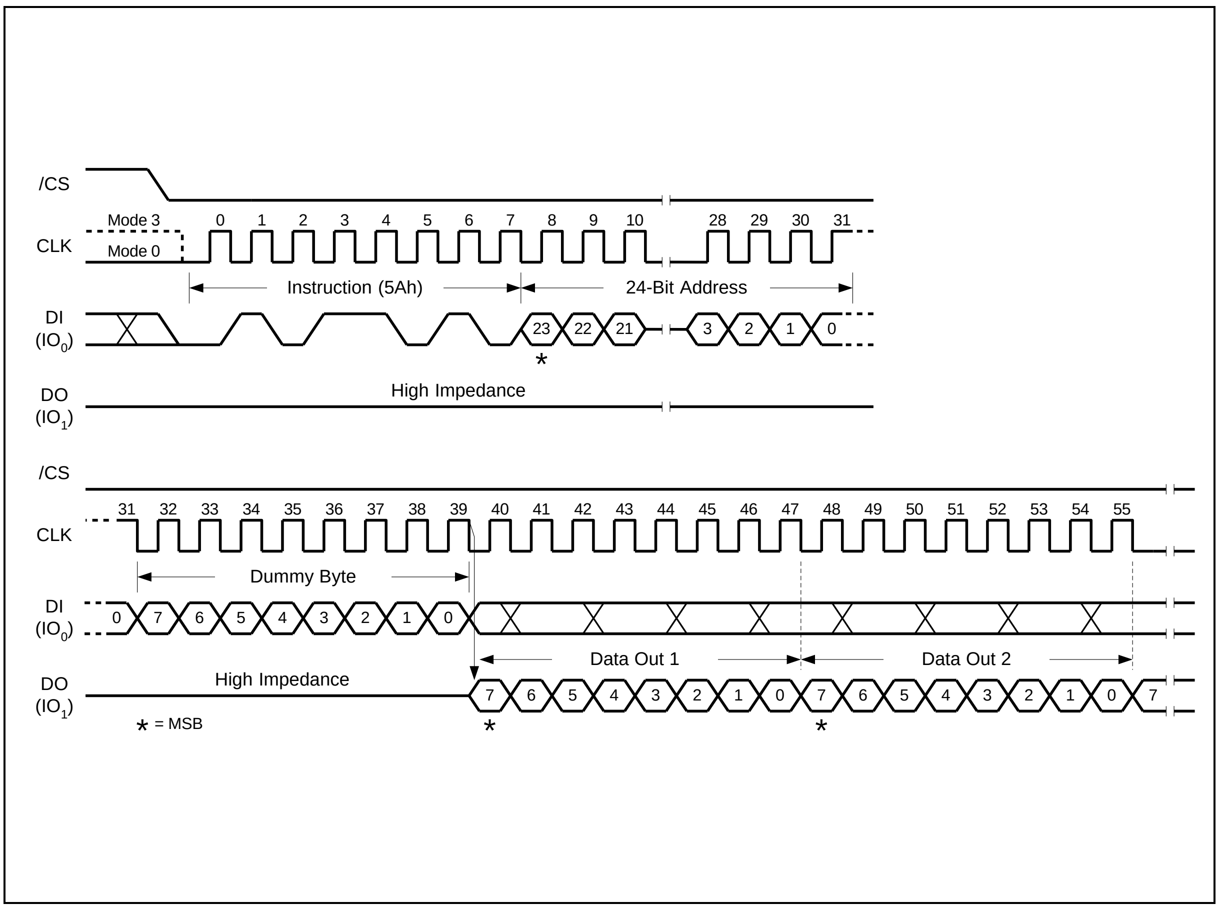


Figure 31. Read SFDP Register Instruction Sequence Diagram

7.2.33 Erase Security Registers (44h)

The W25Q80BV offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don't Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don't Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don't Care

The Erase Security Register instruction sequence is shown in figure 32. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits LB[3:1] in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (See 7.1.9 for detail descriptions).

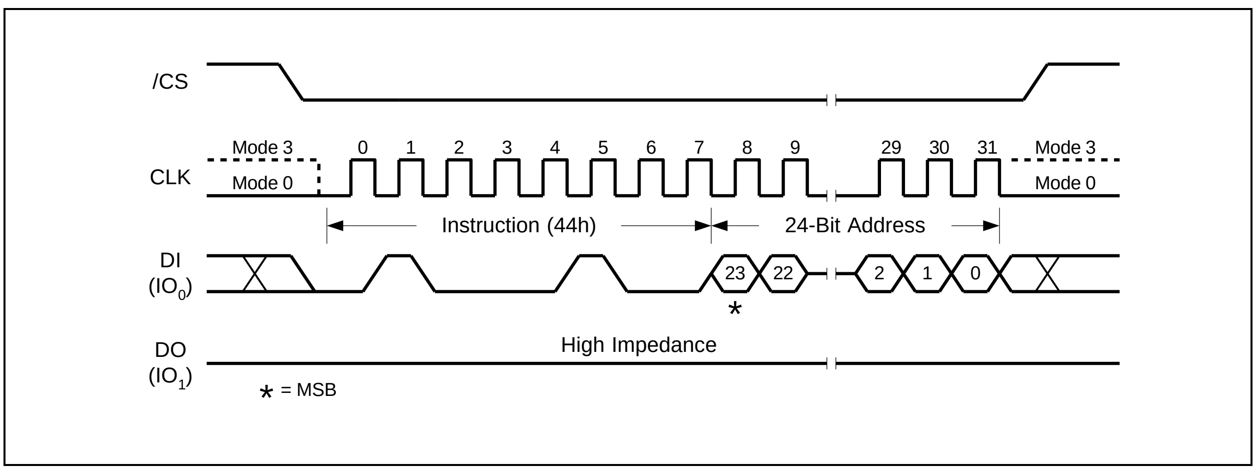


Figure 32. Erase Security Registers Instruction Sequence

7.2.34 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in figure 33. The Security Register Lock Bits LB[3:1] in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 7.1.9, 7.2.17 for detail descriptions).

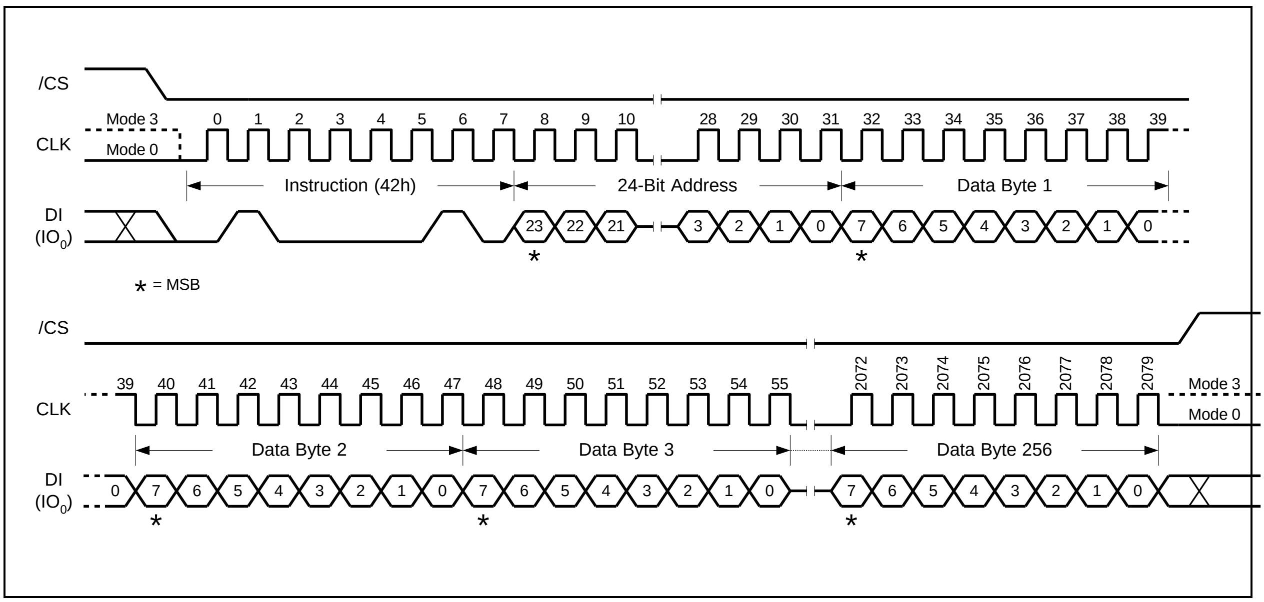


Figure 33. Program Security Registers Instruction Sequence

7.2.35 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code "48h" followed by a 24-bit address (A23-A0) and eight "dummy" clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in figure 34. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

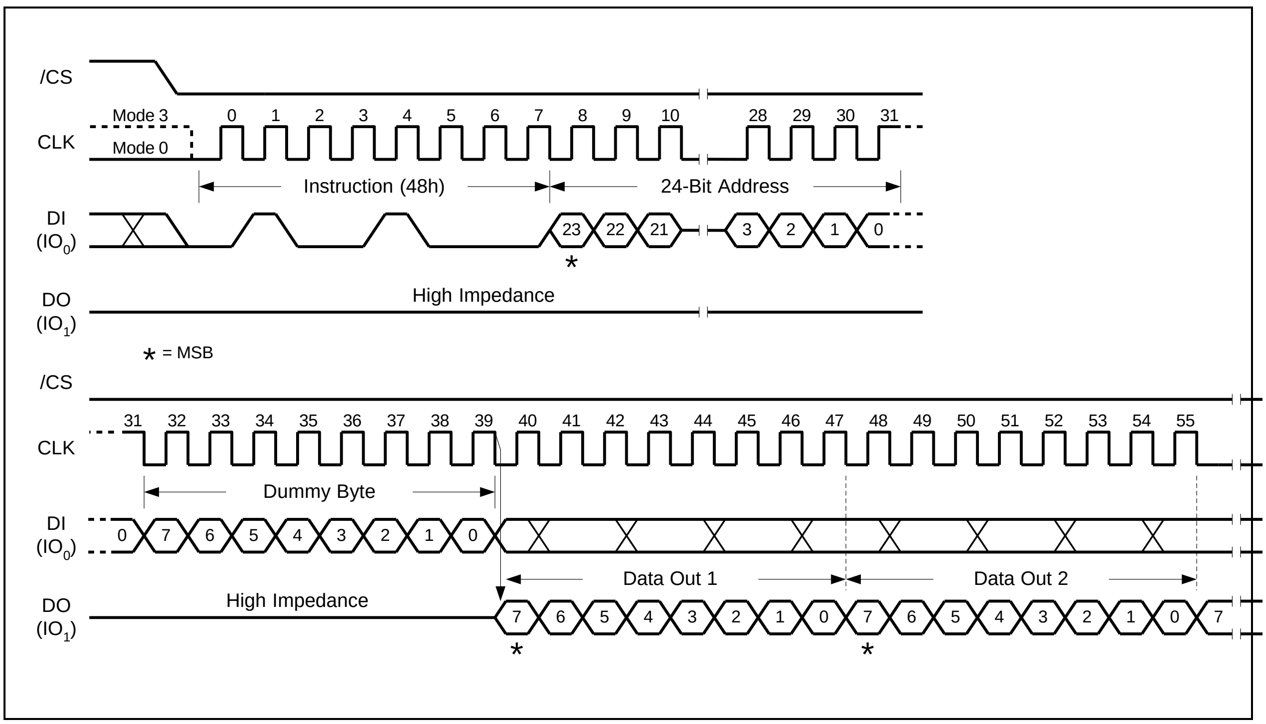


Figure 34. Read Security Registers Instruction Sequence

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings [1]

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	T_{STG}		–65 to +150	°C
Lead Temperature	T_{LEAD}		See Note [2]	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model[3]	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	F_R = 80MHz, f_R = 50MHz Industrial Plus Grade Automotive Grade 3 Automotive Grade 2	2.7	3.6	V
Supply Voltage	VCC	F_R = 66MHz, f_R = 50MHz Automotive Grade 1	2.7	3.6	V
Ambient Temperature, Operating	T_A	Industrial Plus Grade Automotive Grade 3 Automotive Grade 2 Automotive Grade 1	-40	+105 +85 +105 +125	°C

8.3 Power-up Timing and Write Inhibit Threshold

Parameter	Symbol	spec		Unit
		MIN	MAX	
VCC (min) to /CS Low	tVSL(1)	20		µs
Time Delay Before Write Instruction	tPUW(1)	5		ms
Write Inhibit Threshold Voltage	VWI(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

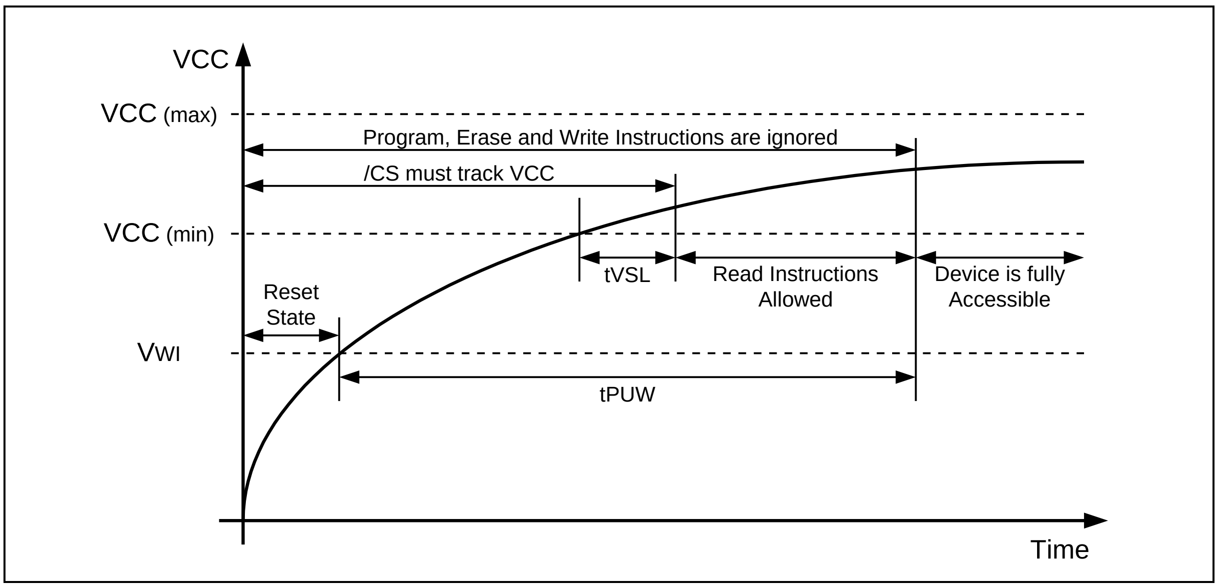


Figure 35a. Power-up Timing and Voltage Levels

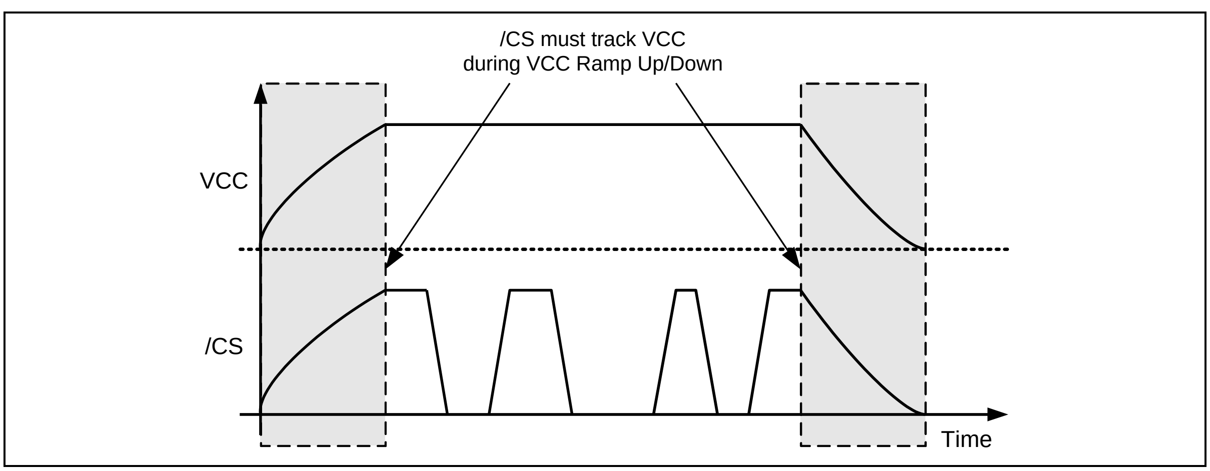


Figure 35b. Power-up, Power-Down Requirement

8.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	$I_{CC}1$	/CS = VCC, VIN = GND or VCC		25	50	µA
Power-down Current	$I_{CC}2$	/CS = VCC, VIN = GND or VCC		1	10	µA
Current Read Data / Dual /Quad 1MHz(2)	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		4/5/6	10	mA
Current Read Data / Dual /Quad 33MHz(2)	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		6/7/8	12	mA
Current Read Data / Dual /Quad 50MHz(2)	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		7/8/9	14	mA
Current Read Data / Dual Output Read/Quad Output Read 80MHz(2)	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		10/11/12	18	mA
Current Write Status Register	$I_{CC}4$	/CS = VCC		8	15	mA
Current Page Program	$I_{CC}5$	/CS = VCC		20	30	mA
Current Sector/Block Erase	$I_{CC}6$	/CS = VCC		20	30	mA
Current Chip Erase	$I_{CC}7$	/CS = VCC		20	30	mA
Input Low Voltage	V_{IL}				VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7			V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3V.
2. Checker Board Pattern.

8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

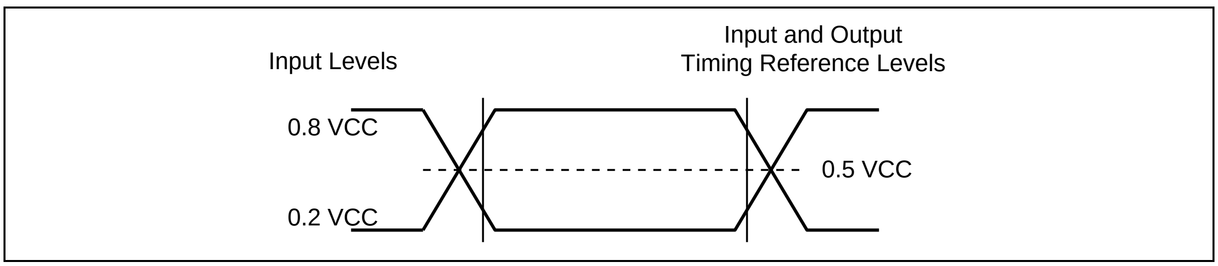


Figure 36. AC Measurement I/O Waveform

8.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions except Read Data (03h) for Automotive Grade 2/3 & Industrial Grade Plus	F_R	f_C	D.C.		80	MHz
Clock frequency for all instructions except Read Data (03h) for Automotive Grade 1	F_R	f_C	D.C.		66	MHz
Clock frequency for Read Data instruction (03h)	f_R		D.C.		50	MHz
Clock High, Low Time for all instructions except Read Data (03h)	t_{CLH1}, t_{CLL1}[1]		4			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}[1]		8			ns
Clock Rise Time peak to peak	t_{CLCH}[2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}[2]		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		5			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		5			ns
/CS Deselect Time (for Array Read → Array Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase or Program → Read Status Registers) & Volatile Status Register Write Time	t_{SHSL2}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ}[2]	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV1}	t_{V1}			7	ns
Clock Low to Output Valid (for Read ID instructions)	t_{CLQV2}	t_{V2}			8	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns

Continued – next page

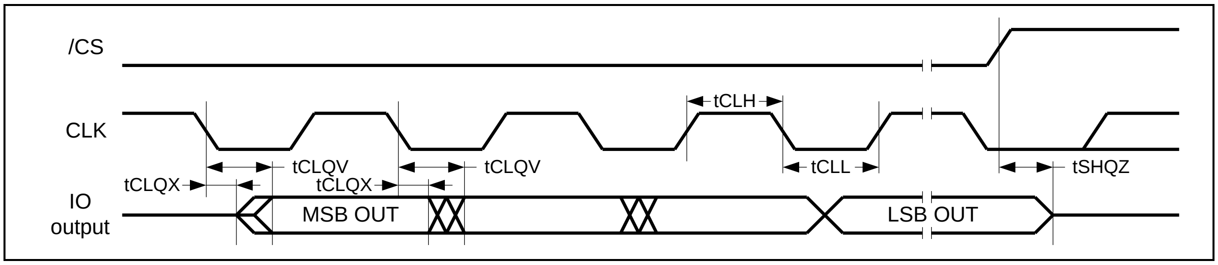
8.7 AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
Suspend Instruction after Program Resume	t_{RSM1}		60			µs
Suspend Instruction after Erase Resume	t_{RSM2}		500			µs
Write Status Register Time	t_W			10	15	ms
Byte Program Time (First Byte) (4)	t_{BP1}			30	60	µs
Additional Byte Program Time (After First Byte) (4)	t_{BP2}			3	15	µs
Page Program Time	t_{PP}			0.8	4	ms
Sector Erase Time (4KB)	t_{SE}			30	400	ms
Block Erase Time (32KB)	t_{BE1}			120	800	ms
Block Erase Time (64KB)	t_{BE2}			150	1,000	ms
Chip Erase Time	t_{CE}			2	6	s

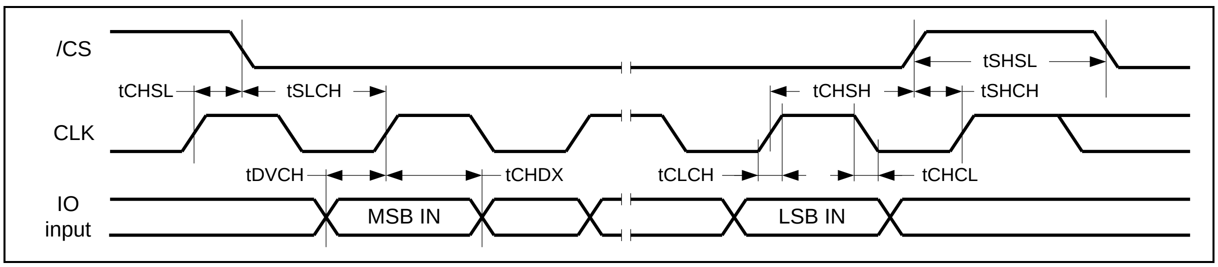
Notes:

1. Clock high + Clock low must be less than or equal to $1/f_C$.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).
4. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

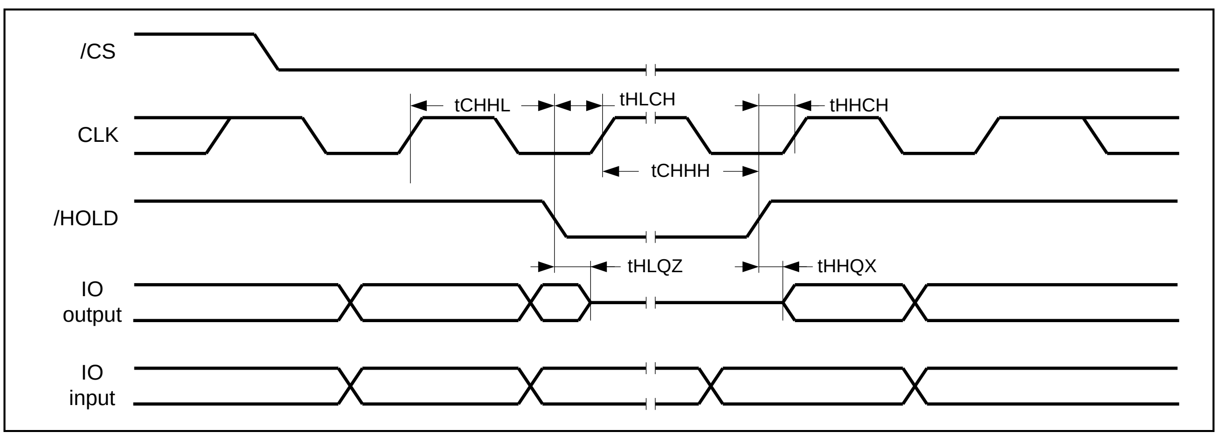
8.8 Serial Output Timing



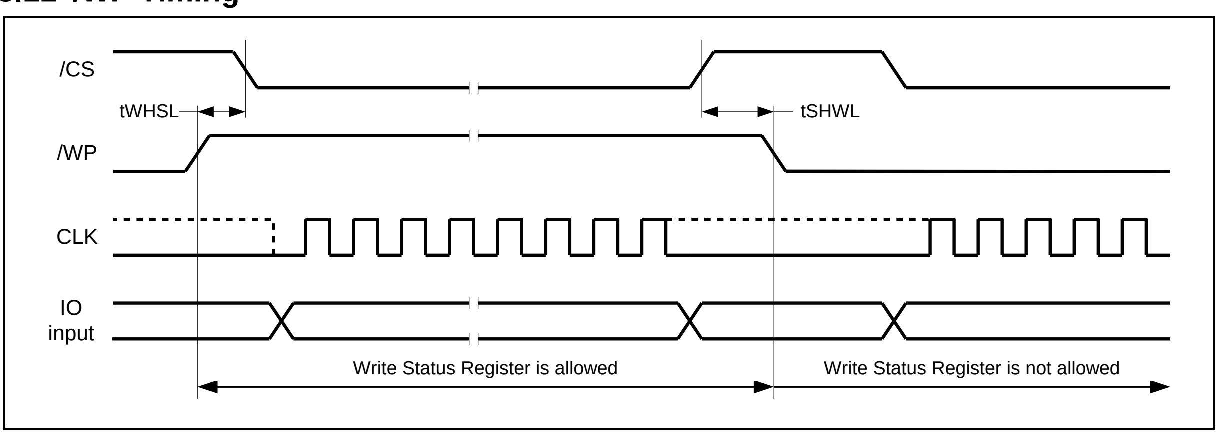
8.9 Serial Input Timing



8.10 /HOLD Timing

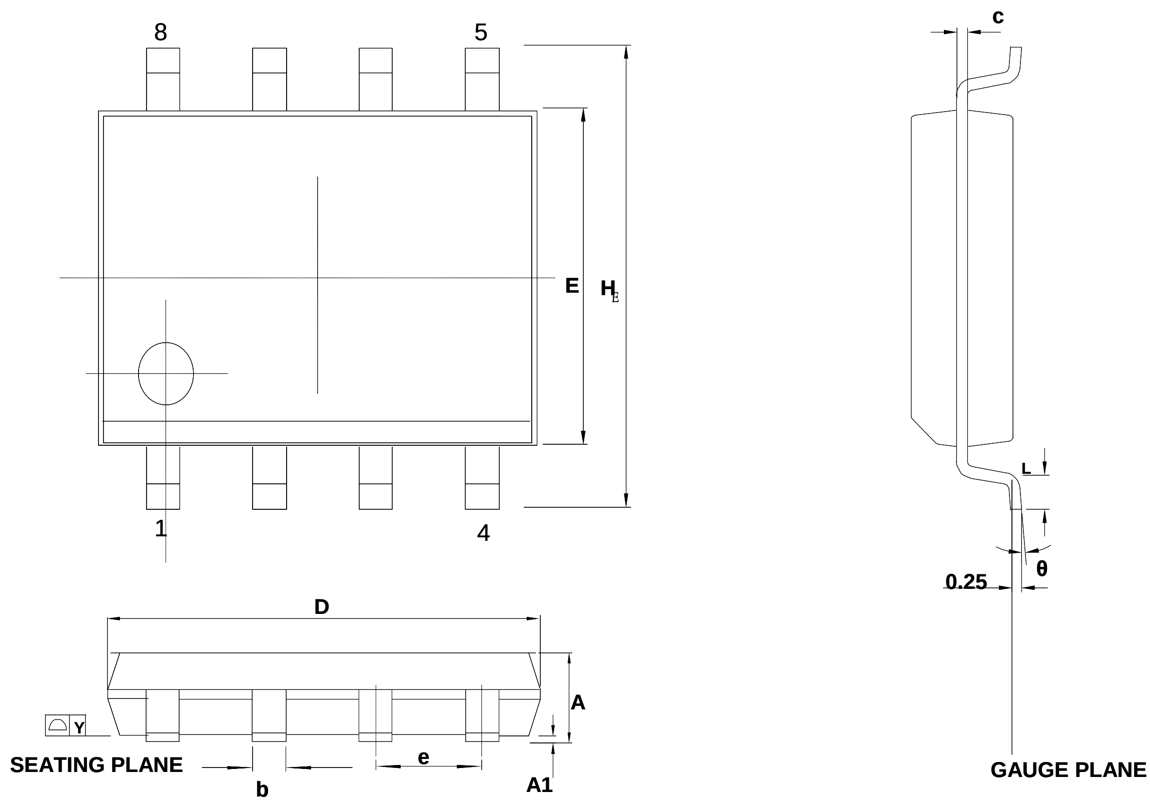


8.11 /WP Timing



9. PACKAGE SPECIFICATION

9.1 8-Pin SOIC 150-mil (Package Code SN)

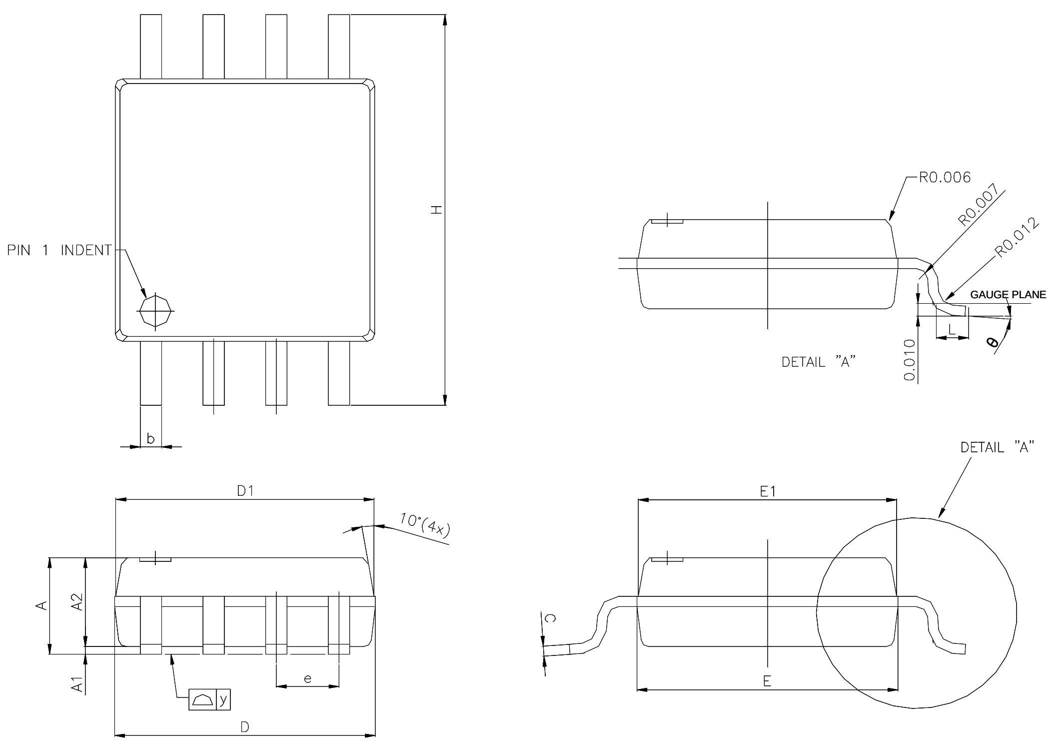


SYMBOL	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E[3]	3.80	4.00	0.150	0.157
D[3]	4.80	5.00	0.188	0.196
e[2]	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y[4]	---	0.10	---	0.004
L	0.40	1.27	0.016	0.050
θ	0°	10°	0°	10°

Notes:

1. Controlling dimensions: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads coplanarity with respect to seating plane shall be within 0.004 inches.

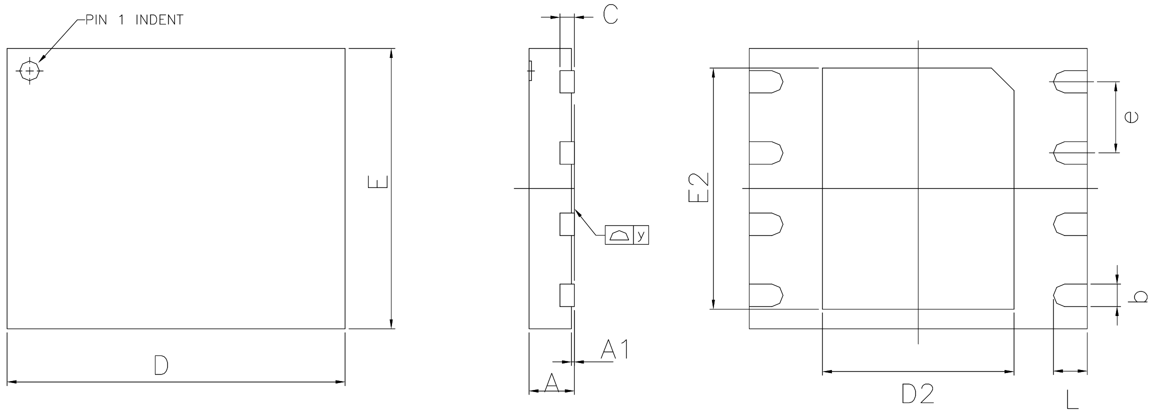
9.2 8-Pin SOIC 208-mil (Package Code SS)



SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e(2)		1.27 BSC.			0.050 BSC.	
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

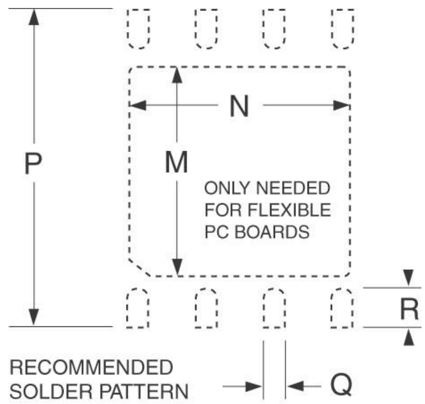
Notes:
1. Controlling dimensions: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads coplanarity with respect to seating plane shall be within 0.004 inches.

9.3 8-Pad WSON 6x5mm (Package Code ZP)



SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF.	---	---	0.008 REF.	---
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	4.25	4.30	4.35	0.167	0.169	0.171
e(2)	1.27 BSC.			0.050 BSC.		
L	0.55	0.60	0.65	0.022	0.024	0.026
y	0.00	---	0.075	0.000	---	0.003

8-Pad WSON 6x5mm Cont'd.

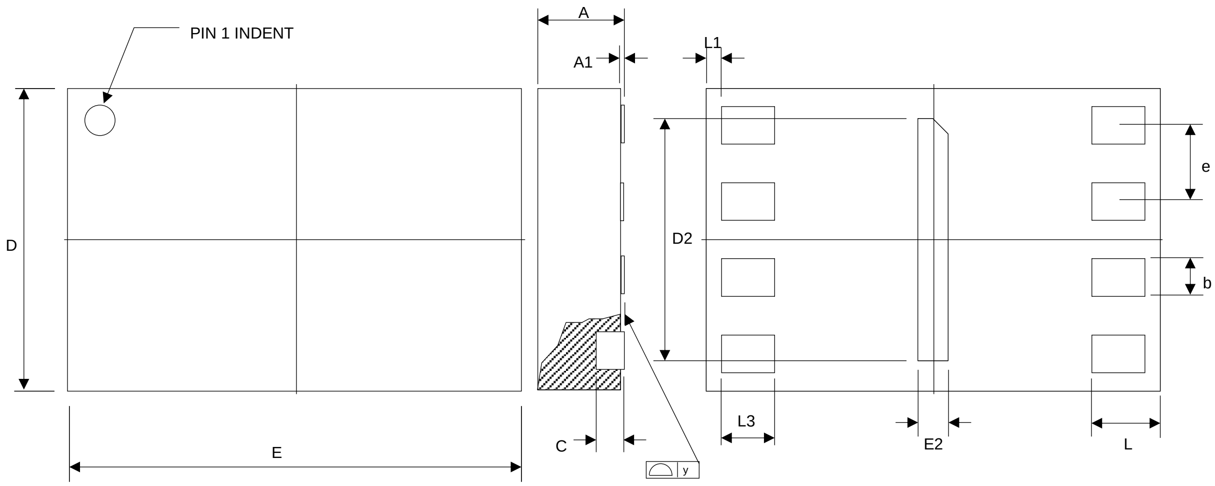


SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
SOLDER PATTERN						
M		3.40			0.134	
N		4.30			0.169	
P		6.00			0.236	
Q		0.50			0.020	
R		0.75			0.026	

Notes:

1. Advanced Packaging Information; please contact Winbond for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

9.4 8-Pad USON 2x3-mm (Package Code UX)



Note: Exposed pad dimension D2 & E2 may be different by die size.

SYMBOL	MILLIMETER			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
C	—	0.15 REF	—	—	0.006	—
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.55	1.60	1.65	0.061	0.063	0.065
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	0.15	0.20	0.25	0.006	0.008	0.010
e	—	0.50	—	—	0.020	—
L	0.40	0.45	0.50	0.016	0.018	0.020
L1	—	0.10	—	—	0.004	—
L3	0.30	0.35	0.40	0.012	0.014	0.016
y	0.000	—	0.075	0.000	—	0.003

10. ORDERING INFORMATION

W[1] 25Q 80B V xx[2] x x

Company Prefix

W = Winbond

Product Family

25Q = SpiFlash Serial Flash Memory with 4KB sectors, Dual/Quad I/O

Product Number / Density

80B = 8M-bit

Supply Voltage

V = 2.7V to 3.6V

Package Type

SN = SOIC-8 150-mil SS = SOIC-8 208-mil
ZP = WSON-8 6x5-mm UX = USON-8 2x3-mm

Temperature Range

J = Industrial Plus (-40°C to +105°C) B = Automotive Grade 3 (-40°C to +85°C)
A = Automotive Grade 2 (-40°C to +105°C) S = Automotive Grade 1 (-40°C to +125°C)

Special Options[3,4]

G = Green Package (Lead-free, RoHS Compliant, Halogen-free (TBBA), Antimony-Oxide-free Sb_2O_3)
P = Green Package with Status Register Power-Down & OTP enabled

RoHS COMPLIANT

Notes:

1. The “W” prefix is not included on the part marking.
2. Only the 2nd letter is used for the part marking; WSON package type ZP is not used for the part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
4. For shipments with OTP feature enabled devices (P), please specify when placing orders.

10.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q80BV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use an 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages use an abbreviated 10-digit number.

Part Numbers for Industrial Plus Grade Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	8M-bit	W25Q80BVSNJG	25Q80BVNJG
SS SOIC-8 208mil	8M-bit	W25Q80BVSSJG	25Q80BVSJG
ZP(1) WSON-8 6x5mm	8M-bit	W25Q80BVZPJG	25Q80BVJG
UX(2) USON-8 2x3mm	8M-bit	W25Q80BVUXJG	8DxxJ 0Gxxxx

Part Numbers for Automotive Grade 3 Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	8M-bit	W25Q80BVSNBG	25Q80BVNBG
SS SOIC-8 208mil	8M-bit	W25Q80BVSSBG	25Q80BVSBG
ZP(1) WSON-8 6x5mm	8M-bit	W25Q80BVZPBG	25Q80BVBG
UX(2) USON-8 2x3mm	8M-bit	W25Q80BVUXBG	8DxxB 0Gxxxx

Part Numbers for Automotive Grade 2 Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	8M-bit	W25Q80BVSNAG	25Q80BVNAG
SS SOIC-8 208mil	8M-bit	W25Q80BVSSAG	25Q80BVSAG
ZP(1) WSON-8 6x5mm	8M-bit	W25Q80BVZPAG	25Q80BVAG
UX(2) USON-8 2x3mm	8M-bit	W25Q80BVUXAG	8DxxA 0Gxxxx

Part Numbers for Automotive Grade 1 Temperature:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	8M-bit	W25Q80BVSNSG	25Q80BVNSG
SS SOIC-8 208mil	8M-bit	W25Q80BVSSSG	25Q80BVSSG
ZP[(1)] WSON-8 6x5mm	8M-bit	W25Q80BVZPSG	25Q80BVSG

Notes:

1. WSON package type ZP is not used in the top side marking.
2. USON package type UX has special top marking due to size limitation.
   8 = 8Mb; D = W25Q series, 3V; 0 = Standard part; G = Green.
3. Not all the part numbers are readily available for ordering, please contact Winbond for more information.

11. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	10/21/13		New Create Preliminary
B	09/02/14	5	Modified Note 1 description.
C	09/10/14	All 65	Removed preliminary designation Updated Top Side Marking for USON 2x3mm
C1	07/17/18	5	Corrected typos.

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