
# VW2010 A/V/S CODEC Chip Hardware Description

*Proprietary and Confidential*

**Preliminary**

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**Vweb Corporation**
**5300 Stevens Creek Blvd., Suite 320**
**San Jose, CA 95129, USA**

**408-615-1888**
**www.vwebcorp.com**

***Revision Table***

| Date | Version | Author | Description |
|---|---|---|---|
| June 28, 2001 | 0.1 | BR | First Revision |
| June 29, 2001 | 0.2 | BR | Improved the audio section, added information for the video decode path and enhanced the information about motion refinement. |
| July 6, 2001 | 0.3 | BR | Changed the audio pin-out section. |
| July 31, 2001 | 0.4 | BR | Changed the audio input and output descriptions |
| Dec. 19, 2001 | 0.5 | BR | Updated the signal description and feature list |
| Feb. 15, 2002 | 0.6 | PH | Revised per recent engineering reviews |
| Feb. 28, 2002 | 0.7 | PH | Major rewrite per new info and new data flow diagrams |
| March 4, 2002 | 0.72 | PH | Corrections per engineering review |
| March 11, 2002 | 0.8 | PH | Conversion and production; corrections per review |
| March 15, 2002 | 0.81 | PH | Corrections and updates |
| March 31, 2002 | 0.82 | PH | Pin-out corrections and updates |
| April 12, 2002 | 0.83 | PH | Misc. corrections and updates throughout |
| April 23, 2002 | 0.84 | PH | Pin-out corrections, more timing info, more misc info |
| May 17, 2002 | 0.85 | PH | Updated DMA engine, drive attributes, pin-outs, unused pin info; added application notes, made misc. other corrections. |
| June 11, 2002 | 0.86 | PH | Corrections to DMA, more timing and other info |
| June 25, 2002 | 0.87 | PH | General corrections |
| July 2, 2002 | 0.88 | PH | Added package dimensions, revised unused pin info |
| Aug. 6, 2002 | 0.89 | PH | Revised DMA info, new/revised timing diagrams |
| Nov. 1, 2002 | 0.90 | PH | General updates; revised HIU, DMA, pin-outs |
| Jan. 7, 2003 | 0.91 | PH | Simplified the DMA description |
| May 13, 2003 | 0.92 | PH | Fixed: host modes; host mode selection; unused pins; i2c, i2s, CDO timing diagrams; SDRAM requirements; audio PLL clock spec.; CDO legacy mode, ASI mode; interrupt pin spec; buffer sizes.<br>Added: OSD description. |

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# CHAPTER 1 *Functional Description*



## Physical Modules

The VW2010 is a very flexible MPEG-1, -2, -4 and H.263 A/V/S encoder/decoder (CODEC) chip. As Figure 1 on page 2 shows, it consists of an embedded RISC/DSP processor, a number of modules that comprise the encoder, a number of modules that comprise the decoder, and a number of I/O modules.

### MPEG Encoder Modules

The MPEG encoder in the VW2010 consists of the following modules:

- Video input unit (VIU)
- Audio input unit (AIU)
- Video encoder/compression core units
  - Motion estimation unit (MEU)
  - Motion vector refinement unit (MRU)
  - Chroma compensation unit (CCU)
  - Mode select unit (MSU)
  - Rate control unit (RCU)
  - Encoder central processor unit (eCPU)
  - Video encoder unit (VEU)
- Audio encoder/compression in the RISC/DSP processor
- Multiplexer and buffer controller (MUX and BUF)

As an MPEG audio/video encoder, the VW2010 compresses video data using a proprietary, patent-pending, motion estimation and rate control algorithm that has been optimized for low latency, fast scene detection, and smooth bit rate allocation. The embedded RISC/DSP processor packetizes the compressed data into an output MPEG stream format selected by the user. The VW2010 accepts two channels of $I^2S$ audio, and uses the audio encoder functions in the RISC/DSP to generate compressed audio data, which may be multiplexed into the output MPEG stream.

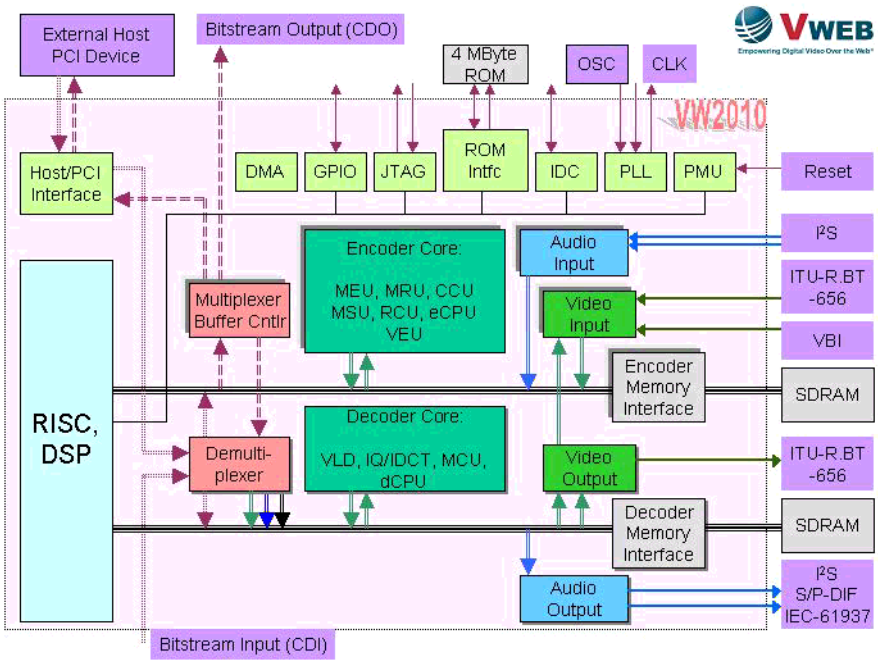


**Figure 1 Block Diagram of the VW2010**

## MPEG Decoder Modules

The MPEG decoder in the VW2010 consists of the following modules:

- Demultiplexer (DEMUX)
- Video decoder/decompression core units
  - Variable length decoding unit (VLD)
  - Inverse quantization / inverse discrete cosine transform unit (IQ/IDCT)
  - Motion compensation unit (MCU)
  - Decoder central processor unit (dCPU)
- Audio decoder/decompression in the RISC/DSP processor
- Video graphics and output unit (VOU)
- Audio output unit (AOU)

As an MPEG video and audio decoder, the VW2010 demultiplexes an MPEG bit-stream into its video, audio and user data components (if any), decompresses the video and audio information, and combines the video with graphics, Closed Caption, Teletext or other user data. The output video data is presented in standard ITU-R.BT.656 format. The output audio is available in $I^2S$ or S/P-DIF digital audio format, or as IEC-61937 compressed audio.

## System Modules

The VW2010 includes a power management module (PMU) and a number of I/O interface modules:

- Host/PCI interface (for an external processor, storage and other devices)

- DMA controller (DMA)
- ROM interface (for boot and other microcode)
- General purpose input / output (GPIO)
- Boundary scan ports (JTAG and EJTAG)
- Phase-locked loops (main PLL and audio PLL)
- Inter-device communications interface (ICI)

All of these modules are described in some detail later in this manual ("Encoder Modules" on page 19, "Decoder Modules" on page 29, and "System Modules" on page 39).

## Host Interface Modes

The host interface of the VW2010 can be configured to operate in the following host modes:

- 16-bit Motorola-style mode
- 16-bit Intel-style mode
- PCI target mode

These modes can be selected at power-up / reset, as described in the section titled "Host Mode" on page 49.

## Data Paths

Transfer of data among these modules takes place using the following means:

- Direct input and output ports (shown in Figure 2 on page 5)
- Two dedicated high-speed SDRAM buses (shown in Figure 2 on page 5)
- DMA channels between selected modules (shown in Figure 3 on page 8)

The main I/O ports of the VW2010 are shown in Figure 2 on page 5. A list and description of the I/O signals are presented at the end of this manual ("Encoder Interface Signals" on page 63, "Decoder Interface Signals" on page 69, and "System Interface Signals" on page 75).

Two dedicated high-speed SDRAM buses connect the RISC to the two SDRAM interfaces. The encoder SDRAM bus is 32 bits wide, and the decoder SDRAM bus is 64 bits wide. Both interfaces to the external SDRAM devices are 32 bits wide. All modules in the encoder exchange data among themselves via the encoder SDRAM bus. All modules in the decoder exchange data among themselves via the decoder SDRAM bus.

To perform the functions of the VW2010, the physical data paths can be used to facilitate the following functional data paths between I/O and encoder/decoder modules:

- Taking ITU-R.BT.656 video data and VBI data from the video input ports, and $I^2S$ audio data from the audio input ports.
- Encoding this same data.
- Presenting compressed data on the compressed data out port, or on the host/PCI port.
- Taking compressed video (+ audio + user) data from the compressed data input port, or the host/PCI port.
- Decoding this same data.
- Presenting the ITU-R.BT.656 video on the video output port.
- Presenting $I^2S$ and S/P-DIF digital audio or IEC-61937 compressed audio on the audio output ports.
- Transrating / transcoding.
- Time shifting.

Two control buses are used to set up and configure these data paths, as described under "Control Buses" on page 8.

*Note:* All internal buses and all I/O buses of the VW2010 are big-endian. (Among other things this means that bit 0 is the least significant bit.) The only exception is the host/PCI port:

*Note:* The host/PCI port may be big-endian or little-endian, depending on the host mode. For more details, see "Host Interface, Motorola Mode" on page 76 and "Host Interface, Intel Mode" on page 78.

For a more detailed discussion of the internal data paths, given in terms of the data buffers set up in SDRAM, see the sections titled "Encoder Buffers" on page 22 and "Decoder Buffers" on page 30.

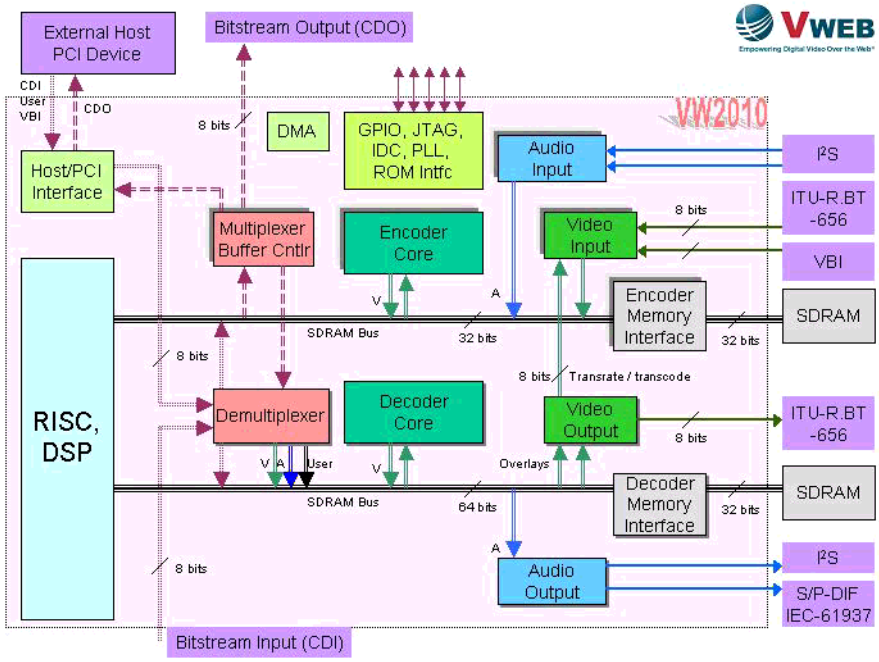


**Figure 2 Data Path Diagram of the Vweb VW2010**



## Uncompressed Data Input Paths

The video data to be encoded is available on one of the video input unit's (VIU) input ports:

- 8-bit ITU-R.BT.656 uncompressed video data
- 8-bit VBI data
- A special 8-bit port from the video output unit (VOU) that is used in transcoding/transrating applications.

The audio data to be encoded is available on the two $I^2S$ input ports of the audio input unit (AIU).

## Encoder Path

The VIU filters and loads its input data into the encoder SDRAM via the high speed encoder SDRAM bus. The video encoder core modules retrieve this data from SDRAM as needed. The video encoding core modules read and write to the SDRAM the intermediate and final results of the MPEG-1, -2, -4 or H.263 encoding process. This compressed data is available to the multiplexer in the RISC via the SDRAM.

The AIU sends its input data to the RISC via the encoder SDRAM. Audio compression is done by the audio digital signal processing (DSP) extensions in the RISC. The DSP puts the compressed audio back into SDRAM so the data will be available to the multiplexer in the RISC.

In the RISC, the compressed video from the encoder core modules is optionally combined with compressed audio, and with user data, if any; then the data is multiplexed and/or processed for network delivery. The resulting compressed data stream (CDO bitstream) is sent to the multiplexer buffer controller (BUF) via the encoder SDRAM bus.

By this time the CDO is a regular MPEG bitstream (SS, PS, TS, ES or PES, depending on how the encoder was set up). For the sake of generality, in this document this MPEG bitstream is still called CDO.

### Compressed Data Output Paths (CDO)

Under control by the RISC, the multiplexer buffer controller (BUF) sets up the appropriate buffers and FIFOs, and routes the CDO bitstream to the host/PCI interface unit's output port, or directly to the dedicated 8-bit parallel or 1-bit serial CDO output port.

### Compressed Data Input Paths (CDI)

Multiplexed / combined / compressed data input bitstream (CDI), as well as user data and VBI, can be input on one of the input ports: on the host/PCI port, or on the dedicated 8-bit parallel / 1-bit serial CDI input port. From these ports, the data is internally routed to the demultiplexer (DEMUX), which directly stores the data in the decoder or encoder SDRAM via the corresponding high speed SDRAM bus (without demultiplexing at this time).

There is no separate compressed audio input path. It is assumed the CDI bistream may contain or may consist of tagged video, audio or user data components.

### Decoder Paths

Decoder processing begins in the RISC. It selects buffers and FIFOs for use by the demultiplexer (DEMUX). The DEMUX retrieves the CDI from SDRAM, extracts video, audio and user data from the CDI, and places each type of data into their separated buffers and FIFOs. The data flow between the decoder modules the takes place via the decoder SDRAM, as follows.

The demultiplexer (DEMUX) extracts video data from the CDI bitstream, and sends it to the video decoder core via the decoder SDRAM. The video decoder core modules retrieve this data from SDRAM as needed. The video decoding core modules read and write to the SDRAM the intermediate and final results of the MPEG-1, -2, -4 or H.263 decoding / decompressing / filtering calculations. The decoder core sends the resulting video data to the video output unit (VOU) via SDRAM. The VOU completes the conversion of the video data to the ITU.R-BT.656 format. The VOU also contains a graphics module, which, under user control, can generate multiple graphics overlays to be superimposed on the video.

The DEMUX extracts user data from the CDI bitstream, and sends it to the decoder SDRAM, for further processing by the RISC. In the RISC, user data is converted to Closed Caption or Teletext data, and sent back into SDRAM as VBI data to be mixed with the video data in the VOU.

The DEMUX extracts audio data from the CDI bitstream, and sends it to the decoder SDRAM. The audio is decompressed using the DSP extensions within the RISC, and put back into SDRAM. The audio output unit (AOU) retrieves this data from SDRAM and converts it to $I^2S$ or S/P-DIF format.

### Uncompressed Data Output Paths

The VOU sends video data in ITU.R-BT.656 format either to an off-chip NTSC/PAL encoder (to be displayed on a standard television screen), or back to the video input unit (VIU) in transrating/trancoding applications.

The decompressed audio output of the AOU is presented on the $I^2S$ or S/P-DIF ports.

Compressed audio in IEC-61937 format is available as a bypass option on the S/P-DIF port.

### Transcoding / Transrating Path

The VW2010 can be used to transrate (change the bit rate of) or transcode (change the MPEG encoding format of) a video data stream. Either application requires both the encoder and the decoder. By definition a data stream to be transrated or transcoded is a CDI, therefore first it must be decoded as usual (that is, as described above). However, instead of presenting it as ITU-R.BT.656 data to an external NTSC/PAL encoder, it is routed as input to the VIU on an internal 8-bit data path between the decoder's VOU and the encoder's VIU. Thus introduced into the encoder data path, the data can be re-rated or re-coded as desired, and routed to any of the CDO ports, just like any other CDO bitstream.

### Time Shifting Path

The VW2010 can be used to do time shifting. This application requires both the encoder and the decoder. In this case the program to be time-shifted (from the external NTSC/PAL decoder) is an input to the VIU, encoded as usual, and written out as CDO to an external storage device (such as a hard disk). At a later time of the viewer's choosing, the compressed data is retrieved from the external storage device, input to the decoder as a CDI bitstream, decoded as usual, and sent back out as ITU-R.BT.656 data to an external NTSC/PAL encoder.



## DMA Data Paths

The data paths that can be set up via DMA channels between selected modules in the VW2010 are shown in Figure 3 on page 8. (Some of the data paths described in previous sections are actually implemented by means of these DMA paths.) As the figure shows, the DMA engine can be thought of as a direct bridge between the following devices in the chip:

- The dmem data cache in the RISC
- External host memory, via the host/PCI interface
- The encoder SDRAM, via the EMIU
- The encoder MUX (and then the EMIU and the encoder SDRAM)
- The decoder SDRAM, via the DMIU
- The decoder DEMUX (and then the DMIU and decoder SDRAM)

Note that not every possible combination of source and destination devices is supported by the DMA engine. For specific details, see "DMA Controller" on page 46.

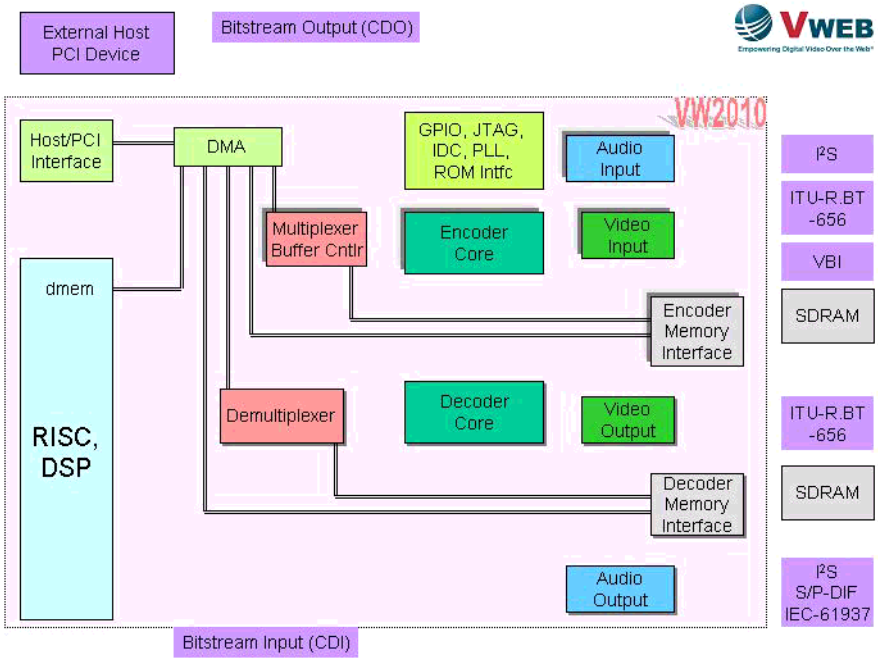


**Figure 3 DMA Data Paths of the Vweb VW2010**

The DMA engine uses the internal 32-bit SDRAM bus to talk to the encoder's EMIU and BUF. The DMA engine uses the internal 64-bit SDRAM bus to talk to the decoder's DMIU and DEMUX. As both of there buses are connected to the RISC, dmem can send or receive data on whichever one is active at the time. The DMA engine uses the internal CDI/CDO bus to talk to the HIU's holding buffer for host/PCI memory.

*Note:* As Figure 3 on page 8 indicates (by omission), the chip's direct CDO port, and the bus from the MUX to the CDO port, are not available to the DMA engine.

For more detail, see the section titled "DMA Controller" on page 46.



## Control Buses

The DMA channels and other I/O paths are set up and configured by means of signals on a control bus for the encoder and another control bus for the decoder. Both control buses are connected to the host interface unit (HIU). The DMA module, as well as the other I/O modules, gain control of these buses by bridging with the HIU. This is shown schematically in Figure 4 on page 9.

The embedded RISC or external host processor gains control over these buses, and therefore the DMA and other I/O data paths, by means of internal registers. Note the following:

- The hardware path from the embedded RISC or external host processor to the registers is provided via the HIU.
- Software access is provided by high-level protocols and APIs, not by direct access to registers or microcode.

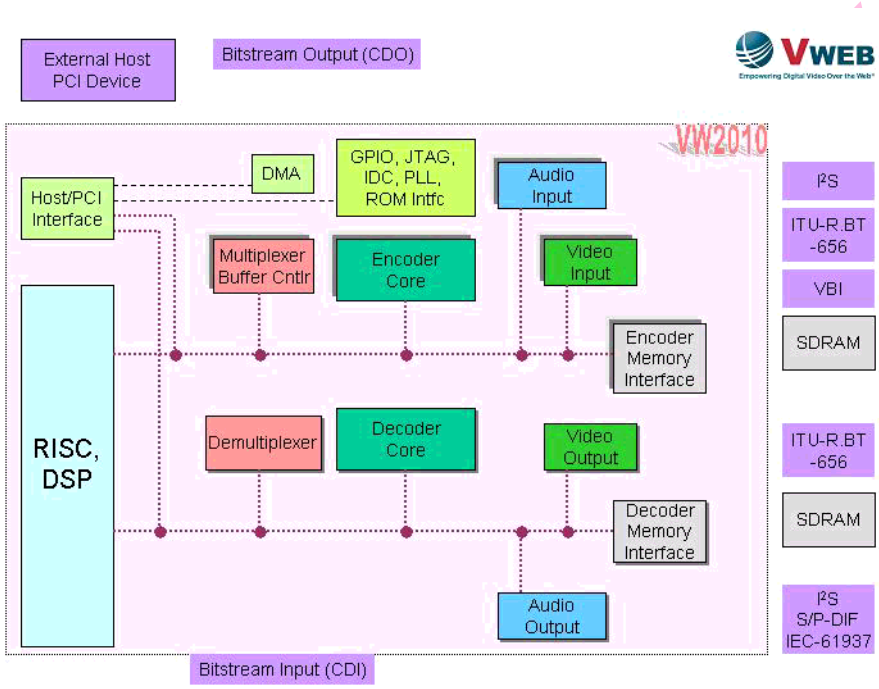


**Figure 4 Control Buses of the Vweb VW2010**



## Microcode

A number of modules in the VW2010 require microcode to operate. These include, for example, the RISC processor as well as the dedicated RISC engines in the encoder and decoder core. As Figure 1 on page 2 indicates, the VW2010 chip design anticipates that the microcode would be stored in an external ROM (flash, EEPROM or other type of ROM device); the ROM interface is built into the chip.

The microcode from this ROM would be downloaded into the chip at power-up / boot time. As the signal multiplexing scheme described in the chapter titled "Pin Lists" on page 87 indicates, the ROM data pins are available for other uses after power-up.

The size of ROM may depend on user preference or board design; however, one 4-Mbyte ROM, such as an AT49BV1614, should be sufficient for each VW2010 chip used in the design. (See Figure 23 on page 59.) The minimum required ROM space is set by the type and size of firmware used on the board, but typically is not expected to exceed 512KB. (Vweb reference/debug board designs place a ROM of 2 or 4 MB on the board).

However, it is also possible to load the microcode from an external host via the HIU. In such a design, the user may still need to keep basic boot parameters in a small ROM device (even such as a 128-byte SEEPROM). In such a case the boot parameters could be programmed into the ROM via the ICI bus, and at boot time loaded from the ROM into the VW2010 again via the ICI bus. (See Figure 24 on page 59; see also "Boot from ICI" on page 46.)

# CHAPTER 2 *Feature Set*

The VW2010 is a real-time MPEG-1, -2 and -4 audio/video/system CODEC chip (simultaneous compression/decompression, or encode/decode) that fully complies with ISO/IEC-11172-2, ISO/IEC-13818-2, ISO/IEC-14496-2 and ITU-T H.263 (baseline). The video encoder accepts uncompressed ITU-R.BT.656 digital video. It filters the input and compresses the video into MPEG-1, -2, -4 or H.263 formats. The audio encoder accepts two independent channels of $I^2S$ digital audio, filters the input, and compresses each audio into MPEG-1, MPEG-2, MP3, AAC, or AC-3 audio formats. The VW2010 outputs them as transport streams for network applications or program streams for storage applications. The video decoder accepts an MPEG bit-stream and outputs ITU-R.BT.656 digital video. The audio decoder accepts an MPEG-1, MPEG-2, MP3, AAC, or AC-3 bitstream and outputs $I^2S$, S/P-DIF or IEC-61937 audio.

This chapter tabulates the feature set of the VW2010. The features are described in greater detail in subsequent chapters.



## Feature List

### Video Encoding

- Support for MPEG-1
- Support for MPEG-2 MP@ML
- Support for MPEG-4 Simple Profile @ L1, L2 and L3, with extensions to full D1 and interlaced video
- Adaptive field/frame motion compensation and DCT type
- 4:2:2 to 4:2:0 conversion
- Scene change detection
- Inverse telecine (3:2 pulldown)
- Motion estimation search range ±127 pels horizontal and ± 63 pels vertical, with half-pel accuracy
- 8-tap horizontal filter and 4-tap vertical filter

- Extraction of VBI data (including close captioned and NABTS data) from the ITU-R.BT.656 input
- Support for private and user data insertions from VBI port or host/PCI port
- Dynamically adjustable controls
  - Fixed frame rates of 29.97 (NTSC) or 25 (PAL) frames per second, or variable frame rates in low delay mode
  - Constant or variable bit-rate from 22.5 Kb/s to 15 Mb/s
  - Horizontal resolution between 128 pixels and 720 pixels in 16-pixel steps
  - Vertical resolution between 80 pixels and 480 pixels (NTSC) or 576 pixels (PAL) in 16-pixel steps
- Programmable GOP structure and length: I, IP, IBP and IBBP
- Programmable low delay mode

## Audio Encoding

- MPEG-1 Layer I, II
- MPEG-1 Layer III (MP3)
- MPEG-2 Layer I and II
- 2-channel consumer-grade AAC
- 2-channel consumer-grade AC-3
- G.7xx
- Sampling frequencies: 8, 16, 22.05, 24, 32, 44.1, 48 and 96 KHz.
- Number of bits per channel: 16, 20, 24, 32 bits

## Video Decoding

- MPEG-1, -2, -4 and H.263 baseline decoding
- 7-tap horizontal filter and 2-tap vertical filter
- Letterbox conversion
- 3:2 pulldown
- Closed Captioning and Teletext

## Audio Decoding

- MPEG-1 Layer I, II
- MPEG-1 Layer III (MP3) [1]
- MPEG-2 Layer I and II
- 2-channel consumer-grade down-mixed AAC [1]
- 2-channel consumer-grade down-mixed AC-3 [1]
- G.7xx [1]
- Sampling frequencies: 8, 16, 22.05, 24, 32, 44.1, 48 and 96 KHz.
- Number of bits per channel: 16, 20, 24, 32 bits
- For S/P-DIF, 32, 44.1 and 48 KHz at 32 bits

## Multiplexing

***Input***

- User data or VBI data insertion
- Video and audio Elementary Stream (ES) or Packetized Elementary Stream (PES)

***Output***

- MPEG-1 System Stream

1. Future option

- MPEG-2 Program Stream (PS) or Transport Stream (TS)
- MPEG-4 video encapsulated in MPEG-2 TS
- ES and PES output without multiplexing

## Demultiplexing

***Input***

- System stream, program stream, and transport stream

***Output***

- Program clock recovery (PCR)
- 7 output buffers: 1 video, 4 audio, 1 PSI, 1 user (subtitle, Teletext)

## Graphics

- Background (solid color) plane
- MPEG video plane
- Two 32-bit ARGB (RGB with alpha-blending) or AYUV (YUV with alpha-blending) 8:8:8:8 graphics planes
- Cursor plane
- 2-, 4- or 8-bit color indexing
- 0.5X or 2X vertical scaling; arbitrary horizontal scaling on 16-pixel boundaries (letterboxing, QSIF to SIF, SIF to D1, D1 to SIF, SIF to QSIF)
- Per-pixel alpha-blending
- Deflicker filter

## MPEG-4 / MPEG-2 Feature Differences

Table 1 summarizes features that represent an MPEG-4 enhancement over MPEG-2.

The VW2010 encoder supports most features of MPEG-4 Simple Profile (including but not limited to the features listed in this Table), plus some additional features of the MPEG-4 Advanced Simple Profile (flagged with "ASP" in this Table), as noted in the "Implementation" column.

The VW2010 decoder supports all features of the encoder, plus additional features of MPEG-4 Simple Profile and MPEG-4 Advanced Simple Profile (flagged with "SP" and "ASP" in this Table), as noted in the "Implementation" column.



**Table 1 MPEG Feature Enhancements Implemented in the VW2010**

| Feature | Implementation | | | | SP[1] / ASP[2] | Benefit |
|---|---|---|---|---|---|---|
| | MPEG-2 Encoder | MPEG-2 Decoder | MPEG-4 Encoder | MPEG-4 Decoder | | |
| Prediction | One-directional DC prediction | One-directional DC prediction | AC/DC prediction | AC/DC prediction | SP | Saves bits |
| Quantization style | MPEG-2 | MPEG-2 | MPEG-2 | MPEG-2 | ASP | Medium-high bit rate |
| | | | H.263 | H.263 | SP | Low bitrate |
| Bits per macro-block | Quantizer coding, 5 bits for quantizer per macroblock | Quantizer coding, 5 bits for quantizer per macroblock | Dquant coding, 2 bits for quantizer per macroblock | Dquant coding, 2 bits for quantizer per macroblock | SP | Saves bits |

**Table 1 MPEG Feature Enhancements Implemented in the VW2010 (Continued)**

| Feature | Implementation | | | | SP[1] ASP[2] | Benefit |
|---|---|---|---|---|---|---|
| | MPEG-2 Encoder | MPEG-2 Decoder | MPEG-4 Encoder | MPEG-4 Decoder | | |
| VLC tables | MPEG-2 VLC tables | MPEG-2 VLC tables | H.263 VLC tables | H.263 VLC tables | SP | Low bitrate |
| Motion vector prediction | One-directional | One-directional | Median value - based | Median value - based | SP | Saves bits |
| No. of motion vectors | 2 motion vectors (one-directional) | 2 motion vectors (one-directional) | 2 motion vectors (one-directional) | 4 motion vectors (one-directional) | SP | Medium-high bit rate, detail-focused app's |
| Unrestricted motion vectors | No | No | No | Yes | SP | Scenes with global motion |
| Motion estim. accuracy | Half-pel | Half-pel | Half-pel | Half-pel | SP | |
| Global motion estimation | No | No | No | No | ASP | Scenes with global motion |
| Error resilience | No | No | No | Yes | SP | Robust to errors |
| Coding | Interlaced<br>Non-interlaced | Interlaced<br>Non-interlaced | Interlaced (frame DCT / field predict.)<br>Non-interlaced | Interlaced (frame DCT / field predict.)<br>Non-interlaced | ASP | Interlaced I/O |
| B-frames | Yes | Yes | No | No | ASP | Medium-high bit rate |

1. "SP" = MPEG-4 Simple Profile

2. "ASP" = MPEG-4 Advance Simple Profile



## General System Facts

- 162 MHz MIPS-like RISC processor with DSP extensions for multiplexing, demultiplexing, audio encoding and audio decoding
- 365-pin PBGA package; physical dimensions: 27 mm by 27 mm
- Input voltages: 1.8 V (internal), 3.3 V (I/O)

- Estimated power consumption: under 1.0 W in normal operating mode (see Table 18 on page 147);
  On-chip power management
- Boundary scan and assembly testing compliant with IEEE 1149.1 (JTAG) and EPI EJTAG 2.0 (extended JTAG)

# Interfaces

## Host Interfaces

- 16-bit Motorola-style interface
- 16-bit Intel-style interface
- PCI interface, target mode: 32 bits, 33 MHz

## System Interfaces

- GPIO (general purpose input/output): 12 pins
- ROM interface
- ICI (inter-device communication interface, similar to Philips $I^2C$ master mode)
- SDRAM
  - 32-bit memory interface, using 1Mx16-5 or 2Mx32-5 SDRAM
  - Minimum requirements, VW2010: 4 to 8 MB for encoder, plus 4 to 8 MB for decoder (8 MB recommended if OSD is used)

## A/V Input Interfaces

***Uncompressed Input*** MPEG Encoder

- Video: 8-bit ITU-R.BT.656
- Audio: two $I^2S$ ports
- VBI, user data: 8-bit video input

***MPEG Bitstream Input*** MPEG Decoder

- 8-bit / 1-bit compressed data input interface (CDI)
- PCI interface
- Host interface

## A/V Output Interfaces

***Compressed Output*** MPEG Encoder

- 8-bit / 1-bit compressed data output interface (CDO)
- PCI interface
- Host interface

***Uncompressed Output*** MPEG Decoder

- Video: 8-bit ITU-R.BT.656 port
- Audio: $I^2S$ port, IEC-958 S/P-DIF digital audio port with IEC-61937 compressed audio bypass
- VBI, user data:

- 1-bit (serial) bitstream using ICI or GPIO interface
- Embedded in 8-bit video bitstream

## Features and Benefits

| | |
|---|---|
| ■ Uses (less than) 8 MB of external SDRAM<br>■ 32-bit SDRAM interface<br>■ Proprietary motion estimation algorithm<br>■ MPEG-4 compression reduces storage requirements | Saves money and power |
| ■ Easy to set up and configure | Decreases time to market |
| ■ Efficient rate control algorithm monitors 60 different variables, which results in a more consistent GOP structure; thus, scene changes are handled well. | Superior video quality |
| ■ Programmable frame rates, bit rates, resolution and low delay mode<br>■ Programmable GOP structure<br>■ Transcoding and transrating among MPEG-1, -2, - 4 and H.263 | Superior flexibility |
| ■ MPEG-1, -2, -4 full-D1 interlaced encoder/decoder<br>■ Low latency support<br>■ MPEG-4 short header support (H.263 base-line support) | Superior ingenuity |



## Applications

The VW2010 is ideally suited for the following consumer applications:

- Camcorder
- Network camera
- Personal video recorder
- Set-top box
- PC capture device for video capture, content creation, and display
- VCD, Super-VCD and DVD player and recorder
- Cellular phones and PDAs

In addition, the VW2010 is suited for the following network applications:

- Streaming video distribution over DSL, cable, ethernet, fiber and wireless networks
- Transcoding and transrating among MPEG-1, -2, - 4 and H.263
- Video conferencing
- Security / surveillance
- Video-on-demand servers

# CHAPTER 3 Encoder Modules



This chapter presents more detailed descriptions of each individual encoder module's functions. Figure 5 on page 19 summarizes the encoder modules in the VW2010, and their relationships to each other. In this figure, the middle row of modules belong to the encoder.

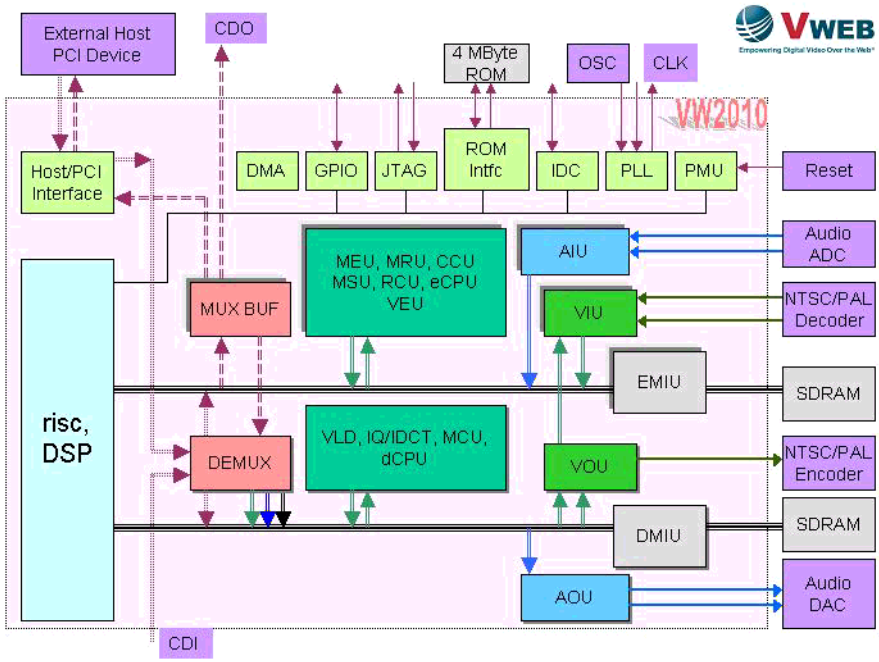


**Figure 5 Modules of the VW2010**

# Input Modules

The VW2010 encoder has two input modules:

- Video input unit (VIU)
- Audio input unit (AIU)

## Video Input Unit (VIU)

The VIU serves as the interface between the VW2010 and the uncompressed digital video data. The VIU reads a standard 8-bit ITU-R.BT.656 (parallel D1) port. The VIU performs the following functions:

- **Video input decoding**; the video input decoding process extracts the timing information and VBI data.
- **Scaling**; the scaling engine consists of a 3-line buffer, 4-tap vertical filter and 8-tap horizontal filter, which supports variable resolutions from sub-QCIF to full D1 in 16-pixel increments.
- **Color sub-sampling**; the color sub-sampling engine converts the image from the 4:2:2 to the 4:2:0 format.
- **SAD statistic gathering**; the SAD statistical gathering process supports the 3:2 pull-down engine among other prediction services.

## Audio Input Unit (AIU)

The AIU accepts uncompressed digital audio input data on two $I^2S$ channels; the encoder can process two stereo audio streams simultaneously. The AIU supports master and slave timing. When using master-timing mode, an internal timing module generates all timing signals for the external ADC. When using slave-timing mode, the AIU reads the data according to externally supplied clock signals. In the end, the audio and video clocks can be tied together using program clock recovery (PCR).

The AIU supports the audio sampling frequencies (sampling rates from 8 KHz to 96 KHz) and the bits-per-channel, left/right modes (from 16 to 32 bits) shown in the "Feature List" on page 11.

The AIU sends the audio data to the RISC/DSP via the SDRAM, for processing by the audio encoder and multiplexer functions implemented in the RISC/DSP.



# Encoder Core Modules

The VW2010 encoder core consists of the following modules:

- Motion estimation unit (MEU)
- Motion vector refinement unit (MRU)
- Chroma compensation unit (CCU)
- Mode select unit (MSU)
- Video encoder unit (VEU)
- Encoder processor unit (eCPU)
- Rate control unit (RCU)

### Motion Estimation Unit (MEU)

The MEU estimates the distance that a macroblock has moved relative to the reference frame, for the luma component of the video data. The MEU uses a proprietary search scheme, which reduces the computational complexity of calculating the motion vectors. A coarse estimate of the motion vectors is calculated within the search window. The best-matched frame and field motion vectors and vertical field-select bits are sent to the MRU. Table 2 on page 21 shows the maximum search windows. The search range is programmable in 16-pixel steps.

**Table 2 Maximum Search Range Table**

| | Frame Prediction | Field Prediction |
|---|---|---|
| P-Picture | Horizontal: ± 127 pels<br>Vertical: ± 63 pels | Horizontal: ± 127 pels<br>Vertical: ± 63 pels |
| B-Picture | Horizontal: ± 63 pels<br>Vertical: ± 63 pels | Horizontal: ± 63 pels<br>Vertical: ± 63 pels |

### Motion Vector Refinement Unit (MRU)

The MRU takes the output of the MEU and applies a "fine search refinement scheme" to fine-tune the luma motion vectors to within one-half pel. The MRU initiates a second search around the origin of the coarse motion estimation block calculated by the MEU.

### Chroma Compensation Unit (CCU)

The CCU takes the refined motion vectors from the MRU (for the luma component), and uses them to perform motion compensation on the chroma component.

### Mode Select Unit (MSU)

The MSU performs macroblock inter/intra DCT decision and activity measure calculations required by the RCU. It performs the following calculations:

- Squared error of the best prediction
- Variance of the currently coded macroblock
- Activity measure of the current coded macroblock
- Parameters for field- or frame- DCT decisions

### Video Encoder Unit (VEU)

The VEU actually performs the video compression. Based on the MSU calculations, unless overridden by the host processor, the VEU performs field or frame-based DCT calculations. The DCT coefficients are quantized, zig-zag-scanned and VLC-coded. The VEU performs the inverse quantization (IQ) and inverse DCT (IDCT) calculations to generate the reconstructed image that is used in the motion vector calculations. In sum, the VEU performs the following tasks:

- Download the user-defined quantization matrix for MPEG-2 quantization
- MPEG-1, -2, -4 quantization / inverse quantization
- Frame/field forward DCT / inverse DCT
- Coded block pattern generation
- DC/AC prediction in MPEG-4
- Motion-vector prediction and coding

- MPEG-1, -2, -4 variable length coding (VLC)
- Reconstruction of macroblocks
- Distortion measurements between original and reconstructed macroblocks
- Keeping track of the number of bits generated

### Encoder Processor Unit (eCPU)

The eCPU is implemented using a proprietary RISC processor with up to 4K x 20 bits of microcode. The eCPU controls the operations of the encoder. It sequences the input video data through the compression process up to the ES output, places the MPEG video headers on the data, monitors the status of the various modules, and controls the output of the data. The Vweb Corporation provides the microcode in binary format.

### Rate Control Unit (RCU)

The RCU is implemented using a proprietary RISC processor with up to 4K x 24 bits of microcode. Different parts of the rate control algorithms are invoked by signals from the eCPU and VEU at various points during the encoding process. The RCU calculates sixty variables, which it uses to manage the encoded bit rate and bit budget. The Vweb Corporation provides the microcode in binary format.

## Output Modules

The VW2010 encoder has one output module:

- Encoder multiplexer unit (MUX)

and two output ports:

- Multiplexer compressed data out (CDO) port
- Host / PCI port

### Multiplexer (MUX)

The MUX provides user control of the compressed data output (CDO) buffers and FIFOs for routing the combined / multiplexed CDO bitstream from the RISC (that is, from the encoder SDRAM after the RISC has finished its work on the bitstream) to the host/PCI port or to the CDO port. If the destination is the CDO port, the MUX can generate either an 8-bit parallel or a 1-bit serial CDO bitstream.

#### *Encoder Buffers*

In the encoder, the multiplexer (MUX) also acts as a buffer controller (BUF). The multiplexer (under control of the RISC) sets up eight buffers in SDRAM for transport multiplexing; that is, combining video, audio and user data to create the CDO, and to route data into and out of the encoder. The buffers in SDRAM, and the corresponding buffers set up by the RISC in dmem, are listed in Table 3 on page 23.

*Note:* The role of these buffers in DMA transfers is shown under "DMA Controller" on page 46.

**Table 3 Buffers in Encoder SDRAM and dmem [1]**

| Encoder SDRAM | I/O | dmem |
|---|---|---|
| Video | Out | |
| User | In | User |
| VBI | In | |
| Mux (out) | Out | Mux |
| Audio1 | In | Audio1 |
| Audio2 | In | Audio2 |
| Audio3 | Out | |
| Audio4 | Out | |

1. The buffer sizes are set by Vweb firmware and may vary with each release.

***Data Paths via the Buffers***

The data paths, in terms of the A/V buffers, are shown in Figure 6 on page 23. Note that there is a 1:1 correspondence between a PID and the buffer for the data type identified by the PID.



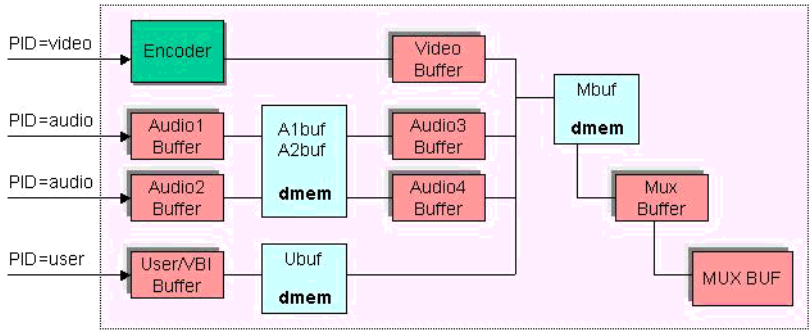


**Figure 6 Data Paths through the Multiplexer Buffers**

As Figure 6 on page 23 shows, the RISC/DSP takes uncompressed data from two audio input buffers to generate compressed audio:

- Audio 1 buffer
- Audio 2 buffer

The results are stored in a second set of two audio buffers (audio 3 and 4). Under control by the RISC, the MUX gets the components of the CDO bitstream from up to five sets of FIFOs and buffers (depending on the video/audio/user data actually being encoded):

- Video buffer
- Audio 3 buffer
- Audio 4 buffer
- VBI buffer
- User data buffer

Data in the video buffer is the output of the video encoder core modules. There is no user data / VBI output buffer, as user data can multiplexed into the compressed video stream from the encoder core at the TS, PES or picture level. The resulting multiplexed, compressed data is stored in an eighth buffer:

- Mux buffer

The MUX gets the compressed data from this buffer for routing it as a CDO stream to the CDO port.

### External Buffer Control

CDO is pumped out to an external device in the host, typically a system FIFO under the control of a system FIFO controller. The interface is summarized in Figure 7 on page 24.

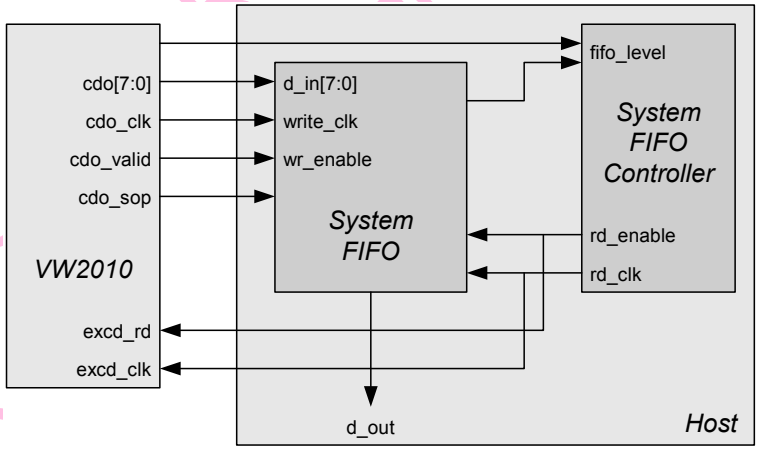


**Figure 7 External FIFO Interface**

Compressed data is pumped out the CDO port cdo[7:0] at the rate set by cdo-clk when the chip indicates that the CDO data is valid. The fifo_level signal from the chip as an interrupt to the system FIFO controller when the chip's output FIFO is half full.

The host can control the CDO data rate, by sending excd_rd to inform the chip about the external FIFO level, and by sending excd_clk to latch excd_rd. Using this information, Vweb firmware adjusts the CDO burst size to match the output data rate of the

system FIFO. The fifo_level signal from the system FIFO as an interrupt to the system FIFO controller when the system FIFO reaches a user-defined value.

## CDO Port

The CDO port is part of the MUX. The external interface signals are listed under "Multiplexer Interface" on page 66.

### *CDO Modes*

The CDO port runs in two modes:

- VW2000 mode, bursting data out at sysclk/4 = 40.5 MHz
- ASI mode, clocking data out in 188-byte packets at 27, 13.5 or 6.75 MHz.

In VW2000 legacy mode, the interface consists of six signals shown in Figure 7 (cdo[7:0], cdo_clk, cdo_valid, excd_rd, exd_clk, fifo_level). Strictly speaking, excd_rd and excd_clk are not needed; in such a case, of course, there is no data rate adjustment.

In ASI mode, the interface consists of the five VW2010 output signals (cdo[7:0], cdo_clk, cdo_valid, cdo_sop, fifo_level). The burst size is fixed, always 188 bytes. The cdo_sop signal can go to a FIFO as shown in Figure 7, or, more typically, to a DVB-ASI encoder chip as shown in the Vweb win10 schematic.

### *CDO Streams*

The CDO bus is used to output a transport stream (TS). However, it can also be programmed to output ES, PES, video ES, audio ES, video PES, audio PES.

When outputting TS, PCR is inserted automatically. If the PCR PID is the same as the video PID, then the PCR is inserted into the video packet, and the PCR_Present bit is set in the TS header. If the PCR PID is different from the video PID, then a PCR packet is generated exclusively.

When outputting TS, PAT and PMT are also generated automatically and inserted into the TS. The interval is programmable; the default is the industry standard for DVB, 600 ms.

## Host / PCI Port

For a detailed description, see "System Modules" on page 39 and "System Interface Signals" on page 75.

The host/PCI port can be used to input and output CDO streams, download microcode into the VW2010 device, program the graphics plane, as well as other data.



# Application Notes

The VW2010 encoder connects directly, seemlessly, without glue logic, to a video decoder such as the Philips SAA7115 and to an audio ADC such as the Philips UDA1342 CODEC, as illustrated in the following figure (based on the schematic of the VwebWin10 Evaluation Board).

The video decoder and audio ADC have their own requirements for input signal filtering and input power smoothing, and in the case of the Philips video decoder, requires an external 32.11 MHz oscillator. These requirements are explained in the Philips data sheets.

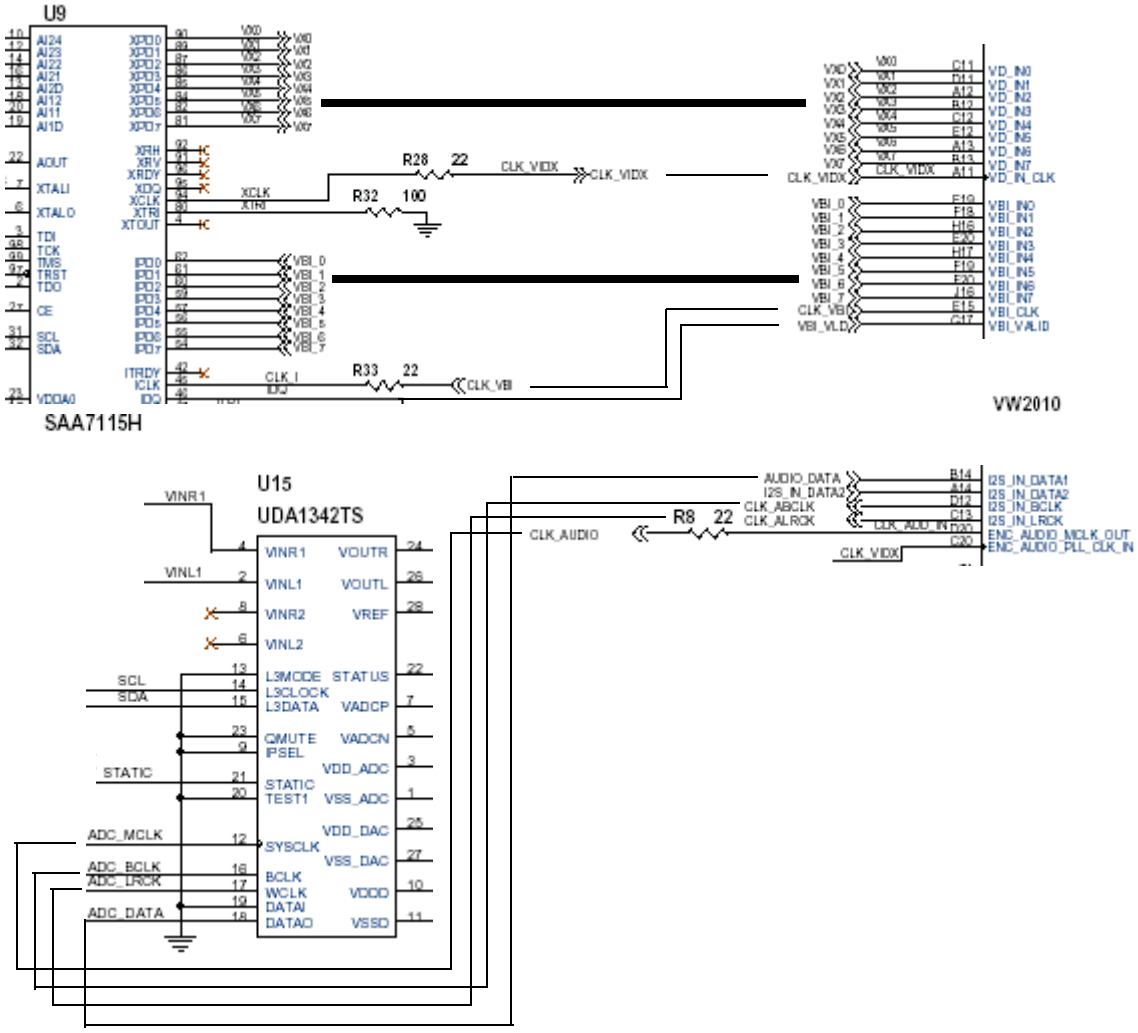


**Figure 8 Connections between the MPEG Encoder, Video Decoder and Audio ADC**

# CHAPTER 4 Decoder Modules

This chapter presents more detailed descriptions of each individual VW2010 decoder module's functions. Figure 9 on page 29 summarizes all the modules that constitute the VW2010, and their relationships to each other. The bottom row of modules belong to the decoder.



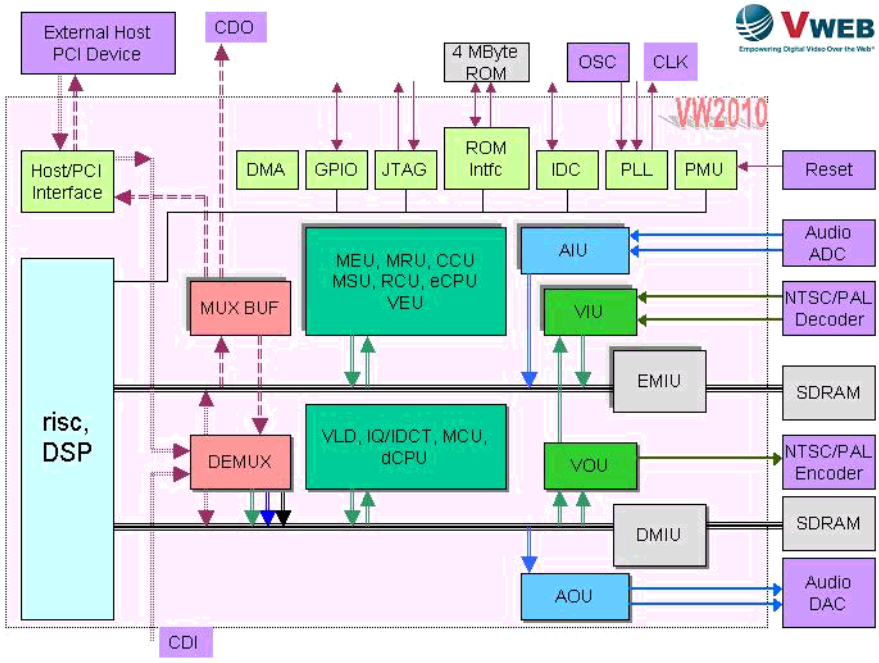


**Figure 9 Modules of the VW2010**

# Input Modules

The VW2010 has two input modules:

- Decoder demultiplexer (DEMUX)
- Host interface unit (HIU)

and two input ports:

- Demultiplexer compressed data in (CDI) port
- Host / PCI port

## Demultiplexer (DEMUX)

The DEMUX provides user control of buffers and FIFOs used in demultiplexing the compressed data input (CDI) bitstream, and for routing the resulting video and audio streams to the video and audio output ports, or to the host/PCI port. The DEMUX accepts CDI either from the CDI port or from the host/PCI port. In either case, there is a bypass in the DEMUX unit to store the incoming data either in encoder SDRAM or in decoder SDRAM. If the active input is the CDI port, the DEMUX can process either an 8-bit parallel or a 1-bit serial CDI bitstream.

### *Decoder Buffers*

In the decoder, the DEMUX acts as a buffer controller. The DEMUX (under control by the RISC) sets up eight buffers in SDRAM for transport demultiplexing; that is, separating video, audio and user data from the CDI. The buffers in SDRAM, and the corresponding buffers set up by the RISC in dmem, are listed in Table 4 on page 30.

*Note:* The role of these buffers in DMA transfers is shown under "DMA Controller" on page 46.

**Table 4 Buffers in Decoder SDRAM and dmem [1]**

| Decoder SDRAM | I/O | dmem |
|---|---|---|
| Video | In | |
| Demux | In | |
| PSI | In | PSI |
| User | In | User |
| Audio1 | In | Audio1 |
| Audio2 | In | Audio2 |
| Audio3 | Out | |
| Audio4 | Out | |

1. The buffer sizes are set by Vweb firmware and may vary with each release.

There is no output buffer for video/demodulator and user data, as video/demodulator data is an output streamed by the decoder core modules directly to a video encoder, and

user/VBI data can be output directly either to the internal graphics module or streamed out on the ICI port.

### Data Paths via the Buffers

The data paths, in terms of the A/V buffers, are shown in Figure 10 on page 31. Note that there is a 1:1 correspondence between a PID and the buffer for the data type identified by the PID.

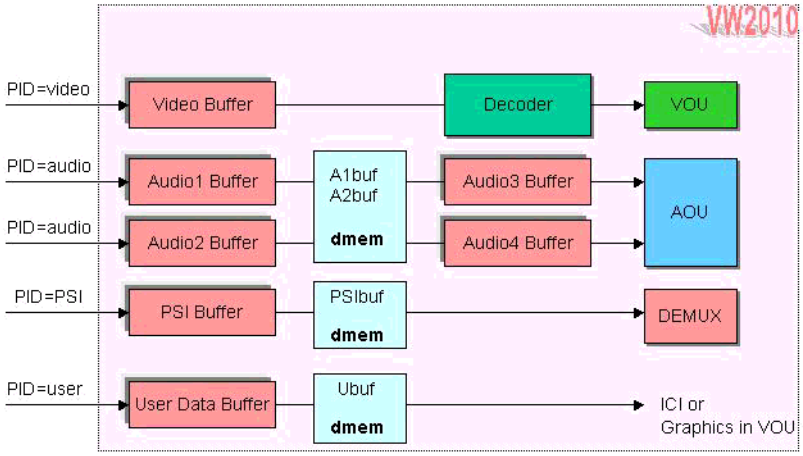


**Figure 10 Data Paths through the Demultiplexer Buffers**

As Figure 10 on page 31 shows, under control by the RISC the DEMUX stores the components of the CDI bitstream in up to five sets of FIFOs and buffers (depending on the contents of the CDI bitstream):

- Video buffer
- Audio 1 buffer
- Audio 2 buffer
- PSI buffer
- User data buffer

Data from the video buffer is processed through the video decoder core modules. The user/VBI data may be routed to the graphics module in the VOU, or output to an external device on the ICI port. PSI data is processed in the DEMUX. The RISC/DSP takes data from the two audio buffers to generate uncompressed audio. The results are stored in a second set of two audio buffers:

- Audio 3 buffer
- Audio 4 buffer

Data from audio 3 and 4 are used by the audio output unit (AOU) to generate its outputs.

### CDI Port

The CDI port is part of the DEMUX. The external interface signals are listed under "Demultiplexer Interface" on page 70.

### Host / PCI Port

For a detailed description, see "System Modules" on page 39 and "System Interface Signals" on page 75.

## Decoder Core Modules

The VW2010 decoder core consists of the following modules:

- Variable length decoding unit (VLD)
- Inverse quantization / inverse DCT unit (IQ/IDCT)
- Motion compensatio unit (MCU)
- Decoder processor unit (dCPU)

The decoder can handle MPEG-1 and MPEG-2 I, P and B pictures, and MPEG-4 I-VOP and P-VOP.

### Decoder Processor Unit (dCPU)

The dCPU is implemented using a proprietary RISC processor with up to 4K x 20 bits of microcode. The dCPU controls the operations of the decoder. It sequences the input compressed data through the decompression process up to the VOU input, removes the MPEG video headers on the data, monitors the status of the various modules, and controls the output of the data. The Vweb Corporation provides the microcode in binary format.

The dCPU generates motion vectors and decodes the following video layers:

- Sequence headers
- Group of pictures
- Picture
- Slice
- Macroblock
- Block

### Variable Length Decoding Unit (VLD)

The VLD unit performs the following functions to start the decoding process:

- Variable-length decoding
- Inverse scan

The VLD uses variable-length decoding to recover the DC and AC coefficients for intra-coded blocks, and DC coefficients for non-intra-coded blocks. From these coefficients the VLD computes a set of predictors for each of the three color components.

Then the VLD uses inverse scan to convert the one-dimensional matrix of predictors into the two-dimensional matrix of coefficients required by the IQ/IDCT unit.

For further details, see the MPEG specification ISO/IEC 13818-2, Clause 7, section 7.3.

### Inverse Quantization / Inverse DCT Unit (IQ/IDCT)

The IQ/IDCT unit performs field- or frame-based inverse quantization (IQ) to produce the reconstructed DCT coefficients. Then it performs inverse discrete cosine transform calculations (IDCT) to obtain the inverse transform values, which are needed in the MCU to generate the reconstructed image.

For further details, see the MPEG specification ISO/IEC 13818-2, Clause 7, section 7.4 and 7.5.

### Motion Compensation Unit (MCU)

The MCU recreates (reconstructs) pixels based on the data from the IQ/IDCT unit. The MCU takes the decoded motion vectors from the dCPU, and translates them into row and column coordinates. The MCU supports frame and field motion vector types, and implements the following prediction modes:

- Frame prediction mode
- Field prediction mode
- Field prediction mode with 16x8 motion compensation and forward/backward/bi-directional motion vectors.

The MCU is accurate to 1/2 pel and it limits the saturation value of the final reconstructed pixel to between 0 and 255.

For further details, see the MPEG specification ISO/IEC 13818-2, Clause 7, section 7.6.

## Output Modules

The VW2010 has two output modules:

- Video output unit (VOU)
- Audio output unit (AOU)

### Video Output Unit (VOU)

The VOU includes post-processing filters, mixers and display control timing. The VOU outputs 4:2:2 compatible data in ITU-R.BT.656 format. Under the control of the RISC, user data is converted to Closed Caption or Teletext, and is inserted into the VBI.

The VOU also manages up to five graphics planes, which can be superimposed onto each other before converting the data to ITU.R-BT.656 format. If the resultant image does not fit within the constraints of the ITU.R-BT.656, then the resultant image will be cut off at the boundary points. The five graphics planes are shown in Figure 11 on page 34.

#### *Background Color Plane*

The background plane allows for the padding of a 24-bit YCbCr color around the MPEG display. Alpha blending is not enabled, therefore the background cannot be blended with the MPEG video.

#### *MPEG Display Plane*

The MPEG display plane converts the 4:2:0 data to the 4:2:2 output format. It provides support for pan and scan, ½ and ¼ decimation, up to 8x interpolation, and windowing.

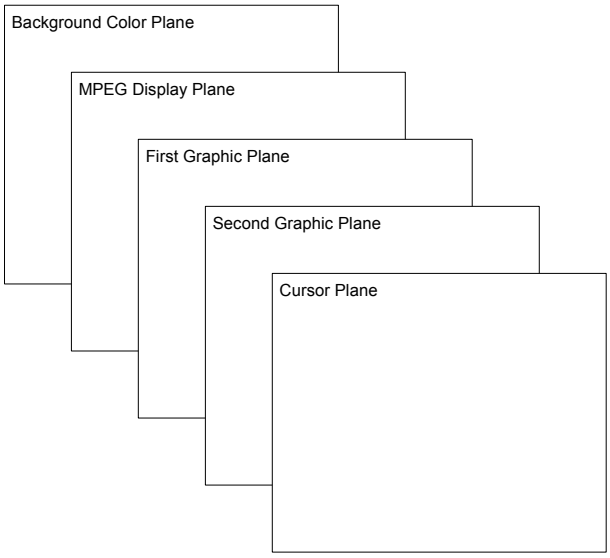


**Figure 11 Graphics Plane Hierarchy**

***Graphics Planes***

The two graphics planes are identical except for their ordering with respect to alpha blending. Both planes accept graphics input and allow for the following features:

- 2-, 4-,8- and 24-bit color look-up tables (CLUT)
- Each graphics plane can have its own separate CLUT
- 32-bit ARGB and AYCbCr (alpha-blended RGB and YCbCr):
  - 8 bits alpha (256 levels of transparency)
  - 8 bits Y or R
  - 8 bits Cb or G
  - 8 b its Cr or B
- All input formats are stored in 4:4:4 chroma format in separate fields
- Each CLUT entry uses 32-bit wide ARGB or AYCbCr
- Multiple regions can exist within the graphics plane; however, the regions cannot overlap and two regions cannot be programmed on the same line.

***Cursor Plane***

The cursor plane supports five programmable dimensions for the cursor:

- 8x128 pixels
- 16x64 pixels
- 32x32 pixels
- 64x16 pixels
- 128x8 pixels

The cursor can be placed anywhere on the entire screen. It uses four bits per pixel (16-colors) and a transparency factor.

***Alpha Blending***

The various graphics planes are mixed according to the blending scheme shown in Figure 12 on page 35.

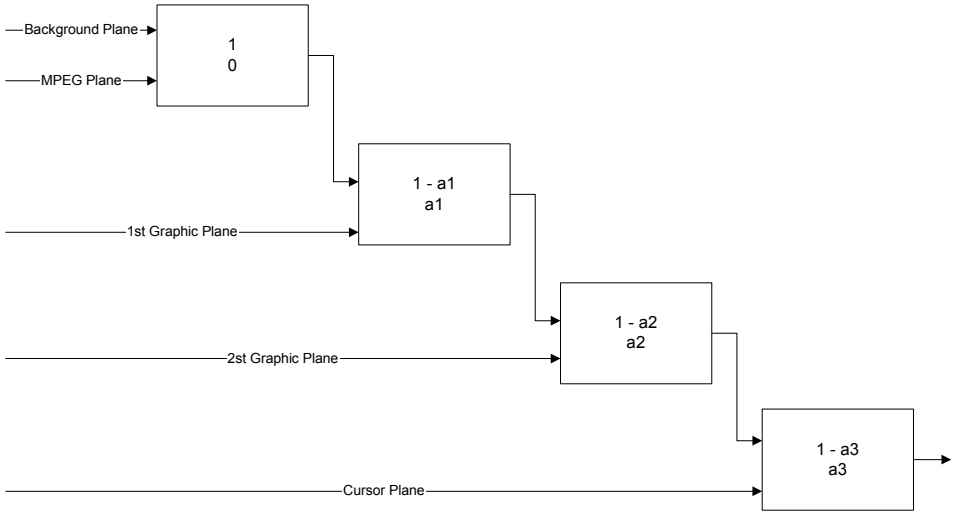


**Figure 12 Alpha-Blending Hierarchy**

***Anti-flickering***

The VW2010 performs anti-flickering by using the two graphics planes in concert. The two planes must be programmed with the same configuration. A two-tap vertical filter is used to filter one line from each of the graphics planes. Three sets of coefficients are provided:

- {¼, ¾}
- {¾, ¼}
- {½, ½}

These three sets of coefficients represent the relative weightings of lines from each of the two graphics planes used in anti-flickering. The three sets of coefficients make possible three different anti-flicker schemes to be implemented using the two graphics planes, depending on the choice of the coefficients (1/4, 1/2 or 3/4) that can be applied to the starting line in the process. After that, the pairs of coefficients applied to subsequent lines are alternated. For example, the first line from plane 1 with coefficient 1/4 is combined with the first line from plane 2 with coefficient 3/4 to produce the first line of filtered output. To generate the second line of output, 3/4 is applied to the second line from plane 1 and 1/4 to the second line from plane 2.

***On-Screen Display (OSD)***

The VOU includes two OSD engines, OSD_0 and OSD_1. Both can write user data to the two graphics planes described above. User data is written to an OSD engine by means of a PCI, Motorola or Intel interface described in "Host / PCI Interface" on page 41, using the signals decribed in "System Interface Signals" on page 75.

The operation of the OSD engine is described in the Vweb VW2010 Programmer's Reference Manual.

### Audio Output Unit (AOU)

The AOU supports two independent output ports, $I^2S$ and S/P-DIF, of digital audio data output. Both ports support linear PCM audio data output. In addition, on the S/P-DIF port, the output data can be presented either as 2-channel uncompressed data using IEC-958, or as compressed non-linear PCM-encoded audio bit-stream data using IEC-61937 formatting (compressed audio bypass). The IEC-61937 bypass is set up under register control. The AOU generates its own audio timing signals from a single audio master input clock of either 24.576MHz or 16.9344MHz and PLL locked to the decoder video master clock.

The AOU supports the audio sampling frequencies (sampling rates from 8 KHz to 96 KHz) and the bits-per-channel, left/right modes (from 16 to 32 bits) shown in the "Feature List" on page 11. To this end, the audio PLL can generate the audio master clock frequencies shown in Table 7 on page 52.

The AOU also supports user-controlled data pause. During data pause, the output channel continues to send out the last left/right samples prior to the pause state. After the pause state has been cancelled, the audio data resumes its normal operation.

## Application Notes

The VW2010 decoder connects directly, seemlessly, without glue logic, to a video encoder such as the Philips SAA7120, and to an audio DAC such as the Cirrus CS4331, as illustrated in the following figure (based on the schematic of the VwebWin10 Evaluation Board).

The video encoder and audio DAC have their own requirements for input signal filtering and input power smoothing. These requirements are explained in the vendor's data sheets.

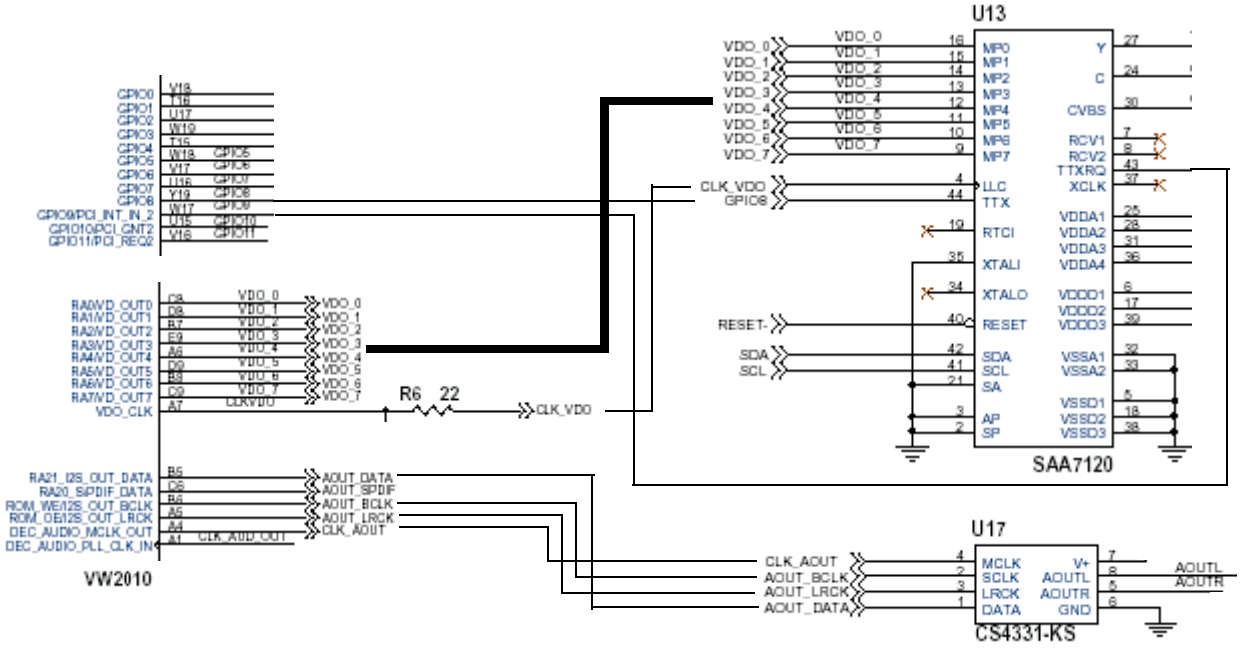


**Figure 13 Connections between the MPEG Decoder, Video Encoder and Audio DAC**

# CHAPTER 5 System Modules

This chapter presents more detailed descriptions of each individual system module's functions. Figure 14 on page 39 summarizes all the modules that constitute the VW2010, and their relationships to each other. The top row of modules (DMA ... PMU) plus the HIU, the RISC, the EMIU, and the DMIU perform system-level functions for the chip.



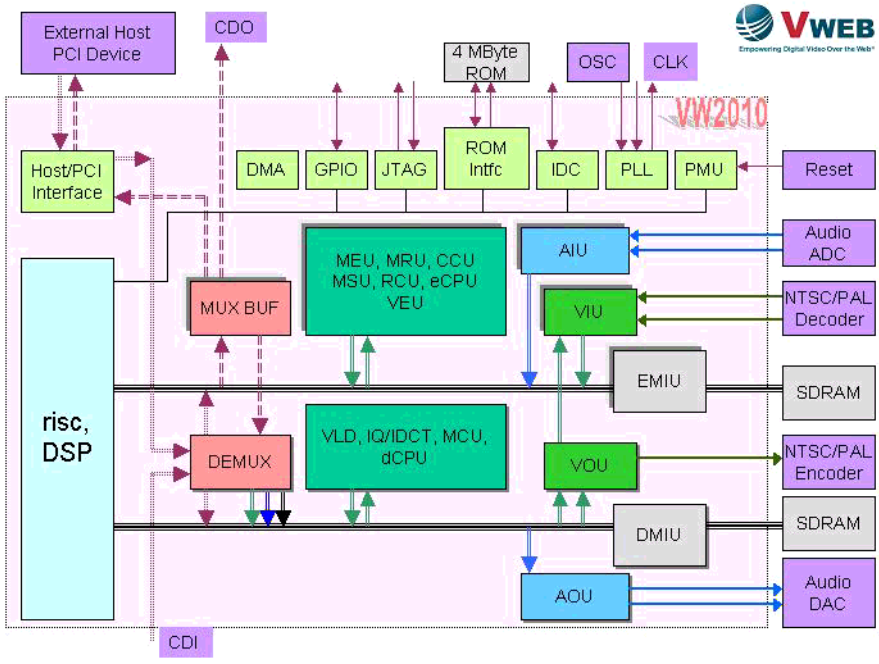


**Figure 14 Modules of the VW2010**

# Embedded Processor (RISC/DSP)

The embedded processor is a RISC-like RISC engine with extensions to function as an audio DSP. The RISC/DSP implements various functions, including overall control of the VW2010, as well as audio encoding, A/V multiplexing, A/V demultiplexing, and audio decoding.

## RISC Multiplexer

The RISC multiplexer works with the MUX and performs the following tasks:

- Combines the compressed audio, video and user data.
- Generates MPEG-1 system streams, MPEG-2 program streams, or MPEG-2 transport streams (TS, PS, SS or PES bitstreams) suitable for use as input to an off-chip decoder device.

The data can be presented as one of the following:

- MPEG transport stream
- System or program stream
- Independent MPEG elementary streams

## RISC Audio Encoder

The RISC/DSP audio encoder compresses the audio signal by calculating a transform and applying a psychoacoustic model to estimate the noticeable noise level. Then it quantizes and codes the audio data in a way to meet both the bit-rate and the masking requirements. The audio encoder supports the formats shown in the "Feature List" on page 11.

The audio encoder presents the data to the multiplexer (in the RISC/DSP), where the audio data is multiplexed with video and user data, or processed for network delivery.

## RISC Demultiplexer

The RISC demultiplexer works with the DEMUX and performs the following tasks:

- The RISC processor separates the audio, video, and user data, and places them into separate FIFOs set up and configured by the DEMUX.
- The RISC processor extracts the other program identifiers (PIDs) into separate FIFOs set up and configured by the DEMUX.

## RISC Audio Decoder

The RISC/DSP audio decoder reconstructs the audio by performing an inverse quantization. The audio decoder supports the same formats as the encoder. The audio encoder presents the decompressed audio data to the audio output unit (AOU).

## Data Cache (dmem)

The dmem data cache is an active working memory of the RISC. Parts of dmem are dynamically assigned, as needed, as temporary buffers used by the RISC. This is shown in Figure 17 on page 48.

The section titled "DMA Controller" on page 46 explains the role of dmem in DMA transfers. For additional details see also the sections titled "Multiplexer (MUX)" on page 22, and "Demultiplexer (DEMUX)" on page 30.

# Memory Interfaces

The VW2010 has two SDRAM interfaces; one for the encoder (EMIU), one for the decoder (DMIU). Each SDRAM interface performs the following functions:

- Provides all required signals to control an external memory device (two 1Mx16, or one 2Mx32).
- Includes a 32-bit data bus and 11-bit row and column address bus operating at 162 MHz.
- Acts as the memory access bandwidth arbitrator among the various modules.
- Supports the following style of 16-bit or 32-bit wide SDRAM parts on the market:
  - 200 MHz (or 5 ns)
  - CAS latency of 3-cycles
  - 11 bits for row and column addressing with up to 2 bank select bits
  - Micron-style power-up sequence

### Encoder Memory Interface Unit (EMIU)

The EMIU performs the functions listed above to control the 4 or 8 Mbytes of SDRAM needed to compress the video images.

### Decoder Memory Interface Unit (DMIU)

The DMIU performs the functions listed above to control the 4 or 8 Mbytes of SDRAM needed to uncompress the video images.



# Host / PCI Interface

### Architecture

The host/PCI interface consists of two internal modules, HIU and PCI. The HIU is a 16-bit core that allows glueless connection to a 16-bit Motorola 68K or Intel x86 type device or host bus; the HIU can be configured to run in one of these host modes. The PCI is a 32-bit 33 MHz core that supports the PCI Local Bus Specification version 2.2. The HIU and PCI both access the outside world via one set of shared pins; that is, the VW2010 can use either the HIU or the PCI interface, but not both at the same time. Therefore, the PCI interface appears as just another host mode (see "Host Interface Modes" on page 3; see also Figure 29 on page 76).

The host/PCI interface is accessible from an external host or PCI device, as well as from the main RISC processor embedded in the VW2010. Internally, specific hosts (Motorola, Intel, PCI, and the main RISC embedded in the chip) appear simply as I/O devices sharing the same address bus and data bus into the HIU core module.

The host interface mode - that is, how the host/PCI interface is configured for external access - is selected as described in "Host Mode" on page 49.

### Applications

The versatility of the VW2010 host/PCI interface allows a variety of applications:

- In an embedded design, the VW2010 can access off-chip devices through the host/PCI interface.

- In a host-based design, the host/PCI interface connects the VW2010 to a standard PCI bus; that is, to the host motherboard and other plug-in cards.
- In stand-alone designs, the host/PCI interface allows glueless connection to a standard Motorola or Intel device, as well as to a ROM device. In this mode, the external host processor can communicate with the VW2010 using the appropriate HIU host mode running at a clock speed up to 30 MHz.

## Functions

The host/PCI interface allows access to the internal hardware registers in the VW2010, as well as to the encoder SDRAM and the decoder SDRAM. The host/PCI interface includes an interrupt controller that manages interrupts from the individual modules, A/V buffers and FIFOs in the chip, and allows the external host to determine the source of the interrupt. The host/PCI interface allows the external host to soft-reset individual modules in the encoder, the decoder, as well as the main RISC processor. The host/PCI interface responds to and facilitates DMA requests. And the host/PCI interface includes a set of internal registers that hold the parameters for the A/V capture and encoding process, as well as the control bits to start and stop the encoder and decoder.

The host/PCI interface is the controller and the conduit for different kinds of data that could appear on the host/PCI bus:

- Encoder and decoder parameters, such as quantization matrix, filter coefficients, etc.; encoder and decoder control signals
- Microcode for the main RISC, the encoder CPU and RCU, and decoder CPU
- Compressed A/V bitstream (CDI, CDO) in SS, TS, PS, ES or PES formats
- User data, VBI data

## Data Paths

The host/PCI interface sets up (can be set up to provide) the following data paths in either host or PCI mode:

- CDO write
- CDI read
- SDRAM read/write
- Register read/write
- Microcode download
- Boot-time download paths
- Soft reset

The following sections describe the physical data paths in each case. The actual implementation is set up and executed by means of the internal HIU registers, and is the topic for the VW2010 Register Specifications and the VW2010 Programmer's Reference manuals.

### *CDO Write*

Compressed, encoded data can be saved out the host/PCI interface, and written to external host memory or other storage device. The source of the data can be the A/V buffers (which are set up in encoder SDRAM), in which case registers are used to set up the buffer and FIFO watermarks and other controls. The source of the data can also be the encoder or decoder SDRAM in general (not restricted to A/V data).

The data path is shown in the following figure. CDO is passed from SDRAM, to the MIU, to the DMA controller / DMA FIFO, and to the HIU.

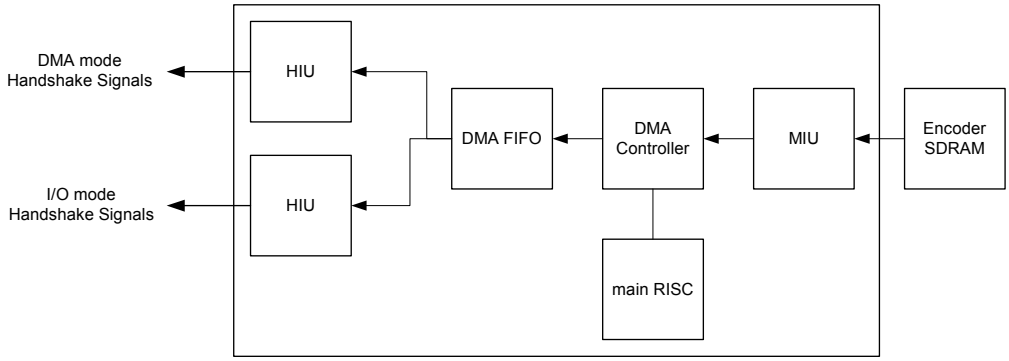


**Figure 15 CDO Data Path via the HIU**

The figure above is slightly misleading in the sense that there is only one HIU, but it can be set up in two modes, DMA or I/O. The main RISC microcode sets up the DMA transfer. The host sets up I/O read mode.

In DMA mode, the interface signals are the following:

- host_hiu_cdo_req (out); the chip has data ready to send
- hiu_host_cdo_ack (in); the host has received a line of data
- host data bus (out)
- hiu_host_dtack (out); the chip has sent all the data it had; the current cycle has finished.

In DMA mode, the chip sends the next line of data as soon as it sees cdo_ack from the host; it does not send another cdo_req.

In host I/O read mode, the interface signals are the following:

- host_hiu_cdo_req (out)
- host_hiu_cs (in)
- host_hiu_as (in)
- host data bus (out)
- host address bus
- hiu_host_dtack (out)
- host_hiu_rw (in)

In host mode the full handshake protocol is set up and executed for every byte of data.

These handshake signals are described in the chapter titled "System Interface Signals" on page 75, and the interface timing signals are shown in "Electrical Characteristics" on page 147.

### CDI Read

Compressed, encoded data can be captured from external host memory or other storage device via the host/PCI interface, and written to the decoder SDRAM. The desti-

nation of the data can be the A/V buffers (which are set up in decoder SDRAM), in which case registers are used to set up the buffer and FIFO watermarks and other controls. The destination of the data can also be the encoder or decoder SDRAM in general (not restricted to A/V data).

The data path is shown in the following figure. CDI is passed from the HIU, to the DMUX FIFO, to the DMIU, and to the SDRAM.

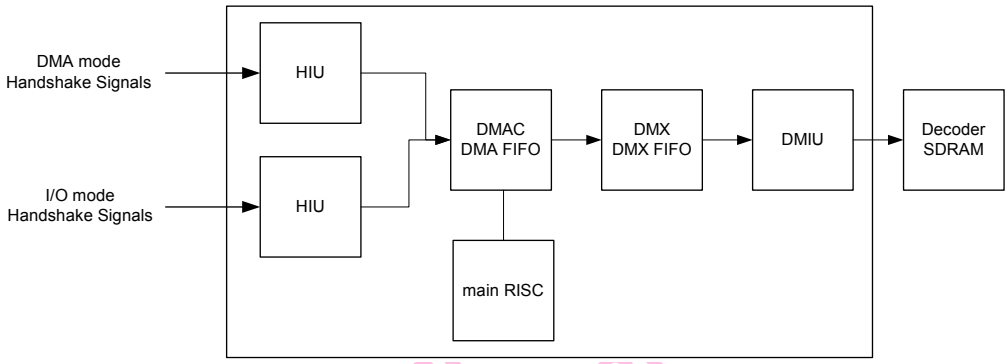


**Figure 16 CDI Data Path via the HIU**

The figure above is slightly misleading in the sense that there is only one HIU, but it can be set up in two modes, DMA or I/O. The main RISC microcode sets up the DMA transfer. The host sets up I/O read mode.

In DMA mode, the interface signals are the following:

- host_hiu_cdi_req (out); the chip is ready to receive data
- hiu_host_cdi_ack (in); the host is ready to send data
- host data bus (out)
- hiu_host_dtack (out); the chip has received all the data it can handle; the current cycle has finished.

In DMA mode the chip accepts data as fast as the host can send it.

In host I/O read mode, the interface signals are the following:

- host_hiu_cdi_req (out)
- host_hiu_cs (in)
- host_hiu_as (in)
- host data bus (in)
- host address bus
- hiu_host_dtack (out)
- host_hiu_rw (in)

In host mode the full handshake protocol is set up and executed for every byte of data.

These handshake signals are described in the chapter titled "System Interface Signals" on page 75, and the interface timing signals are shown in "Electrical Characteristics" on page 147.

***SDRAM Read/Write***

The data path for SDRAM access is as shown in the figures above. The HIU can access encoder SDRAM after the SDRAM has been initialized by the VW2010, which is about 12000 clock cycles after reset or power-up. Data between the HIU and SDRAM is passed via a set of HIU registers, with appropriate adjustments for the 16-bit register widths, and the 32 bits for data and 20 bits for address.

SDRAM addressing through the HIU is word-aligned; that is, 32 bits wide. For example, by putting 0x0001 on host_hiu_data, the host is trying to access physical SDRAM location 0x0004.

The HIU can also access the decoder SDRAM, but through a different set of registers. In addition, decoder SDRAM is 64 bits wide and is addressed by 24 bits. Therefore, the 16-bit registers must be used in the appropriate combinations to accommodate these bus widths.

***Register Read/Write***

The HIU provides an I/O path to the chip's internal hardware registers. The HIU gains access by issuing a register_read or register_write command. An HIU command consists of two parts, the HIU command code (such as read or write) and the register address. The HIU can access those registers that are shown in the VW2010 Register Specifications with the legend "Access: Host R/W." The register addresses are also shown in that manual. Th HIU commands are described in the VW2010 Programmer's Reference Manual.

***Soft Reset***

The HIU allows an external host to reset individual modules in the chip, either by hardware reset at power up, or by software at any time ("soft-reset"). Soft-reset is implemented by means of a reset register for the encoder modules and another reset register for the decoder modules.

***Microcode Download***

The HIU provides a path to download microcode into the encoder CPU, decoder CPU, and the main RISC. Microcode download is similar to register access and SDRAM access: it requires an HIU command (of the form, load_[target_module]_microcode and microcode_download_done), and the HIU must accommodate the differences between the instruction lengths (24 bits for the RCU, 20 bits for the eCPU and the dCPU), the data-in bus width (16 bits), and the widths of the internal registers (16 bits).

The microcode download is a module-specific multi-step process, and is described in the VW2010 Programmer's Reference Manual.

***Boot-time Download Paths***

The VW2010 supports three boot modes:

- Boot from ROM
- Boot from ICI
- Boot from host

In all three cases, microcode for the main RISC, the encoder CPU and the decoder CPU is loaded into decoder SDRAM.

***Boot from ROM -*** When this option is used, all microcode should reside in external ROM. After reset is removed from the chip, all modules need to be initialized. At this time the main RISC performs a hardware jump to a location that is mapped to the ROM area. The code inside the ROM must include a small bootstrap program that will copy a code image into decoder SDRAM, then perform a jump to the beginning of the code image. This code image will be responsible for the rest of the encoder and decoder initalization. This mode is used in stand-alone applications.

***Boot from ICI -*** When this option is used, a bootstrap loader resides in an SEEPROM. Since the SEEPROM is small (128 bytes), the rest of the microcode must be downloaded through the HIU. Therefore, this option is not used in stand-alone applications.

***Boot from host -*** When this mode is used, all microcode is downloaded through the HIU. There is no need for either ROM or SEEPROM in the system.

In this mode, the external host is responsible for the downloading procedure. Once all of the microcode is download and all of the modules are being initalized, the external host can start the encoder, decoder and the main RISC.

# DMA Controller

## DMA Features

The DMA controller in the VW2010 chip transfers blocks of data, independent of the embedded main RISC processor or the external PCI host. Data is moved on the host/PCI interface port and the internal encoder or decoder SDRAM buses shown in Figure 2 on page 5. The following is a summary of DMA features:

- The DMA engine uses two DMA channels, 0 and 1. The two DMA channels operate completely independently from each other.
- The DMA engine operates by executing link lists. It can execute up to eight link lists, 0-7. Each link list consists of any number of descriptors. Each descriptor consists of four consecutive 4-byte (32-bit) fields that specify transfer parameters. Each link list has a specific starting address.
  Link lists and descriptors are described in the Vweb VW2010 Programmer's Reference Manual.
- The DMA transfer size is 1024 bytes per descriptor in a link list. The total amount of data per DMA transfer is the buffer size or available memory (depending on the source of data for the transfer). The DMA will flush any remaining data, even if less than the 1KB transfer size, using the last descriptor in the link list.
- The DMA engine is controlled by eight identical sets of registers; one set per link list.
  The DMA registers are described in the Vweb VW2010 Register Specifications.
- The DMA engine can operate in direct or in chaining (scatter/gather) mode.

- The DMA engine supports word-aligned (32-bit aligned) transfers only.
- The DMA arbiter manages the DMA channels, link lists and descriptors in a round-robin / time-multiplexed fashion. The DMA arbiter is implemented fully in hardware, with no microcode overhead.
  The operation of the DMA arbiter is described in the Vweb VW2010 Programmer's Reference Manual.
- The DMA engine generates an interrupt upon completion of a transfer.

Note the following:

- A DMA channel is the logical assignment of a link list to a DMA engine, and the specific configuration of the physical data paths in the chip so that a physical connection would be established between the source and destination device to effect the data transfer specified in a particular descriptor in the link list.
- The operation of the DMA controller is totally transparent to the external host processor.
- The DMA controller, the DMA arbiter, the DMA channels and the link lists are accessible only by the RISC processor embedded in the VW2010.
- External host access to the DMA controller, and external host control of a DMA transfer, are implemented by means of high-level protocols and APIs, not by direct access to the DMA controller and its internal workings.
  The API is described in the Vweb VW2010 Programmer's Reference Manual.
- The link lists are generated and stored in SDRAM by the main RISC.
- The DMA configuration registers are set by the main RISC.
- The descriptors are downloaded into the other DMA registers by the main RISC.
- All hardware and software handshake is controlled by the main RISC. In hardware the DMA transfer specified in a descriptor proceeds with the usual handshake of DMA_Request and DMA_Grant signals.
- The DMA arbiter resolves race conditions (two channels issuing simultaneous bus requests), as well as simultaneous memory hits (two channels accessing the same address), by allowing one channel to go first, and making sure the other one goes next, ahead of any additional descriptors on the first channel that may be waiting.

## DMA Data Paths

In the VW2010, DMA transfers can take place between the devices shown in the following figure. However, that not all of the possible data paths between these devices make sense, and therefore some of them are not supported in firmware (see the Vweb VW2010 Programmer's Reference Manual for details).

A DMA channel is actually established between dedicated buffers set up in the encoder or decoder SDRAM (or in host memory) and the dmem (data cache memory) in the main RISC processor (see "Encoder Buffers" on page 22 and "Decoder Buffers" on page 30); that is, between

(1) the video, audio, user and other buffers in encoder or decoder SDRAM (or corresponding areas set up in host memory), and

(2) the host/PCI, MUX or DEMUX areas in dmem.

This is illustrated in Figure 17 on page 48.

Dmem is a 16 KB cache, which is implemented as dual-port memory; therefore it can DMA 8 KB at a time.

Note that there are two paths from the DMA engine into encoder or decoder SDRAM:

- Directly into the SDRAM controller (EMIU or DMIU), or
- Via the buffer controller (BUF or DEMUX) into the SDRAM controller (EMIU or DMIU).

The significance of the difference beween these two paths is explained in the Vweb VW2010 Programmer's Reference Manual

In either case, the SDRAM controller (EMIU or DMIU) is always the hardware interface to the external (encoder or decoder) SDRAM. The HIU is always the controller for the external host/PCI RAM.

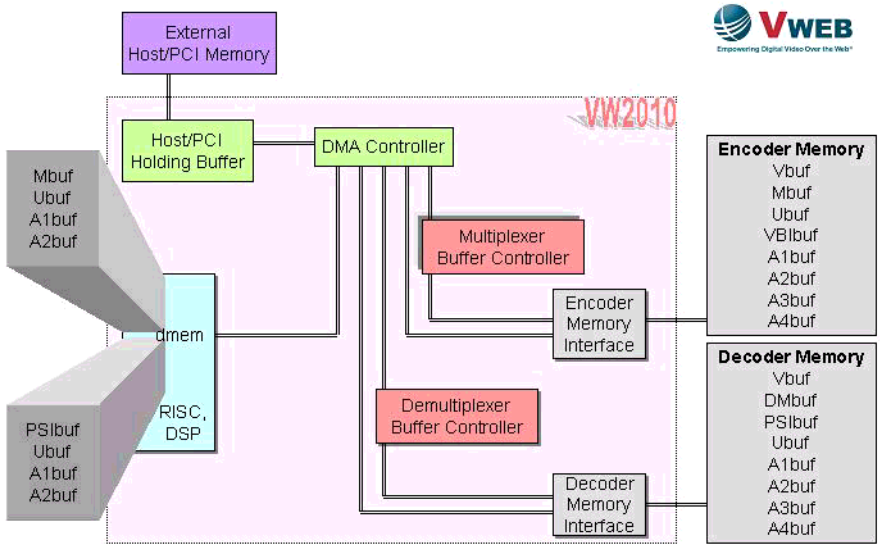


**Figure 17 SDRAM and dmem Buffers Active in DMA Transfers in the VW2010**

# ROM Interface (RIU)

An external ROM may be used to store the bootstrap code and the initial values for internal registers. If so, the ROM may be used either by the embedded main RISC processor or by the external host processor. The VW2010 supports physical ROM sizes up to 4M bytes (1M typical).

When the ROM is selected and its output is enabled, using the rom_cs and rom_oe signals from the VW2010 chip, the ROM puts its contents onto the rom_data bus. When

the rom_cs and rom_oe signals are not active, the rom_data bus is used to specify the VW2010 chip's power-up modes.

## Power-Up Modes

The ROM data bus is used for specific functions at power-up reset, as specified below. The state of the ROM data bus pins is latched into registers at reset; the registers can then be read by software.

### *Boot Mode*

rom_data[2] selects the boot mode:

1 = Boot from ROM

0 = Boot from host (via ICI or HIU, set by rom_data[6])

rom_data[6] further refines the selection of the boot mode:

1 = Boot from ICI

0 = Boot from host (in PCI, Motorola or Intel mode, set by rom_data[1:0])

### *Host Mode*

rom_data[1:0] select the HIU's host mode:

00 = reserved

01 = Motorola 16-bit async mode

10 = PCI mode

11 = Intel 16-bit mode

### *PCI Mode*

rom_data[4] selects the PCI mode:

1 = reserved

0 = Target mode (PCI slave mode; the VW2010 is DMA bus master)

### *Boot Mode Stuffing Options*

The rom_data pins have internal pull-up resistors (~100K ohms); therefore, at boot time the rom_data pins default to high (1). This is an invalid configuration state; therefore the chip's configuration must be set by using external 10K pull-down resistors ("stuffing option") to pull the appropriate pins low (0).

Example:

Select the PCI host interface mode by setting rom_data[1:0] to 10; that is, not stuffing the external pull-down resistor option on rom_data[1] to leave it high, and stuffing it on rom_data[0] to pull it low.



**Table 5 Boot Mode Selection Truth Table**

| rom_data [ ] | | | | | | | | Boot Mode |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | 0 | | x | | 1 | x | x | See "Boot from ROM" on page 46 |
| | 1 | | x | | 0 | x | x | See "Boot from ICI" on page 46 |
| | 0 | | x | | 0 | 0 | 1 | Boot from host in Motorola mode |
| | 0 | | 0 | | 0 | 1 | 0 | Boot from host in PCI target mode |
| | 0 | | x | | 0 | 1 | 1 | Boot from host in Intel mode |

**Table 6 Boot Mode Pull-Down Resistor Stuffing Option**

| rom_data [ ] | | | | | | | | Boot Mode |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | in | | | | | | | See "Boot from ROM" on page 46 |
| | | | | | in | | | See "Boot from ICI" on page 46 |
| | in | | | | in | in | | Boot from host in Motorola mode |
| | in | | in | | in | | in | Boot from host in PCI target mode |
| | in | | | | in | | | Boot from host in Intel mode |

***EJTAG Enable***

rom_data[3] enables the EJTAG port (switches between EJTAG and VBI):

1 = Enable (the VW2010 chip runs in EJTAG mode)

0 = Disable (the VW2010 chip runs in VBI mode)

And, accordingly, rom_data[3] switches the direction of the VBI bus:

1 = Output (the VW2010 chip outputs EJTAG data)

0 = Input (the VW2010 chip accepts VBI data)

*Note:* See important comments under "EJTAG Mode" on page 62.

***Chip Mode Select***

rom_data[5] selects where the Vweb firmware resides:

0 = Microcode resides in decoder SDRAM

In other words:

Set the chip in VW2010 mode by stuffing the external pull-down resistor option on the ROM_DATA[5] pin to pull it low. This has the effect of loading the Vweb firmware into the chip's decoder SDRAM.



# General Purpose I/O (GPIO)

The VW2010 supports 12 pins of GPIO, which can used as desired or reassigned to specific functions, under firmware control; for example:

- Pairs of GPIO pins can be assigned (by firmware) to serve a second ICI port. See "GPIO Signals" on page 82. The actual GPIO pins selected for this purpose depend on the specific board design; for example, pins 1:0, 2:1, 11:10, etc., have been used on various Vweb VW2010-based boards.
- GPIO pins 11:8 can be assigned (by firmware) to control the PCI port when the chip is in PCI host mode. See "GPIO Signals" on page 82.

- These and all other GPIO pins can, of course, be also used as general input, output or bi-directional (I/O) pins.

The GPIO module is controlled by two registers, data and direction. All GPIO pins default to inputs after a reset, and can be independently reconfigured as input or output by the GPIO registers.

Reading from and writing to a GPIO port is a two-step process. First, the GPIO direction register must be programmed (as input for read, output for write) in the bit position that corresponds to the GPIO pin. Then the data is read from (or written to) the GPIO data register.

*Note:* Any use of GPIO pins requires appropriate firmware support.

## Inter-Chip Communication Interface (ICI)

The VW2010 supports two pins for ICI, which is functionally similar to Philips $I^2C$ master mode. The VW2010 can be booted from a 128-byte SEEPROM which is connected to the ICI bus at boottime. After booting up, the VW2010 resumes normal operation in ICI master mode, to program $I^2C$ slave devices such as the SAA7115, for example.

*Note:* The current version of the Vweb software supports two ICI ports.

The port on the SDA and SCL pins is of the type that sends one byte of data on every ICI cycle, or a series of subaddress+data pairs on every ICI cycle.

The port implemented on GPIO pins (see "GPIO Signals" on page 82) is of the type that sends 2-256 data bytes on every ICI cycle.

See the Vweb VW2010 Programmer's Reference Manual for details.

## Main Phase Locked Loop (PLL)

The main PLL generates the 162 MHz system clock and all other internal high-frequency clocks used in the VW2010. The PLL requires a 27 MHz external oscillator to run it.

The internal PLL can be disabled (bypassed) by asserting a bypass signal. In such a case, the 162 MHz system clock from an external source can be applied on the same input that is normally used for the 27 MHz oscillator input.

# Audio PLL

The audio PLL generates the audio master clocks shown in Table 7 on page 52 to drive the external audio ADC and DAC devices. The audio output clock is derived from the 27 MHz clock source, and is always equal to 256 times the selected sampling rate.

**Table 7 Audio PLL Output Frequencies**

| Sampling Frequency (kHz) | PLL Output (MHz) |
|---|---|
| 8 | 2.048 |
| 16 | 4.096 |
| 22.05 | 5.6558 |
| 24 | 6.144 |
| 32 | 8.192 |
| 44.1 | 11.289 |
| 48 | 12.288 |
| 96 | 24.576 |

If the audio PLL is not used, similar clock signals can be generated on the board and used as inputs to the VW2010's audio input and audio output modules.



# Power Management (PMU)

The VW2010 uses the techniques described below to reduce the operating power requirements of the device. The goal is to keep the standard operational power under 1 W. Its core operates at 1.8 V, and its I/O operates at 3.3 V with 5 V tolerance. The VW2010 has three basic power states: initial, sleep and normal, as summarized in Figure 18 on page 53 and described in the following sections.

## Initial State

After applying power or resetting the VW2010, the VW2010 enters the initial state. The external power-up or software reset generates an internal system reset that remains asserted for 32 clocks after the reset input is de-asserted. In the initial state, the system clock (162 MHz) is on, allowing the embedded or external host processor to configure the system. In this state:

- The PLL is on.
- The oscillator is operating at 162MHz.
- The system clock is on.
- The embedded or external host is on.
- The subsystem clocks are off.

- The VW2010 modules are off.

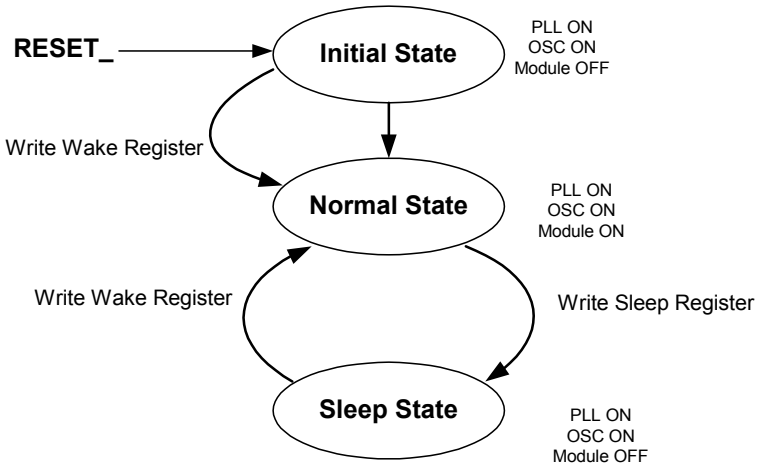


**Figure 18 Power-On / Reset States of the** VW2010

## Normal State

As soon as the embedded or external host turns on the subsystem clocks (by writing to the wake-up register either from the initial state or from the sleep state), the VW2010 enters the normal (working) state.

In the normal state, the VW2010 is processing data. In this state:

- The PLL is generating high-frequency clocks.
- The oscillator is operating at 162MHz.
- The system clock is on.
- The embedded or external host is on.
- The subsystem clocks are on.
- The VW2010 modules are on.

Note that, in the normal state, selected subsystem clocks may be turned on or off by writing to the clock control registers.

## Sleep State

The VW2010 enters the sleep state when the embedded or external host writes to the sleep register. In the sleep state, the system clock is off. In this state:

- The PLL is on.
- The oscillator is operating at 162MHz.
- The system clock is off.
- The embedded or external host is on.
- The subsystem clocks are off.
- The VW2010 modules are off.

Note that, by writing to clock control registers, selected subsystem clocks may be on or off, and the SDRAM auto-refresh may be set on or off, as desired in order to manage the chip's power consumption.

# JTAG

The VW2010 provides a test access port per IEEE Standard 1149.1, "Test Access Port and Boundary Scan Architecture." This port allows for boundary scan testing of the VW2010 on the board on which it is installed.

# Extended JTAG

The VW2010 also provides an extended test access port with additional functions that a JTAG emulator can use to test or control the chip, in accordance with the EPI (Embedded Performance, Inc.) EJTAG 2.0 protocol.

*Note:* EJTAG is for internal Vweb use only.

# Application Notes

## Basic Design

### *Design Example*

A board design using the components described above is the Vweb Win10 Evaluation Board. The glueless connections between the Vweb part and the vendor parts is shown on the Win10 schematics. Excerpts from the schematics of this and other Vweb boards are shown in the following figures.

### *Clock Source*

The VW2010 requires one external crystal oscillator to generate the basic 27 MHz clock, as illustrated in the next figure. The VW2010 generates internal and external clocks from this input.

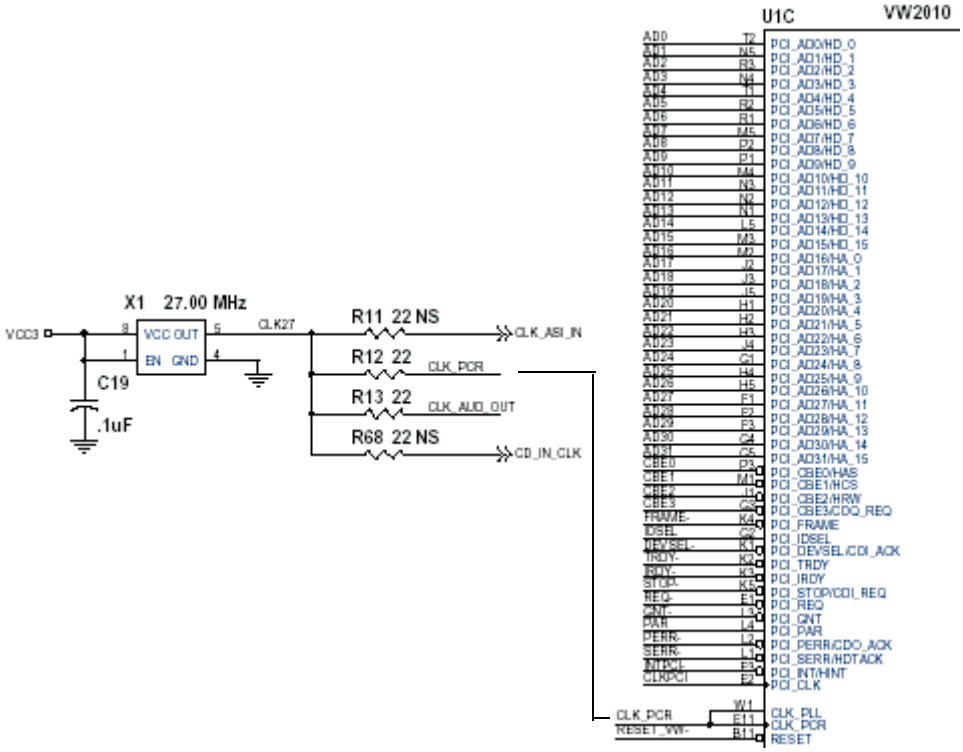


**Figure 19 VW2010 External Clock Oscillator**

***SDRAM Interface***

The VW2010 encoder connects directly, seemlessly, without glue logic, to SDRAM chip(s) such as the Micron MT48LC2M32 as illustrated in the next figure.

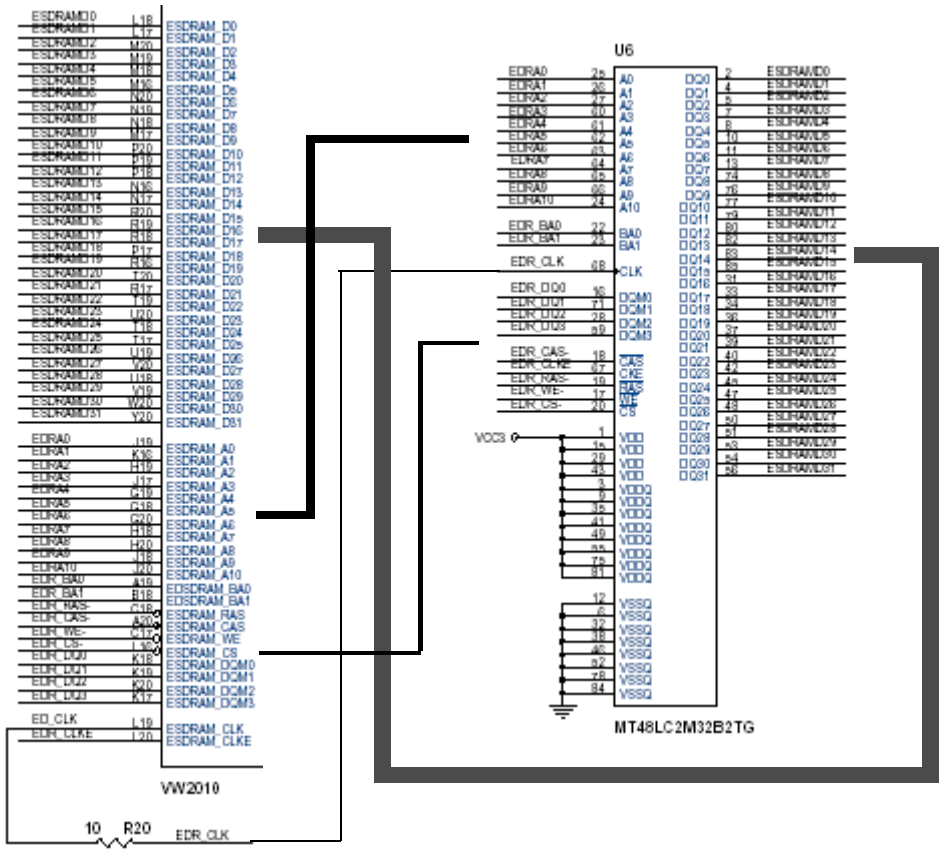


**Figure 20 VW2010 Encoder 2M32 SDRAM Interface**

The VW2010 decoder connects directly, seemlessly, without glue logic, to SDRAM chip(s) such as the Micron MT48LC1M16 or MT48MC2M32 as illustrated in the next two figures.

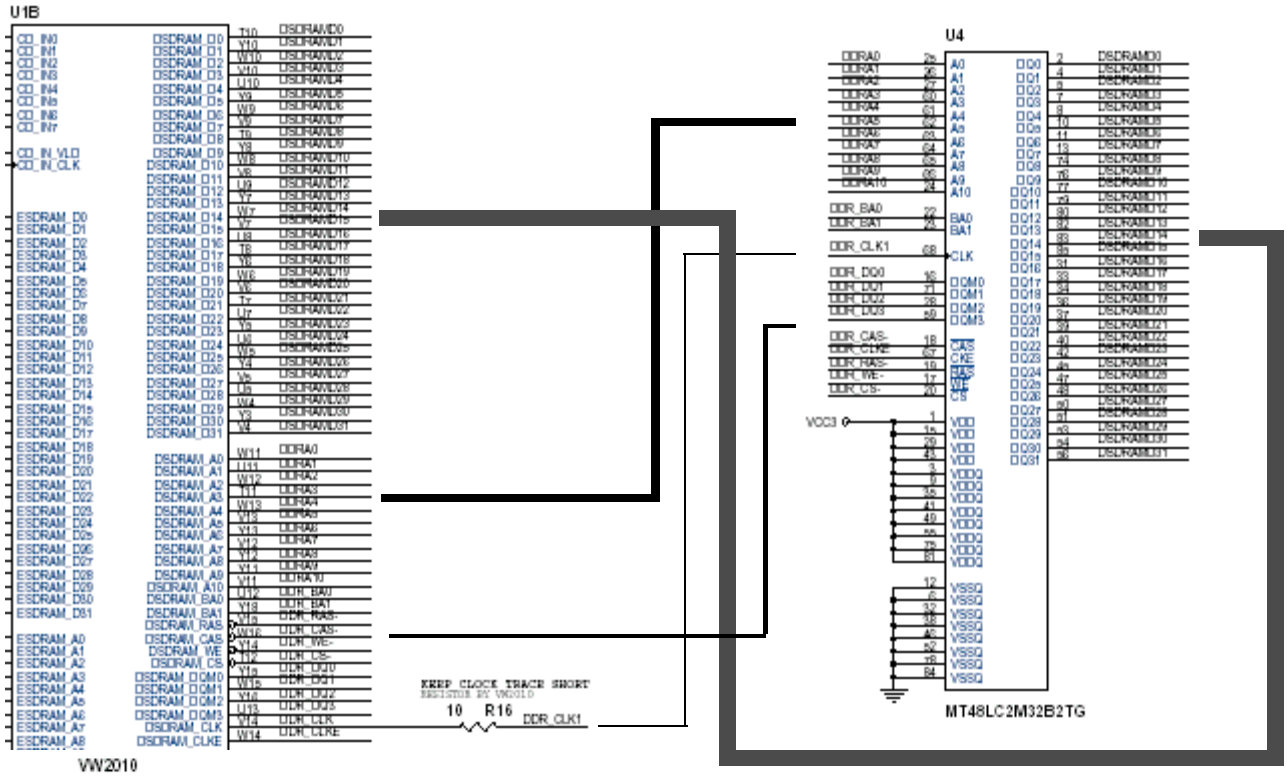


**Figure 21 VW2010 Decoder 2M32 SDRAM Interface**

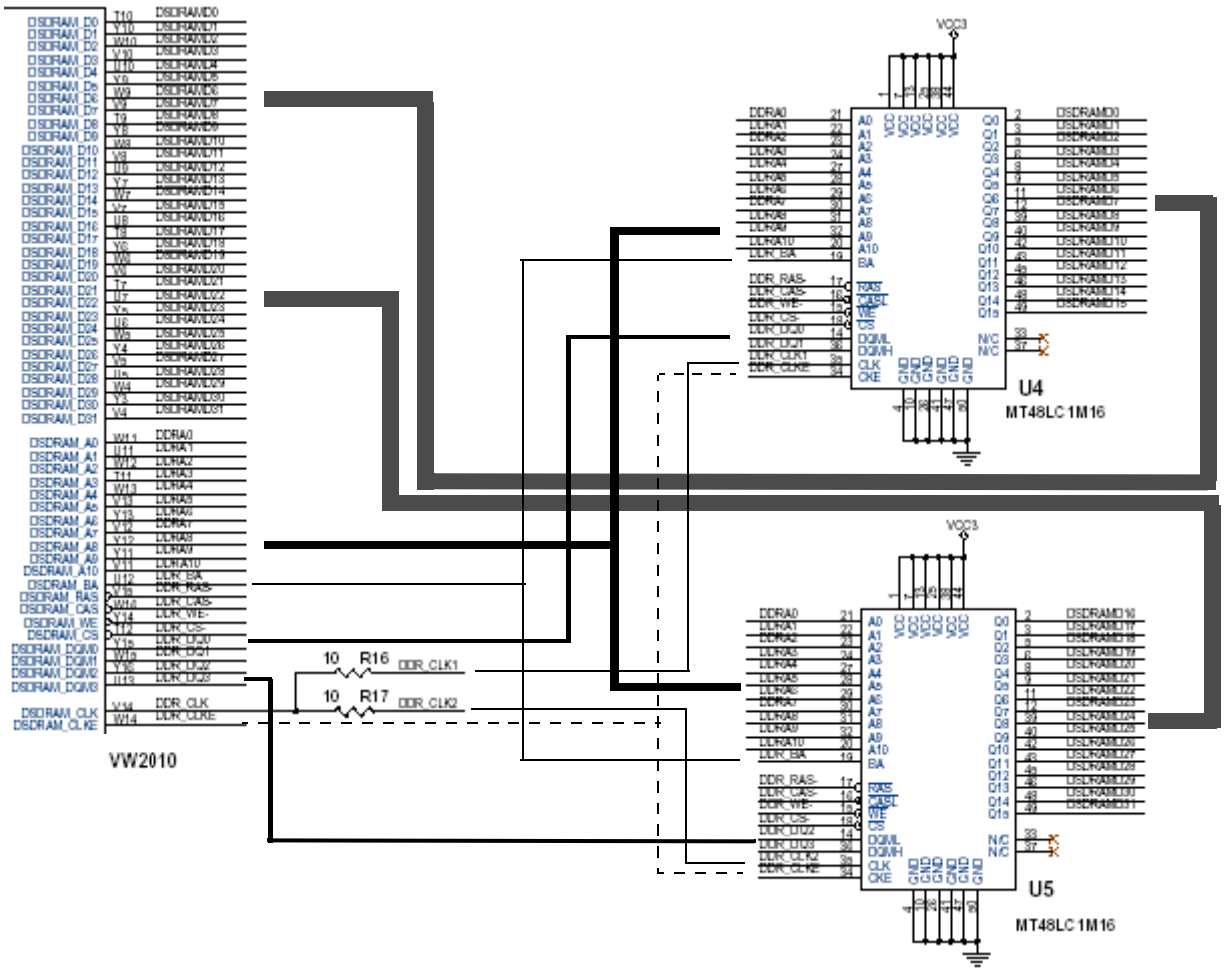


**Figure 22 VW2010 Decoder 1M16 SDRAM Interface**



***ROM Interface***

The VW2010 ROM interface connects directly, seemlessly, without glue logic, to a ROM chip such as the Atmel AT49BV1614 which is used to store all of the VW2010 microcode. This is illustrated in the next figure. However, because the ROM signal lines are active only at boot time, they are used for other purposes at other times. This is also illustrated in the next figure.

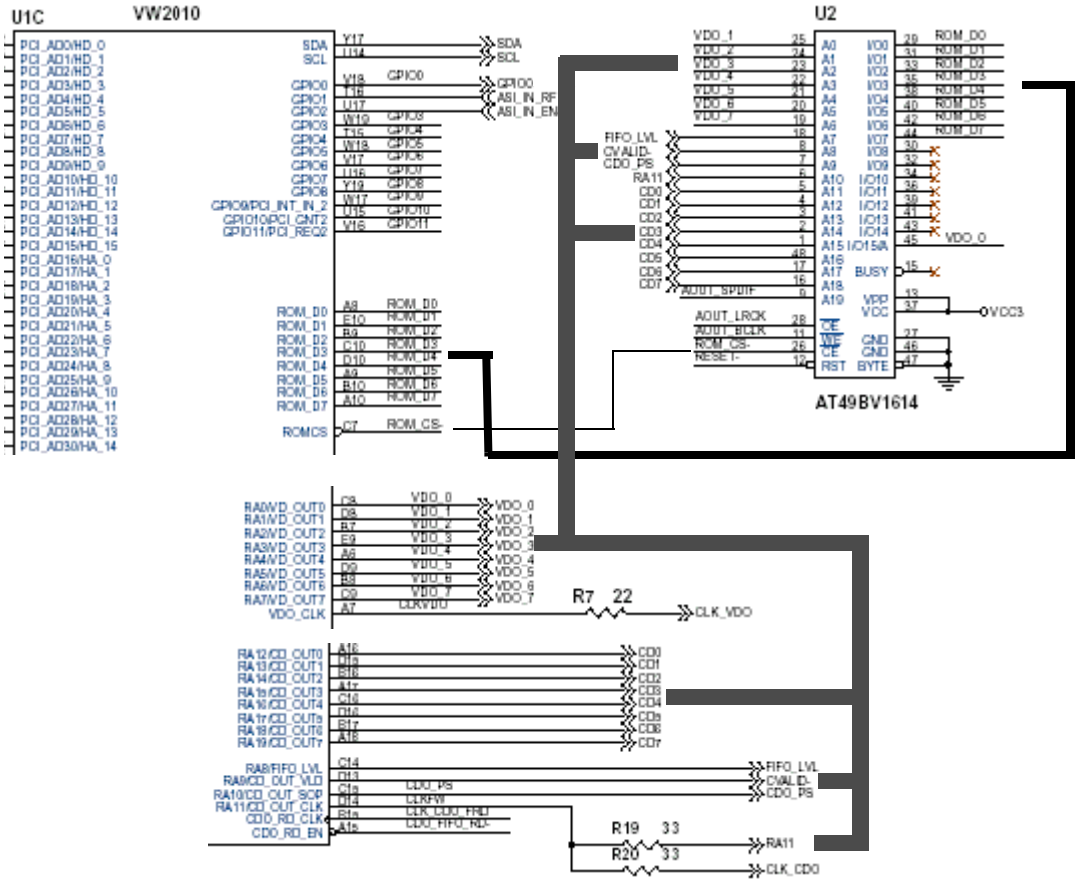


**Figure 23 VW2010 ROM Interface**

However, in some designs the user may decide to use a smaller EEPROM, such as the Xicor X24F032, to store only boot code (and download the full microcode at boot time from the external host via the host/PCI bus). This is illustrated in the next figure.

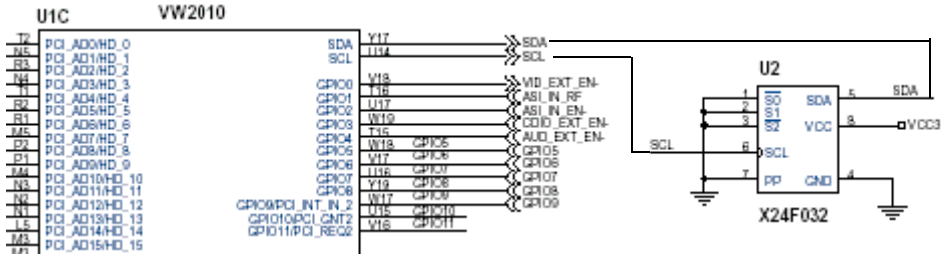


**Figure 24 VW2010 EEPROM Interface**

***Multiple Devices***

Two or more VW2010 devices can be connected to a single host bus or PCI bus.

- If connected to a PCI bus, the VW2010 devices must be configured as PCI slave (target) and the external host must be PCI host.
- If the VW2010 devices are connected to a Motorola- or Intel-style host, an external address decoder is required.

## PCI Interface

The VW2010 HIU connects directly, seemlessly, without glue logic, to a host/PCI port such as the typical edge connector on a PCI card as illustrated in the next figure. To put the VW2010 in PCI mode, proceed as follows:

- Set the ROM-Data pins [6:0] to b'0x0x010, to select PCI mode (see Table 5 and Table 6 on page 50).

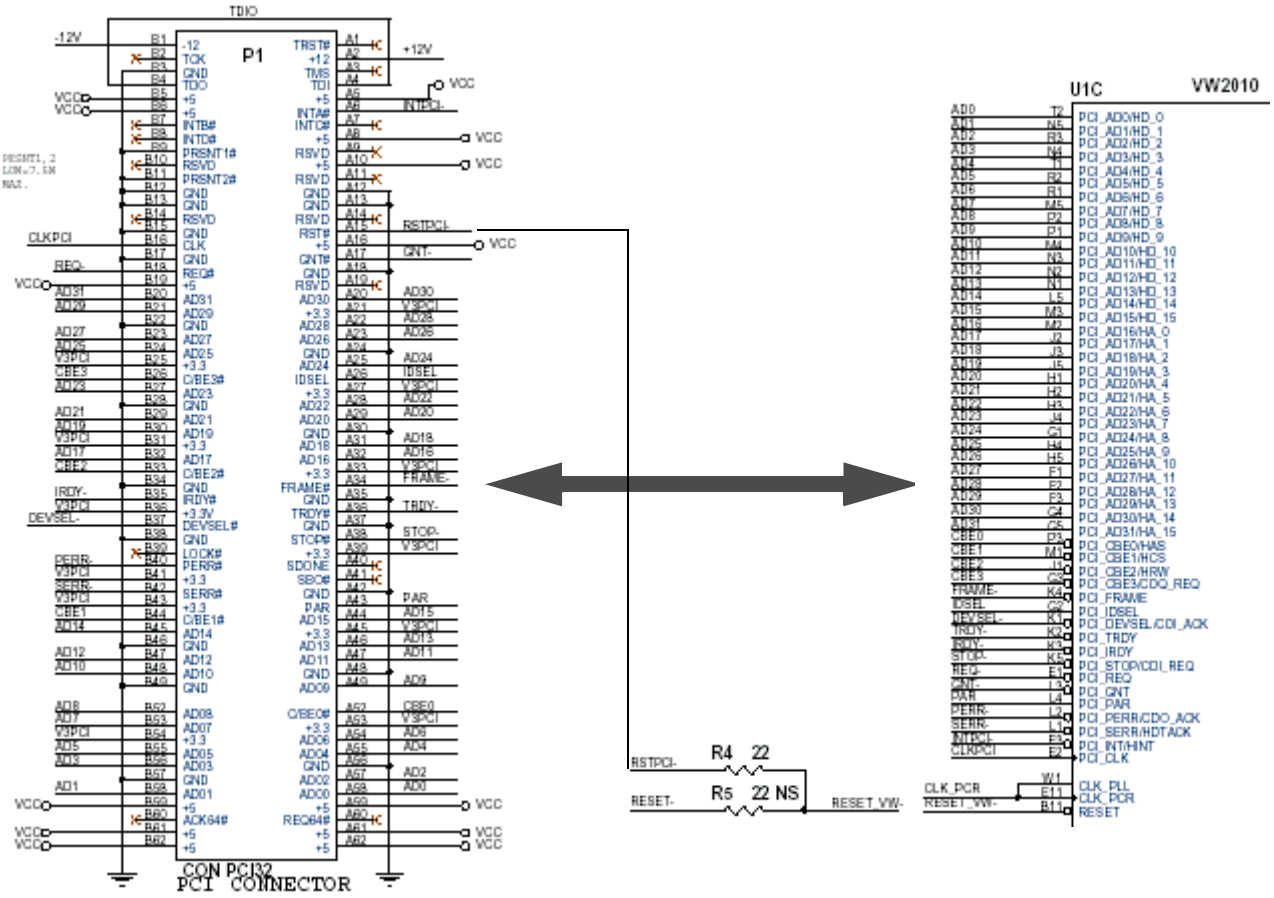


**Figure 25 VW2010 PCI Interface**

## Host Interface

The same set of pins that comprise the chip's PCI port are also used as the HIU port in Motorola or Intel mode. The VW2010 HIU connects directly, seemlessly, without glue logic, to a host interface such as USB chip, as illustrated in the next figure. To put the VW2010 in host mode, proceed as follows:

- Set the ROM-Data pins [6:0] to b'0x1x001 to select Motorola mode, or to b'0x1x011 to select Intel mode (see Table 5 and Table 6 on page 50).
- Tie the unused input pins to ground (see Table 15 on page 142).

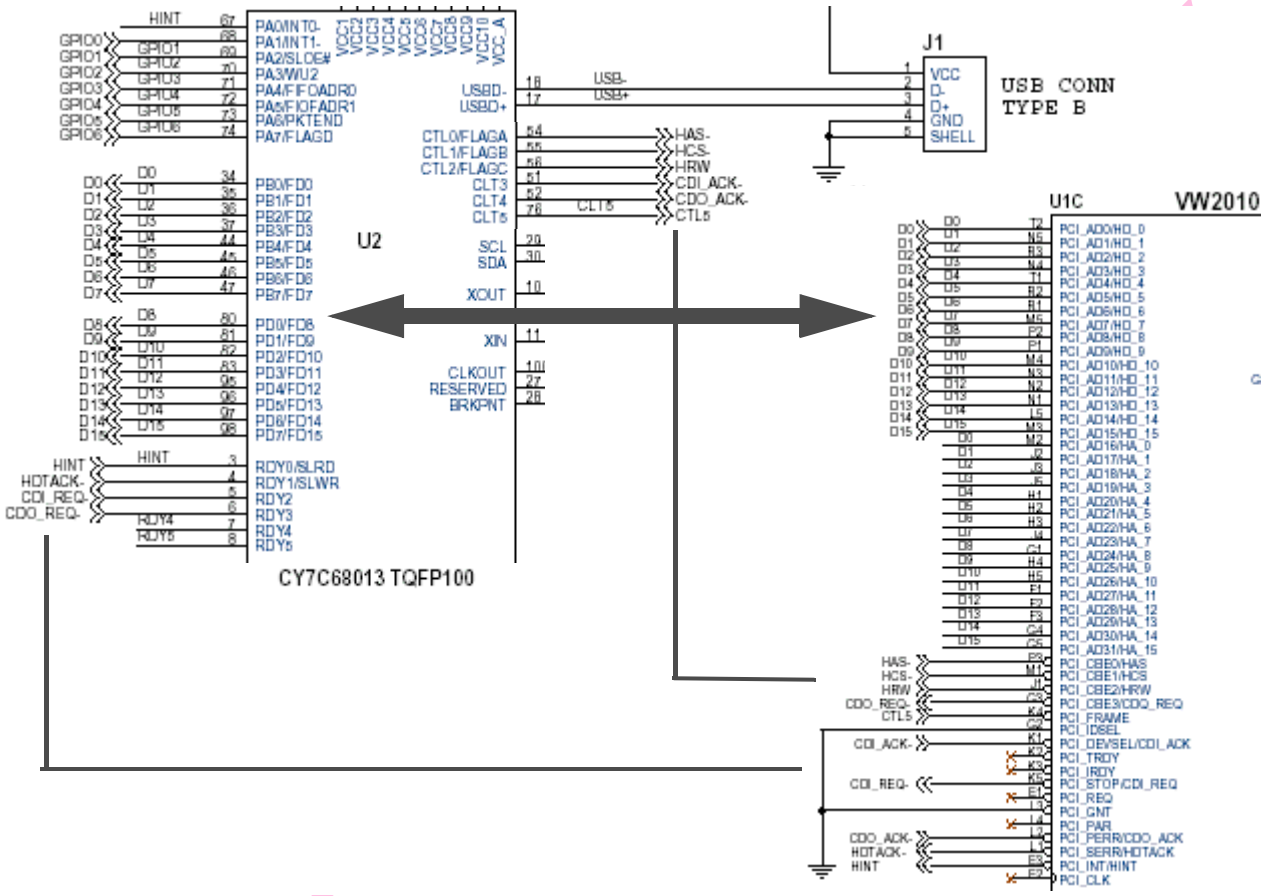


**Figure 26 VW2010 Host Interface (USB)**

## Embedded Host Mode

The VW2010 can be used in a completely embedded application that requires no external host. To put the VW2010 in this no-host mode, proceed as follows:

- Set the ROM-Data[1:0] pins to to b'0x1x011 to select Intel mode (see Table 5 and Table 6 on page 50).
- Tie the unused input pins to ground (see Table 15 on page 142).
- Tie the intel_ad[15:0] pins to ground (see Table 16 on page 144).
- Tie the following pins high to disable them:

- intel_cs_
- intel_as_
- intel_rd_
- intel_wr_ (see Table 17 on page 145)

## EJTAG Mode

When the EJTAG port is enabled, as described under "Power-Up Modes" on page 49,

- The VBI_data bus is switched from input to output. (The drive attributes of the pins are tri-state, and the direction of the bus is switched.)
- The VBI_data bus carries the signals of the ejtag_pcst3 and ejtag_pcst4 bus (instead of VBI input).
- If a hardware design calls for being able to switch the VBI_data bus between VBI data in and EJTAG data out, then external tri-state buffers are required to gate off the VBI data input.
- However, if the hardware design calls for using only one mode of these two modes (and never switch to the other mode), then the pins can be left unconnected (see also "Unused Pins" on page 92 and Table 15 on page 142).

# CHAPTER 6 *Encoder Interface Signals*



This chapter gives a brief description of the external input and output signals of the VW2010 encoder modules.

Note the following:

- Signal names that end in _ (the underscore character) indicate pins that are active low.
- Signals may also be multiplexed; that is, two or more signals may be assigned to the same physical pin. The multiplexing scheme is shown in Table 14 on page 141.
- The electrical properties of the I/O pads (pull-up, pull-down, tri-state, etc.) are shown in "Pin Lists" on page 87.

Figure 27 on page 64 identifies the video and audio I/O and control signals of the encoder in the VW2010.

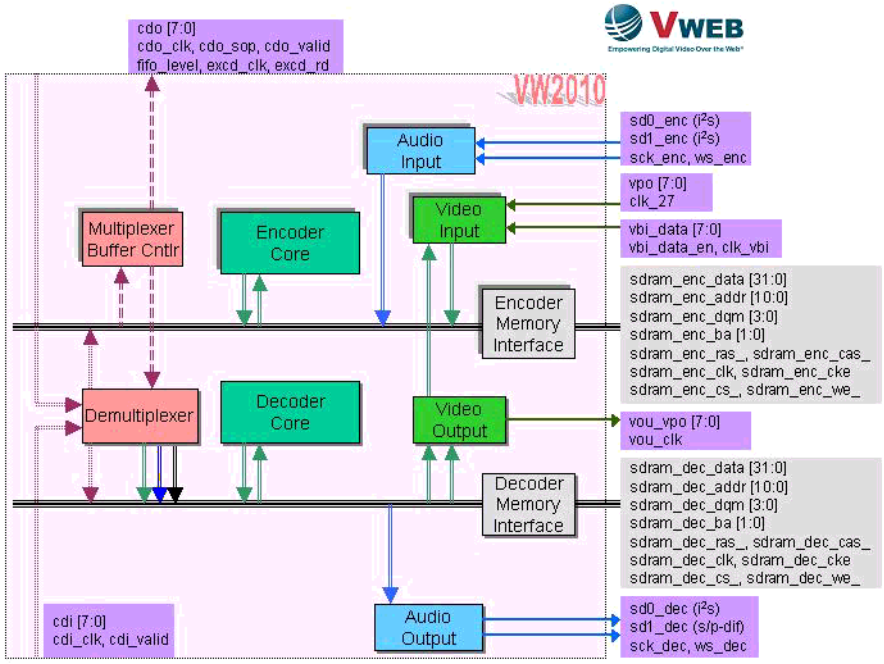


**Figure 27 Audio and Video I/O Signals of the VW2010**



## Video Input Interface

The VIU's external interface consists of the following signals.

| | | |
|---|---|---|
| *vpo [7:0]* | *Video Input Data* | *Input* |
| | These pins capture the interleaved luma and chroma sample (in 4:2:2 format). | |
| *clk_27* | *Video Input Clock* | *Input* |
| | This is the 27 MHz clock from D1 (ITU-R.BT.656). | |

## Audio Input Interface

The AIU's external interface consists of the following signals.

| | | |
|---|---|---|
| *sd0_enc* | *Encoder Audio Input Channel 1*<br>Serial $I^2S$ data is transmitted in two's complement with MSB first. | *Input* |
| *sd1_enc* | *Encoder Audio Input Channel 2*<br>Serial $I^2S$ data is transmitted in two's complement with MSB first. | *Input* |
| *sck_enc* | *Encoder Audio Clock* | *I/O* |
| *ws_enc* | *Encoder Audio Channel Select*<br>The word select line indicates the channel being transmitted:<br>0 = Channel 1 (Left)<br>1 = Channel 2 (Right) | *I/O* |

## VBI Input Interface

The VBI input interface consists of the following signals.

| | | |
|---|---|---|
| *vbi_data [7:0]* | *VBI Data In* | *Input* |
| *clk_vbi* | *External VBI Clock*<br>27 MHz Clock for VBI data. | *Input* |
| *vbi_data_en* | *VBI Data Enable*<br>The external VBI data is valid. | *Input* |

## Encoder Memory Interface

The EMIU's external interface consists of the following signals.

| | | |
|---|---|---|
| *sdram_enc_data [31:0]* | *SDRAM Data*<br>Read and write data are transferred between the VW2010 and SDRAM on these pins. | *I/O* |
| *sdram_enc_addr [10:0]* | *SDRAM Address*<br>This output connects directly to the corresponding SDRAM address inputs. | *Output* |

| | | |
|---|---|---|
| *sdram_enc_dqm [3:0]* | *SDRAM Input/Output Mask*<br>The DQM is an input mask signal for write accesses, and an output enable signal for read accesses.<br>The input data is masked when DQM is sampled high during a write cycle.<br>The output buffers are placed in a high-Z state (with a two-clock latency) when DQM is sampled high during a read cycle.<br>DQM [0] corresponds to SDRAM_DATA[7:0].<br>DQM [1] corresponds to SDRAM_DATA[15:8].<br>DQM [2] corresponds to SDRAM_DATA[23:16].<br>DQM [3] corresponds to SDRAM_DATA[31:24]. | *Output* |
| *sdram_enc_ba [1:0]* | *SDRAM Bank Select*<br>This output determines which SDRAM bank is selected.<br>See comment in "Application Notes" on page 67. | *Output* |
| *sdram_enc_ras_* | *SDRAM Row Address Strobe*<br>The memory interface asserts this signal when the SDRAM row address is on the SDRAM_ADDR[10:0] bus. | *Output* |
| *sdram_enc_cas_* | *SDRAM Column Address Strobe*<br>The memory interface asserts this signal when the SDRAM column address is on the SDRAM_ADDR[10:0] bus. | *Output* |
| *sdram_enc_clk* | *SDRAM Clock*<br>This output connects directly to the SDRAM clock input. | *Output* |
| *sdram_enc_cke* | *SDRAM Clock Enable*<br>This output connects directly to the SDRAM clock-enable input. | *Output* |
| *sdram_enc_we_* | *SDRAM Write Enable* | *Output* |
| *sdram_enc_cs_* | *SDRAM Chip Select*<br>CS_ enables (low) or disables (high) the SDRAM commands. | *Output* |



## Multiplexer Interface

The multiplexer's external interface consists of the following signals.

| | | |
|---|---|---|
| *cdo [7:0]* | *Compressed Data Out*<br>This is the bus for compressed data output from the VW2010. | *Output* |
| *cdo_clk* | *Compressed Data Out Clock*<br>27 MHz compressed data output clock; rising edge for strobing CDO signals.<br>This clock can be programmed to 6.75, 13.5, or 27 MHz.<br>The external device reading cdo[7:0] must be slaved to cdo_clk. | *Output* |
| *cdo_sop* | *Compressed Data Out Start Of Packet*<br>Packet start code | *Output* |
| *cdo_valid* | *Compressed Data Out Valid*<br>This is the CDO valid signal. | *Output* |
| *fifo_level* | *MUX FIFO Level*<br>This pin reports the status of the multiplexer's FIFO. | *Output* |
| *excd_clk* | *MUX External Clock*<br>This is an external clock. The multiplexer's compressed data can be output to an external device at this externally generated clock rate (instead of cdo_clk).<br>The maximum frequency of this clock cannot exceed 27 MHz. | *Input* |
| *excd_rd* | *MUX External Read Enable*<br>This is the read enable for the multiplexer's compressed data output. | *Input* |



# Application Notes

***Drive Attributes***

See the chapter titled "Pin Lists" on page 87 for the drive attributes of the signals, the use of multiplexed pins, and the board-level requirements for unused pins.

***AC Timing***

See the chapter titled "Electrical Characteristics" on page 147 for AC timing information.

***SDRAM Bank Select***

Both bank-selects sdram_enc_ba[1:0] are needed for 8 MB (2Mx32), only one bank-select is needed for 4 MB (1Mx16).

# CHAPTER 7 Decoder Interface Signals

This chapter gives a brief description of the external input and output signals of the VW2010 encoder modules.

Note the following:

- Signal names that end in _ (the underscore character) indicate pins that are active low.
- Signals may also be multiplexed; that is, two or more signals may be assigned to the same physical pin. The multiplexing scheme is shown in "Pin Lists" on page 87.
- The electrical properties of the I/O pads (pull-up, pull-down, tri-state, etc.) are shown in "Pin Lists" on page 87.

Figure 28 on page 70 identifies the video and audio I/O and control signals of the encoder and decoder in the VW2010. The bottom row of modules belong to the decoder.

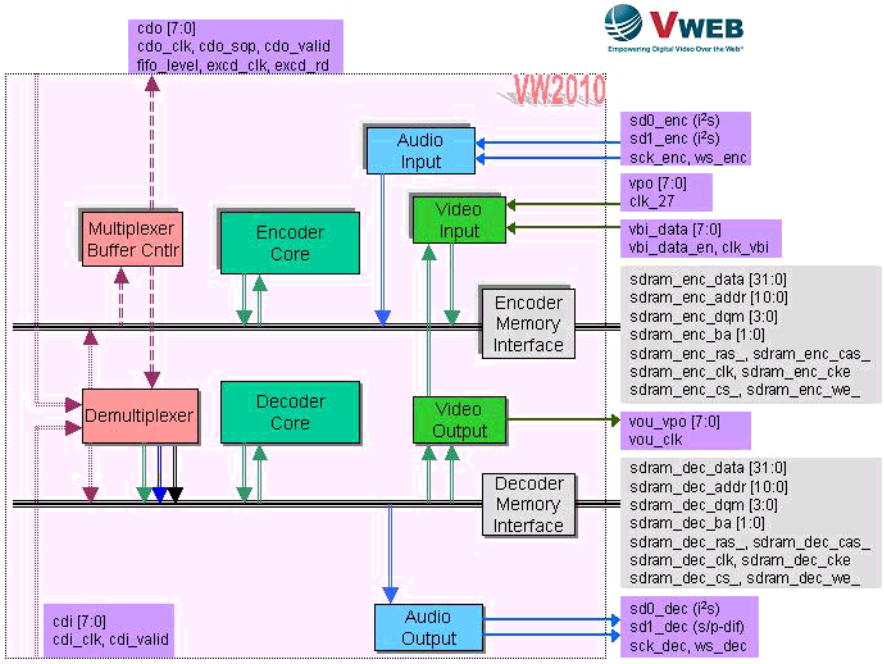


**Figure 28 Audio and Video I/O Signals of the VW2010**



# Demultiplexer Interface

The demultiplexer's external interface consists of the following signals.

| | | |
|---|---|---|
| *cdi [7:0]* | *Demux Data In* | *Input* |

CDI[7:0] is input compressed data from a device such as an MPEG encoder. The data is latched on the rising edge of CDI_CLK if CDI_VALID is high. (There is no handshake or confirmation that data was transferred.) The port can be programmed to operate in serial (1-bit) or parallel (8-bit) mode.

In parallel mode, all 8 bits of data are latched on the rising edge of CDI_CLK.

In serial mode, only CDI[0] is used as input, and it is latched on the rising edge of CDI_CLK; all others are ignored.

| | | |
|---|---|---|
| *cdi_valid* | *Demux Input Data Enable* | *Input* |
| | CDI_VALID is an active-high input signal used to indicate that valid data is on the CDI[7:0] input data bus. Data is latched on the rising edge of CDI_CLK. | |
| *cdi_clk* | *Demux Input Data Clock* | *Input* |
| | CDI_CLK is a clock input. The positive edge of this clock is used to latch the data CDI[7:0] into the VW2010. | |

## Decoder Memory Interface

The DMIU's external interface consists of the following signals.

| | | |
|---|---|---|
| *sdram_dec_data [31:0]* | *SDRAM data bus* | *I/O* |
| | This 32-bit I/O data bus is connected directly to SDRAM. | |
| *sdram_dec_addr [10:0]* | *SDRAM Address Bus* | *Output* |
| | The row/column address bus for SDRAM memory. | |
| *sdram_dec_dqm [3:0]* | *SDRAM Input/Output Mask* | *Output* |
| | The DQM is an input mask signal for write accesses, and an output enable signal for read accesses.<br>The input data is masked when DQM is sampled high during a write cycle.<br>The output buffers are placed in a high-Z state (with two-clock latency) when DQM is sampled high during a read cycle.<br>DQM [0] corresponds to SDRAM_DATA[7:0].<br>DQM [1] corresponds to SDRAM_DATA[15:8].<br>DQM [2] corresponds to SDRAM_DATA[23:16].<br>DQM [3] corresponds to SDRAM_DATA[31:24]. | |
| *sdram_dec_ba [1:0]* | *SDRAM Bank Select* | *Output* |
| | BA selects the bank to which the Active, Read, Write or Pre-charge command is being applied.<br>See comment in "Application Notes" on page 73. | |
| *sdram_dec_ras_* | *SDRAM Row Address Strobe* | *Output* |
| | The memory interface asserts this signal when the SDRAM row address is on the SDRAM_ADDR[10:0] bus. | |

| | | |
|---|---|---|
| *sdram_dec_cas_* | *SDRAM Column Address Strobe* | *Output* |
| | The memory interface asserts this signal when the SDRAM column address is on the SDRAM_ADDR[10:0] bus. | |
| *sdram_dec_clk* | *SDRAM Clock* | *I/O* |
| | This is the 162 MHz SDRAM clock. This signal should be connected as close as possible to the PLL_CLK pin of the VW2010. | |
| *sdram_dec_cke* | *SDRAM Clock Enable* | *Output* |
| | This output connects directly to the SDRAM's clock enable input. | |
| *sdram_dec_we_* | *SDRAM Write Enable* | *Output* |
| | The memory interface asserts WE_ for SDRAM write cycles and holds it deasserted for SDRAM read cycles. | |
| *sdram_dec_cs_* | *SDRAM Chip Select* | *Output* |
| | CS_ enables (low) and disables (high) the command decoder. | |

## Video Output Interface

The VOU's external interface consists of the following signals.

| | | |
|---|---|---|
| *vou_vpo [7:0]* | *Video Data Out* | *Output* |
| | This is the output data that represents the pixel data of the reconstructed picture. The pixel data is in CCIR-601 (ITU-R.BT.656) YCbCr format. | |
| *vou_clk* | *Video Out Clock* | *Output* |
| | This is the video output sampling clock at a nominal frequency of 27 MHz. The output data is driven on the rising edge of this clock. | |

## Audio Output Interface

The AOU's external interface consists of the following signals.

| | | |
|---|---|---|
| *sd0_dec* | *Audio Out Channel 1 - I2S* | *Output* |
| | Serial audio data is transmitted in two's complement with the MSB first. | |

| | | |
|---|---|---|
| *sd1_dec* | *Audio Out Channel 2- S/P-DIF*<br>Serial audio data is transmitted in two's complement with the MSB first.<br>The actual bitstream is either S/P-DIF uncompressed digital audio, or IEC-61937 compressed audio. | *Output* |
| *sck_dec* | *Audio Out Clock*<br>Audio clock | *Output* |
| *ws_dec* | *Audio Out Channel Select*<br>The word select line indicates the channel being transmitted :<br>0 = Channel 1 (Left)<br>1 = Channel 2 (Right) | *Output* |

## Application Notes

***Drive Attributes***

See the chapter titled "Pin Lists" on page 87 for the drive attributes of the signals, the use of multiplexed pins, and the board-level requirements for unused pins.

***AC Timing***

See the chapter titled "Electrical Characteristics" on page 147 for AC timing information.

***SDRAM Bank Select***

Both bank-selects sdram_dec_ba[1:0] are needed for 8 MB (2Mx32), only one bank-select is needed for 4 MB (1Mx16).

# CHAPTER 8 *System Interface Signals*



This chapter gives a brief description of the external input and output signals of the VW2010 system modules.

Note the following:

- Signal names that end in _ (the underscore character) indicate pins that are active low.
- Signals may also be multiplexed; that is, two or more signals may be assigned to the same physical pin. The multiplexing scheme is shown in Table 14 on page 141.
- The electrical properties of the I/O pads (pull-up, pull-down, tri-state, etc.) are shown in "Pin Lists" on page 87.
- The HIU and the PCI access the outside world via shared pins (that is, the VW2010 can use either the HIU or the PCI, but not both at the same time). [1]
- Similarly, the ROM address bus shares pins with (is multiplexed with) the encoder's video output signals, with the decoder's video output signals, and with the decoder's audio output signals. [2]

Figure 29 on page 76 identifies the system I/O and control signals of the VW2010.

1. The host interface modes of the VW2010 are listed in "Host Interface Modes" on page 3, and the host interface mode is selected as described in "Host Mode" on page 49. The host interface signals of the VW2010 are described in the following sections, and the pin sharing and electrical characteristics are shown in Table 16 and Table 17 on page 145
2. The signal multiplexing scheme of the VW2010 is described in Table 14 on page 141.

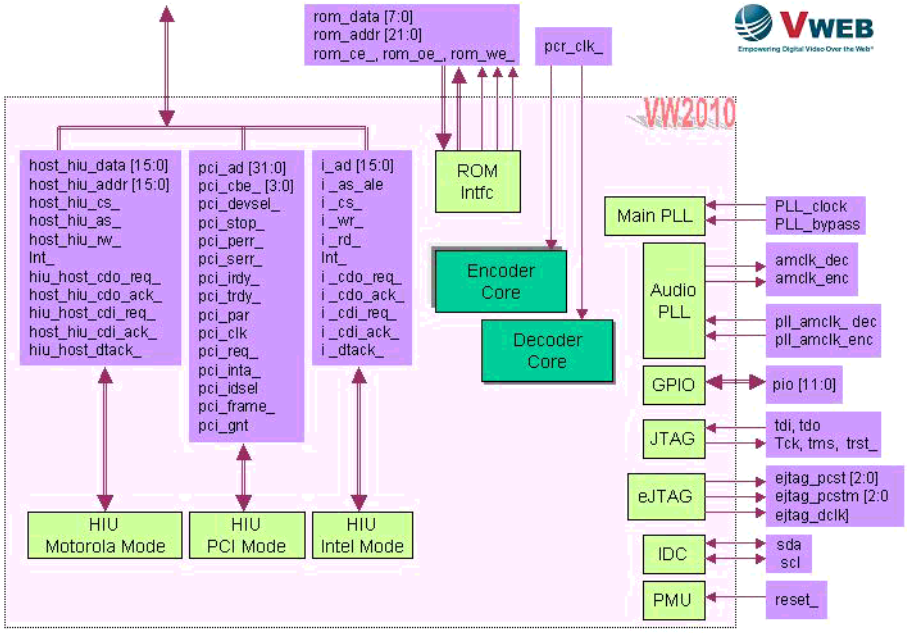


**Figure 29 System I/O Signals of the VW2010**



## Host Interface, Motorola Mode

The HIU's external interface in the Motorola (68K) mode consists of the following signals.

*Note:* The Motorola interface is always in 16-bit mode. Therefore, the UDS and LDS signals of a typical Motorola interface are not used.

*Note:* Motorola mode is big-endian. For example, 0x1234 is stored as 0x1234; the most significant bit comes first in memory.

| | | |
|---|---|---|
| *host_hiu_data [15:0]* | *Host Data* | *I/O* |
| | This is the data bus to/from the external host, to read or write data. | |
| *host_hiu_addr [15:0]* | *Host Address* | *Input* |
| | This is the address bus from the external host, used in an HIU command to access internal registers or memory locations. | |

| | | |
|---|---|---|
| *host_hiu_as_* | *Host Address Select* | *Input* |
| | This is the host address select pin, used to indicate the validity of the address bus. | |
| *host_hiu_cs_* | *Host Chip Select* | *Input* |
| | This is the host chip select pin, used to indicate that the bus is being used by the VW2010. | |
| *host_hiu_rw_* | *Host Read/Write* | *Input* |
| | This is the host read/write select pin (read high, write low). | |
| *int_* | *Host Interrupt* | *Output* |
| | This pin indicates that an interrupt has occurred. The host can check the interrupt source by reading the INTS Source Register after an interrupt is detected. | |
| *hiu_host_cdo_req_* | *Compressed Data Out Request* | *Output* |
| | Host DMA control. This is the request from the HIU to the external host, when the chip has compressed data ready to send to the host. | |
| *host_hiu_cdo_ack_* | *Compressed Data Out Acknowledge* | *Input* |
| | Host DMA control. This is the acknowledge from the external host to the HIU when the host is ready to accept the compressed data. The data is put on the host bus one clock later. | |
| *hiu_host_cdi_req_* | *Compressed Data In Request* | *Output* |
| | Host DMA control. This is the request from the HIU to the external host, when the chip is ready to accept compressed data from the host. | |
| *host_hiu_cdi_ack_* | *Compressed Data In Acknowledge* | *Input* |
| | Host DMA control. This is the acknowledge from the external host to the HIU that the host is sending the compressed data. The data is put on the host bus one clock later. | |
| *hiu_host_dtack_* | *Host CDO Transfer Acknowledge* | *Output* |
| | This is the host input data acknowledge, used to indicate the completion of the external host's read/write operation. | |

For the pin-out and electrical characteristics of the pins, see Table 16 and Table 17 on page 145, and the other tables in the chapter titled "Pin Lists" on page 87.

For interface timing diagrams, see Figure 34 and Figure 35 on page 150.

# Host Interface, Intel Mode

The HIU's external interface consists of the following signals.

*Note:* Intel mode is little-endian. For example, 0x1234 is stored as 0x3412; the least significant bit comes first in memory.

*Note:* The internal buses of the VW2010 are big-endian; therefore, to store data as 0x1234 in VW2010 registers or SDRAM, in Intel mode the input data must be organized as 0x3412.

| | | |
|---|---|---|
| *intel_ad [15:0]* | *Host Data/Address*<br>This is the data/address bus to/from the external host, used in an HIU command to access internal registers or memory locations. | *I/O* |
| *intel_as_ale_* | *Host Address Select / Address Latch Enable*<br>This is the host address select pin, used to indicate the validity of the data/address bus. | *Input* |
| *intel_cs_* | *Host Chip Select*<br>This is the host chip select pin, used to indicate that the data/addressbus is being used by the VW2010. | *Input* |
| *intel_wr_* | *Host Write*<br>This is the host write select pin. | *Input* |
| *intel_rd_* | *Host Read*<br>This is the host read select pin. | *Input* |
| *int_* | *Host Interrupt*<br>This pin indicates that an interrupt has occurred. The host can check the interrupt source by reading the INTS Source Register after an interrupt is detected. | *Output* |
| *intel_cdo_req_* | *Compressed Data Out Request*<br>Host DMA control. This is the request from the HIU to the external host, when the chip has compressed data ready to send to the host. | *Output* |
| *intel_cdo_ack_* | *Compressed Data Out Acknowledge*<br>Host DMA control. This is the acknowledge from the external host to the HIU when the host is ready to accept the compressed data. The data is put on the host bus one clock later. | *Input* |

| | | |
|---|---|---|
| *intel_cdi_req_* | *Compressed Data In Request* | *Output* |
| | Host DMA control. This is the request from the HIU to the external host, when the chip is ready to accept compressed data from the host. | |
| *intel_cdi_ack_* | *Compressed Data In Acknowledge* | *Input* |
| | Host DMA control. This is the acknowledge from the external host to the HIU that the host is sending the compressed data. The data is put on the host bus one clock later. | |
| *intel_dtack_* | *Host CDO Transfer Acknowledge* | *Output* |
| | This is the host input data acknowledge, used to indicate the completion of the external host's read/write operation. | |

For the pin-out and electrical characteristics of the pins, see Table 16 and Table 17 on page 145, and the other tables in the chapter titled "Pin Lists" on page 87.

For interface timing diagrams, see Figure 36 and Figure 37 on page 152.

## Host Interface, PCI Mode

The PCI port's external interface consists of the following signals.

| | | |
|---|---|---|
| *pci_ad [31:0]* | *Address/Data Bus* | *I/O* |
| | This 32-bit bus multiplexes the PCI address and data bus. A bus transaction on this bus starts with an address phase (PCI_FRAME_ is asserted), followed by at least one data phase (PCI_FRAME_ is deasserted during the last data phase).<br>During data phase, PCI_AD[7:0] contain the least-significant byte and PCI_AD[31:24] contain the most-significant byte.<br>Write data is valid when PCI_IRDY_ is asserted; read data is valid when PCI_TRDY_ is asserted. | |
| *pci_clk* | *Bus Clock* | *Input* |
| | This is the PCI bus clock. All PCI transactions are clocked with respect to PCI_CLK. It supports clock speeds up to 66 MHz. PCI_CLK is asynchronous to all other clocks. This input should be tied low when VW2010 is not connected to the PCI bus. | |
| *pci_cbe_[3:0]* | *Bus Command / Byte Enables* | *I/O* |
| | This four-bit bus multiplexes the bus command byte-enables. During the address phase of a bus transaction (when | |

PCI_FRAME_ is asserted), these pins contain the bus command. During the data phase, these pins are byte-enables.

| | | |
|---|---|---|
| *pci_devsel_* | *Device Select* | *I/O* |
| | A low driven onto this input indicates whether any device on the bus has been selected. When actively driven, it indicates that the driving device has decoded its address as the target of the current access. | |
| *pci_frame_* | *Frame Transaction* | *I/O* |
| | PCI_FRAME_ indicates the beginning and duration of a bus transaction. A high-to-low transition on PCI_FRAME_ indicates that a bus transaction is starting. A low-to-high transition on PCI_FRAME_ indicates that the transaction is in its final data phase, or is completed. | |
| *pci_gnt_* | *Bus Grant* | *Input* |
| | Assertion of this input indicates that the agent has been granted use of the PCI bus. The agent ignores this input when PCI_RST_ is asserted. | |
| *pci_idsel* | *Initialization Device Select* | *Input* |
| | This input is the active-high chip select during configuration reads and writes. | |
| *pci_inta_* | *Interrupt A* | *I/O* |
| | The processor asserts this output low to request attention from its device driver. The processor asserts PCI_INT_ asynchronously to PCI_CLK. | |
| *pci_irdy_* | *Initiator Ready* | *I/O* |
| | This signal is used in conjunction with PCI_TRDY_.<br>During a write transaction, a low on PCI_IRDY_ indicates that valid data is present on PCI_AD[31:0].<br>During a read transaction, a low on PCI_IRDY_ indicates the current master is ready to accept data.<br>The data phase is completed when PCI_TRDY_ and PCI_IRDY_ are both sampled asserted. | |
| *pci_par* | *Parity* | *I/O* |
| | PCI_PAR provides even parity across PCI_AD[31:0] and PCI_CBE[3:0]. | |
| *pci_perr_* | *Parity Error* | *I/O* |
| | Assertion of this signal indicates that a data parity error occurred during a PCI transaction. | |

Bit 6 in the PCI Command Register must be set to 1 for this signal to be asserted.

| | | |
|---|---|---|
| *Pci_req_* | *Bus Request* | *Output* |
| | The processor asserts this output to the bus arbiter when it wants control of the PCI bus. | |
| *pci_serr_* | *System Error* | *Output* |
| | Assertion of this signal indicates that an address parity error occurred during a PCI transaction.<br>Bit 8 in the PCI Command Register must be set to 1 for this signal to be asserted. | |
| *pci_stop_* | *Stop Transaction* | *I/O* |
| | A low on PCI_STOP_ indicates that the current target is requesting that the master halt the current transaction. | |
| *pci_trdy_* | *Target Ready* | *I/O* |
| | This signal is used in conjunction with PCI_IRDY_.<br>During a read transaction, a low on PCI_TRDY_ indicates that valid data is present on PCI_AD[31:0].<br>During a write transaction, a low on PCI_TRDY_ indicates the target is ready to accept data.<br>The data phase is completed when PCI_TRDY_ and PCI_IRDY_ are both sampled asserted. | |

For the pin-out and electrical characteristics of the pins, see Table 16 and Table 17 on page 145, and the other tables in the chapter titled "Pin Lists" on page 87.

For interface timing diagrams, see Figure 38 and Figure 39 on page 154. For additional details, see the PCI 2.2 specification.

In PCI host mode, firmware can configure GPIO pins to control a second PCI port. See "GPIO Signals" on page 82.



## ROM Interface

The ROM port's external interface consists of the following signals.

| | | |
|---|---|---|
| *rom_data [7:0]* | *ROM Data* | *I/O* |
| | These bits have special functions at boot/reset time; for details, see "ROM Interface (RIU)" on page 48. | |
| *rom_addr [21:0]* | *ROM Address* | *Output* |

| | | |
|---|---|---|
| *rom_ce_* | *ROM Chip Enable* | *Output* |
| *rom_oe_* | *ROM Output Enable* | *Output* |
| *rom_we_* | *ROM Write Enable* | *Output* |

## Global Signals

The following input signals affect all modules in the VW2010.

| | | |
|---|---|---|
| *pcr_clk* | *PCR CLOCK*<br>27 MHz reference clock source for program clock recovery. | *Input* |
| *reset_* | *Global Reset*<br>This is the chip's global reset pin. | *Input* |

## GPIO Signals

The GPIO interface consists of the following signals.

| | | |
|---|---|---|
| *gpio [11:0]* | *General Purpose I/O*<br>These pins can be individually programmed as inputs or outputs through the GPIO registers. | *I/O* |
| *gpio [11:8]* | *PCI port 2*<br>**In PCI Host Mode only,** these three pins can be assigned by firmware to control a second PCI port, as follows:<br>GPIO[11] - Host PCI Request 2<br>GPIO[10] - Host PCI Grant 2<br>GPIO[9] - n/a<br>GPIO[8] - Host PCI Interrupt 2<br>These are functionally identical to the request, grant and interrupt signals, respectively, described in "Host Interface, PCI Mode" on page 79. | *I/O* |

| | | |
|---|---|---|
| *gpio [11:10]* | *ICI port 2* | *I/O* |
| | These two pins can be assigned by firmware to control a second ICI port, as follows<br>GPIO[11] - SCL 2<br>GPIO[10] - SDA 2<br>These are functionally identical to the $I^2C$ clock and $I^2C$ data signal, respectively, described in the next section (“ICI Signals”). | |

## ICI Signals

The ICI interface consists of the following signals.

| | | |
|---|---|---|
| *sda* | *ICI Data* | *I/O* |
| | The VW2010 inter-device communication interface (ICI) is a slave at reset, so the device can read boot code from the ROM. In normal mode, the device is ICI master. | |
| *scl* | *ICI Clock* | *I/O* |

## Main PLL Signals

The main PLL’s external interface consists of the following signals.

| | | |
|---|---|---|
| *PLL_clock* | *PLL Reference Clock* | *Input* |
| | This is the 27 MHz input from an external crystal oscillator, from which the PLL generates the 162 MHz system clock and other subsystem clocks in the chip. | |
| *PLL_bypass* | *PLL Disable* | *Input* |
| | Test pin only. This pin should be tied to ground during normal operation. This signal disables the PLL. Then an external 162 MHz system clock can be applied as input to the chip directly on the PLL-clock pin. | |

## Audio PLL Signals

The audio PLL's external interface consists of the following signals.

| | | |
|---|---|---|
| *amclk_enc* | *Audio In Master Clock*<br>This is the audio master clock from the encoder, to drive the external audio ADC. For the frequencies generated by the PLL, see Table 7 on page 52. | *Output* |
| *amclk_dec* | *Audio Out Master Clock*<br>This is the audio master clock from the decoder, to drive the external audio DAC. For the frequencies generated by the PLL, see Table 7 on page 52. | *Output* |
| *PLL_amclk_enc* | *External Audio In Master Clock*<br>This is the PLL bypass clock for the encoder, if the audio PLL is not used. | *Input* |
| *PLL_amclk_dec* | *External Audio Out Master Clock*<br>This is the PLL bypass clock for the decoder, if the audio PLL is not used. | *Input* |

## JTAG Signals

The JTAG interface consists of the following signals.

| | | |
|---|---|---|
| *tdi* | *Test Data In*<br>Test data and test instructions are shifted serially into this input during a TAP operation. | *Input* |
| *tdo* | *Test Data Out*<br>tTest data and test instructions are shifted serially out of this output during a TAP operation. | *Output* |
| *tclk* | *Test Clock*<br>This input clocks the state information, boundary scan instructions, and test data into and out of the processor during a TAP operation.<br>If the JTAG port is not used, this input should be tied low. | *Input* |
| *tms* | *Test Mode Select*<br>This input controls the state of the processor's TAP controller. | *Input* |

| | | |
|---|---|---|
| *trst_* | *Test Reset*<br>Asynchronous assertion of this input causes the processor to initialize the TAP controller.<br>If the JTAG port is not used, this input should be tied low. | *Input* |

## Extended JTAG Signals

The extended JTAG interface consists of the following signals.

*Note:* EJTAG is for internal Vweb use only.

| | | |
|---|---|---|
| *ejtag_pcst [2:0]* | *Program Counter Status Trace* | *Output* |
| *ejtag_pcst2 [2:0]* | *Program Counter Status Trace* | *Output* |
| *ejtag_pcst3 [2:0]* | *Program Counter Status Trace* | *Output* |
| *ejtag_pcs4 [2:0]* | *Program Counter Status Trace* | *Output* |
| *ejtag_dclk* | *Debug Clock* | *Output* |



## Application Notes

***Drive Attributes***

See the chapter titled "Pin Lists" on page 87 for the drive attributes of the signals, the use of multiplexed pins, and the board-level requirements for unused pins.

***AC Timing***

See the chapter titled "Electrical Characteristics" on page 147 for AC timing information.

***Signal Multiplexing***

Note the following:

- All host interface modes share the same set of I/O pins.
- The ROM data pins assume special functions at reset time.
- The ROM address pins are used as the I/O of other modules after reset.
- The GPIO pins can be programmed for specific purposes of the user's chosing.

- Some EJTAG pins are normally used for VBI data input.

For further information, see "Signal Multiplexing" on page 91 in general; for details, see Table 14, "Signal Multiplexing Scheme," on page 141 or Table 14 on page 141.

# CHAPTER 9 Pin Lists

## Summary of the Contents

This chapter presents the following information:

- Package dimensions
- Pin-out diagram
- Pin lists
- Signal multiplexing scheme
- Application notes



## Package Dimensions

The VW2010 comes in a 365-pin BGA package, with dimensions shown in the following table:

**Table 8 365L BGA Package Dimensions**

| Dimension | Measurement |
|---|---|
| Package | 27 x 27 x 2.33 mm |
| Ball pitch | 1.27 mm |
| Ball diameter | 0.75 mm |
| Substrate thickness | 0.56 mm |
| Mold thickness | 1.17 mm |
| Other dimensions | See Figure 30 on page 88, Figure 31 on page 88, Figure 32 on page 89 |

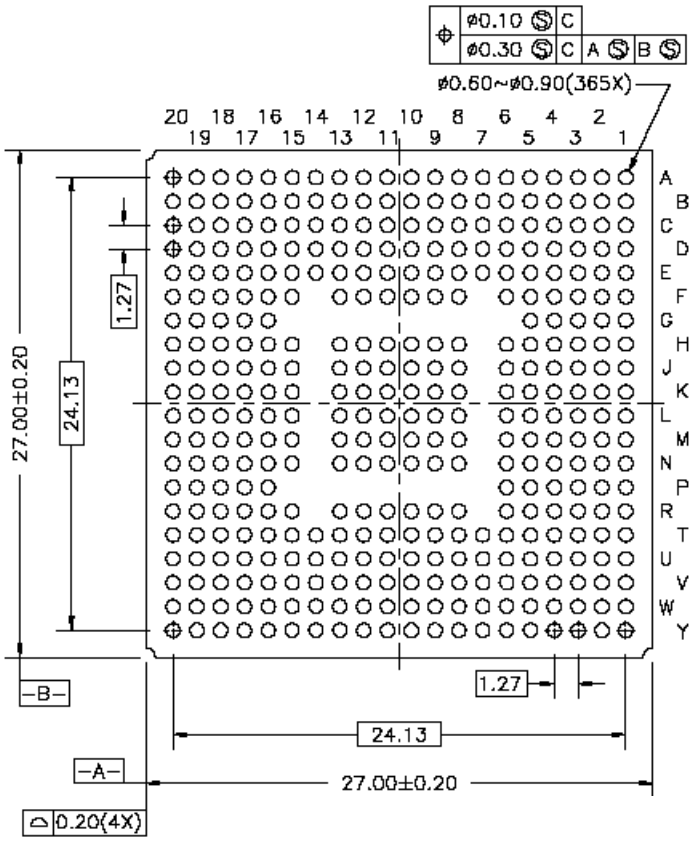


**Figure 30 Package and Ball Array Dimensions (bottom --> up view)**

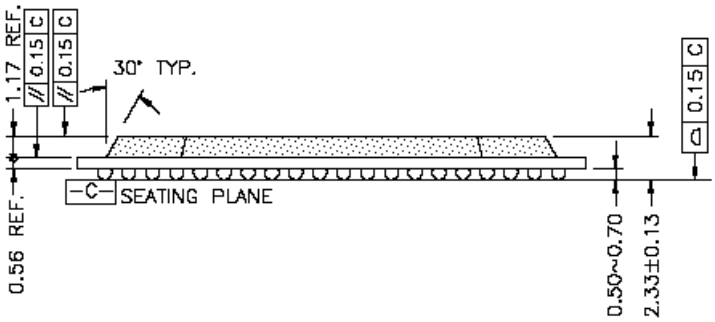


**Figure 31 Package Thickness Dimensions**

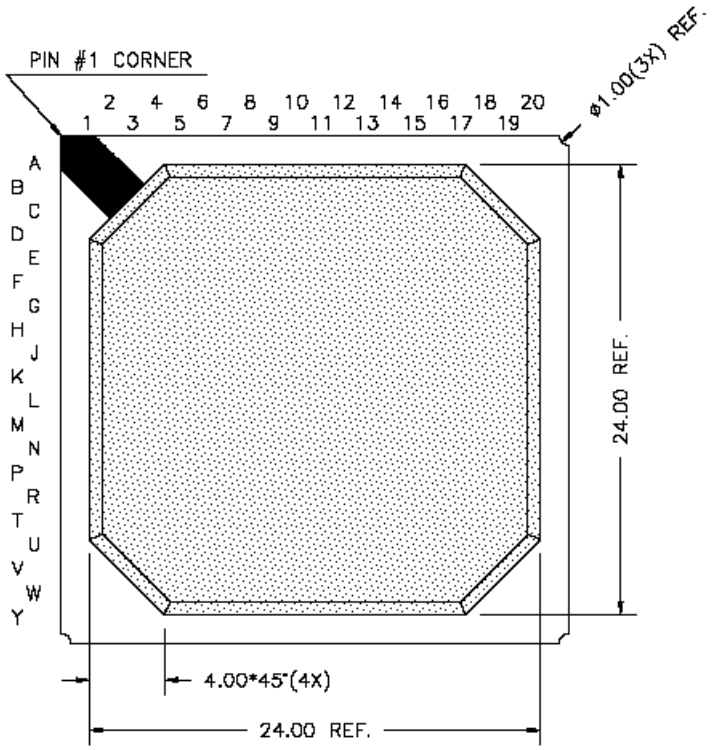


**Figure 32 Package Dimensions (top --> down view)**

## Pin-out Diagram

The pin-out diagram of the VW2010 is shown in Figure 33 on page 90. In the pin-out diagram, note the following:

- Balls numbered from 1 to 300 are the chip's I/O connections.
- Some of these numbered balls are also used for 1.8V core VDD, 1.8V PLL VDD, PLL VSS, 3.3V I/O VDD and I/O VSS.
- P1 are the 1VDD power ring (12 balls), used for 1.8V core VDD.
- P2 are the 0VDDA power ring (3 balls), used for 3.3V I/O VDD.
- P3 are the 0VDDM power ring (6 balls) used for 3.3V I/O VDD.
- P4 are the 0VDD3 power ring (4 balls) used for 3.3V I/O VDD.
- P5 are the PVDD power ring (4 balls), used for 3.3V I/O VDD.
- G/T are the ground/thermal connections (36 balls), used for core and I/O VSS.

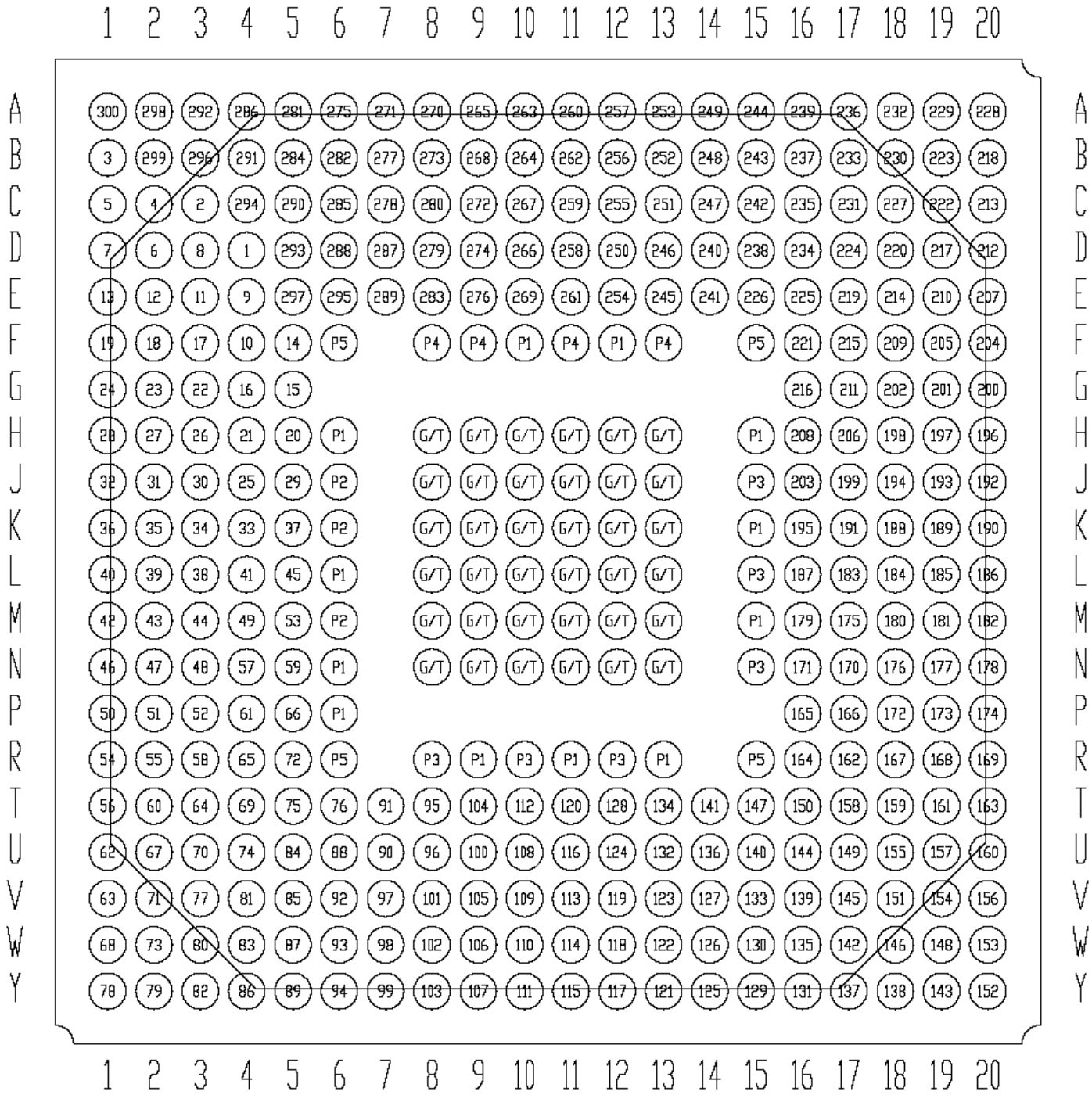


**Figure 33 BGA Ball Map of the VW2010 (top --> down view)**

## Pin Lists

The pin-out of the VW2010 is shown in pin lists sorted by various criteria:

- Table 9, "I/O Signals, Sorted by Pad Number," on page 93
- Table 10, "I/O Signals, Sorted by BGA Coordinates," on page 104
- Table 11, "I/O Signals, Sorted by Module," on page 115
- Table 12, "I/O Signals, Sorted by Signal Name," on page 126
- Table 13, "Power and Ground Connections," on page 137

## Signal Multiplexing

Table 14, "Signal Multiplexing Scheme," on page 141 summarizes the VW2010 chip's use of the same pins for multiple purposes.

The signal multiplexing scheme can also be inferred from Table 9, "I/O Signals, Sorted by Pad Number," on page 93, and Table 10, "I/O Signals, Sorted by BGA Coordinates," on page 104, where you may see two or three signals assigned to the same pad number or BGA coordinate, respectively.

The presentation of this information should not be automatically interpreted to mean that any one set of signals is necessarily "primary" or "secondary." Signal multiplexing simply means the use of the same set of pins for alternate purposes of the user's chosing.

The following are general cases of signal multiplexing in the VW2010 chip:

- The ROM data and address buses are used by the ROM at boot time, when microcode is being downloaded from the ROM into the VW2010 chip; at all other times the same pins are used for the chip's other, "normal" purposes.
- Again at boot time, the ROM data bus pins are used to set the host mode and other power-up modes of the VW2010 chip, as described in "ROM Interface (RIU)" on page 48.
- After power-up, the ROM address bus is not used by the ROM, and is available to support other functions. The upper bits of the ROM address bus are used for the compressed data out (CDO) data bus and its control signals. The low byte of the ROM address bus is used as the video output bus from the decoder. The two high bits of the ROM address bus are the audio outputs from the decoder.
- The host/PCI interface pins are shared by the VW2010 chip's HIU and PCI modules, and, as far as external devices are concerned, the VW2010 may look like a PCI, Motorola or Intel device, depending on how the chip's host mode is set at boot time. See Table 16 on page 144, Table 17 on page 145. This flexibility imposes a chip design requirement on the drive attributes of the chip's host interface pins, which is discussed in "Drive Attributes in Host Mode" on page 92.

# Application Notes

***Drive Strengths***

In the pin list Tables, a drive strength of "PCI" means that the VW2010 is PCI 66 core-compliant, and can work with standard loads of 2, 4, 8 or 16 ma. The actual drive strength is user-selectable.

***Drive Attributes***

The drive attribute shown in the pin list tables is a property of the pad; it is not a recommendation or requirement imposed on the design of a circuit using the VW2010.

For example, "pull-up" means that the pad has a built-in, internal pull-up resistor, and therefore normally the board designer using this chip does not have to put an external pull-up resistor on the pin. "Tri-state" means that the pad has built-in, internal logic to make the pin go tri-state when appropriate.

***Drive Attributes in Host Mode***

The VW2010 chip's host interface pins can be set to operate in one of the host modes listed in "Host Interface Modes" on page 3, and shown in detail in Table 16 on page 144 and Table 17 on page 145. The chip's corresponding I/O pads are designed so that the pins will always behave as required by the standard for the interface mode that was selected. For example, in PCI mode the same pin will behave as a standard PCI pin and go to tri-state as required by the PCI 2.2 specification. In another host mode, the same pin will be an input or an output, whichever is the correct behavior in the other host mode, and therefore the part of the pad's circuit that allowed the pad to go tri-state in PCI mode will be bypassed in the other host mode. See Table 16 on page 144, Table 17 on page 145.

***Clock Pins***

It is good board-design practice to route an active clock output signal through a series resistor connected to the pin.

***Unused Pins***

Unused output pins can be left unconnected / floating. In general, unused bi-directional pins can also be left unconnected / floating. Unused inputs should always be tied to their inactive state; that is, if the signal is active low, tie it high; if it is active high, tie it low. Exceptions are noted in Table 15 on page 142.

Note the following:

- Bi-directional pins of the host/PCI bus, if not used in a particular host mode, are automatically defaulted to tri-state in PCI mode, and to input-only or output-only in the other host modes. See "Drive Attributes in Host Mode" above; see also Table 16 on page 144, and Table 17 on page 145.
- See also "Embedded Host Mode" on page 61.
- It is good board-design practice to tie unused clock pins to ground.

***Termination Rules***

JTAG and EJTAG signals have their own external pull-up/pull-down/termination requirements, depending on the specific emulator used to test the board.

The ICI pins have their own termination rules, as described in the Philips $I^2C$ bus specification.

**Table 9 I/O Signals, Sorted by Pad Number**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 1 | cdi[7] | Demux | Compressed data in [7:0] | Input | | Pull-up | D4 |
| 2 | cdi[6] | Demux | Compressed data in [7:0] | Input | | Pull-up | C3 |
| 3 | cdi[5] | Demux | Compressed data in [7:0] | Input | | Pull-up | B1 |
| 4 | cdi[4] | Demux | Compressed data in [7:0] | Input | | Pull-up | C2 |
| 5 | cdi[3] | Demux | Compressed data in [7:0] | Input | | Pull-up | C1 |
| 6 | cdi[2] | Demux | Compressed data in [7:0] | Input | | Pull-up | D2 |
| 7 | cdi[1] | Demux | Compressed data in [7:0] | Input | | Pull-up | D1 |
| 8 | cdi[0] | Demux | Compressed data in [7:0] | Input | | Pull-up | D3 |
| 9 | cdi_valid | Demux | Compressed data in enable | Input | | Pull-up | E4 |
| 10 | cdi_clk | Demux | Compressed data in clock | Input | | Pull-up | F4 |
| 11 | int_ | HIU / Moto | Host interrupt | Output | PCI | Open-drain | E3 |
| 11 | int_ | HIU / Intel | Host interrupt | Output | PCI | Open-drain | E3 |
| 11 | pci_inta_ | HIU / PCI | PCI interrupt A | Output | PCI | Open-drain | E3 |
| 12 | pci_clk | HIU / PCI | PCI clock | Input | PCI | | E2 |
| 13 | pci_req_ | HIU / PCI | PCI bus request | Bi-Dir | PCI | Tri-state | E1 |
| 15 | host_hiu_addr[15] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | G5 |
| 15 | pci_ad[31] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | G5 |
| 16 | host_hiu_addr[14] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | G4 |
| 16 | pci_ad[30] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | G4 |
| 17 | host_hiu_addr[13] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | F3 |
| 17 | pci_ad[29] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | F3 |
| 18 | host_hiu_addr[12] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | F2 |
| 18 | pci_ad[28] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | F2 |
| 19 | host_hiu_addr[11] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | F1 |
| 19 | pci_ad[27] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | F1 |
| 20 | host_hiu_addr[10] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | H5 |
| 20 | pci_ad[26] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | H5 |
| 21 | host_hiu_addr[ 9] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | H4 |
| 21 | pci_ad[25] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | H4 |
| 22 | hiu_host_cdo_req_ | HIU / Moto | Compressed data out request | Bi-Dir | PCI | Tri-state | G3 |
| 22 | intel_cdo_req_ | HIU / Intel | Compressed data out request | Bi-Dir | PCI | Tri-state | G3 |
| 22 | pci_cbe_[3] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | G3 |
| 23 | pci_idsel | HIU / PCI | PCI init. device select | Input | PCI | | G2 |
| 24 | host_hiu_addr[ 8] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | G1 |
| 24 | pci_ad[24] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | G1 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 25 | host_hiu_addr[ 7] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | J4 |
| 25 | pci_ad[23] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | J4 |
| 26 | host_hiu_addr[ 6] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | H3 |
| 26 | pci_ad[22] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | H3 |
| 27 | host_hiu_addr[ 5] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | H2 |
| 27 | pci_ad[21] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | H2 |
| 28 | host_hiu_addr[ 4] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | H1 |
| 28 | pci_ad[20] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | H1 |
| 29 | host_hiu_addr[ 3] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | J5 |
| 29 | pci_ad[19] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | J5 |
| 30 | host_hiu_addr[ 2] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | J3 |
| 30 | pci_ad[18] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | J3 |
| 31 | host_hiu_addr[ 1] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | J2 |
| 31 | pci_ad[17] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | J2 |
| 32 | host_hiu_rw_ | HIU / Moto | Host read/write | Bi-Dir | PCI | Tri-state | J1 |
| 32 | intel_wr_ | HIU / Intel | Host write | Bi-Dir | PCI | Tri-state | J1 |
| 32 | pci_cbe_[2] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | J1 |
| 33 | intel_rd_ | HIU / Intel | Host read | Bi-Dir | PCI | Tri-state | K4 |
| 33 | pci_frame_ | HIU / PCI | PCI cycle frame / transaction | Bi-Dir | PCI | Tri-state | K4 |
| 34 | pci_irdy_ | HIU / PCI | PCI initiator ready | Bi-Dir | PCI | Tri-state | K3 |
| 35 | pci_trdy_ | HIU / PCI | PCI target ready | Bi-Dir | PCI | Tri-state | K2 |
| 36 | host_hiu_cdi_ack_ | HIU / Moto | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | K1 |
| 36 | intel_cdi_ack_ | HIU / Intel | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | K1 |
| 36 | pci_devsel_ | HIU / PCI | PCI device select | Bi-Dir | PCI | Tri-state | K1 |
| 37 | hiu_host_cdi_req_ | HIU / Moto | Host CDI request | Bi-Dir | PCI | Tri-state | K5 |
| 37 | intel_cdi_req_ | HIU / Intel | Host CDI request | Bi-Dir | PCI | Tri-state | K5 |
| 37 | pci_stop_ | HIU / PCI | PCI stop transaction | Bi-Dir | PCI | Tri-state | K5 |
| 38 | pci_gnt_ | HIU / PCI | PCI grant | Input | PCI | Tri-state | L3 |
| 39 | host_hiu_cdo_ack_ | HIU / Moto | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | L2 |
| 39 | intel_cdo_ack_ | HIU / Intel | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | L2 |
| 39 | pci_perr_ | HIU / PCI | PCI parity error | Bi-Dir | PCI | Tri-state | L2 |
| 40 | hiu_host_dtack_ | HIU / Moto | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | L1 |
| 40 | intel_dtack_ | HIU / Intel | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | L1 |
| 40 | pci_serr_ | HIU / PCI | PCI system error | Bi-Dir | PCI | Open-drain | L1 |
| 41 | pci_par | HIU / PCI | PCI parity | Bi-Dir | PCI | Tri-state | L4 |
| 42 | host_hiu_cs_ | HIU / Moto | Host chip select | Bi-Dir | PCI | Tri-state | M1 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 42 | intel_cs_ | HIU / Intel | Host chip select | Bi-Dir | PCI | Tri-state | M1 |
| 42 | pci_cbe_[1] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | M1 |
| 43 | host_hiu_addr[ 0] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | M2 |
| 43 | pci_ad[16] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | M2 |
| 44 | host_hiu_data[15] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | M3 |
| 44 | intel_ad[15] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | M3 |
| 44 | pci_ad[15] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | M3 |
| 45 | host_hiu_data[14] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | L5 |
| 45 | intel_ad[14] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | L5 |
| 45 | pci_ad[14] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | L5 |
| 46 | host_hiu_data[13] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | N1 |
| 46 | intel_ad[13] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | N1 |
| 46 | pci_ad[13] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | N1 |
| 47 | host_hiu_data[12] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | N2 |
| 47 | intel_ad[12] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | N2 |
| 47 | pci_ad[12] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | N2 |
| 48 | host_hiu_data[11] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | N3 |
| 48 | intel_ad[11] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | N3 |
| 48 | pci_ad[11] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | N3 |
| 49 | host_hiu_data[10] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | M4 |
| 49 | intel_ad[10] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | M4 |
| 49 | pci_ad[10] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | M4 |
| 50 | host_hiu_data[ 9] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | P1 |
| 50 | intel_ad[ 9] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | P1 |
| 50 | pci_ad[ 9] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | P1 |
| 51 | host_hiu_data[ 8] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | P2 |
| 51 | intel_ad[ 8] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | P2 |
| 51 | pci_ad[ 8] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | P2 |
| 52 | host_hiu_as_ | HIU / Moto | Host address select | Bi-Dir | PCI | Tri-state | P3 |
| 52 | intel_as_ale_ | HIU / Intel | Host address select / address latch enable | Bi-Dir | PCI | Tri-state | P3 |
| 52 | pci_cbe_[0] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | P3 |
| 53 | host_hiu_data[ 7] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | M5 |
| 53 | intel_ad[ 7] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | M5 |
| 53 | pci_ad[ 7] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | M5 |
| 54 | host_hiu_data[ 6] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | R1 |
| 54 | intel_ad[ 6] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | R1 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 54 | pci_ad[ 6] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | R1 |
| 55 | host_hiu_data[ 5] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | R2 |
| 55 | intel_ad[ 5] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | R2 |
| 55 | pci_ad[ 5] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | R2 |
| 56 | host_hiu_data[ 4] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | T1 |
| 56 | intel_ad[ 4] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | T1 |
| 56 | pci_ad[ 4] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | T1 |
| 57 | host_hiu_data[ 3] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | N4 |
| 57 | intel_ad[ 3] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | N4 |
| 57 | pci_ad[ 3] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | N4 |
| 58 | host_hiu_data[ 2] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | R3 |
| 58 | intel_ad[ 2] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | R3 |
| 58 | pci_ad[ 2] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | R3 |
| 59 | host_hiu_data[ 1] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | N5 |
| 59 | intel_ad[ 1] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | N5 |
| 59 | pci_ad[ 1] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | N5 |
| 60 | host_hiu_data[ 0] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | T2 |
| 60 | intel_ad[ 0] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | T2 |
| 60 | pci_ad[ 0] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | T2 |
| 61 | trst_ | JTAG | Test reset | Input | | Pull-down | P4 |
| 62 | tms | JTAG | Test mode select | Input | | Pull-up | U1 |
| 63 | tck | JTAG | Test clock | Input | | Pull-up | V1 |
| 64 | tdi | JTAG | Test data in | Input | | Pull-up | T3 |
| 65 | tdo | JTAG | Test data out | Output | 4 | Pull-up/ tri-state | R4 |
| 66 | ejtag_dclk | EJTAG | Debug clock | Output | 8 | | P5 |
| 67 | ejtag_pcst2[0] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | U2 |
| 68 | PLL_clock | mPLL | Main PLL clock | Input | | | W1 |
| 69 | PLL_bypass | mPLL | Main PLL disable / bypass | Input | | | T4 |
| 76 | ejtag_pcst2[1] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | T6 |
| 77 | ejtag_pcst2[2] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | V3 |
| 78 | ejtag_pcst[0] | EJTAG | Program counter status trace[2:0] | Output | 8 | | Y1 |
| 79 | ejtag_pcst[1] | EJTAG | Program counter status trace[2:0] | Output | 8 | | Y2 |
| 80 | ejtag_pcst[2] | EJTAG | Program counter status trace[2:0] | Output | 8 | | W3 |
| 81 | sdram_dec_data[31] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V4 |
| 82 | sdram_dec_data[30] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y3 |
| 83 | sdram_dec_data[29] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W4 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 84 | sdram_dec_data[28] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U5 |
| 85 | sdram_dec_data[27] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V5 |
| 86 | sdram_dec_data[26] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y4 |
| 87 | sdram_dec_data[25] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W5 |
| 88 | sdram_dec_data[24] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U6 |
| 89 | sdram_dec_data[23] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y5 |
| 90 | sdram_dec_data[22] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U7 |
| 91 | sdram_dec_data[21] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T7 |
| 92 | sdram_dec_data[20] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V6 |
| 93 | sdram_dec_data[19] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W6 |
| 94 | sdram_dec_data[18] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y6 |
| 95 | sdram_dec_data[17] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T8 |
| 96 | sdram_dec_data[16] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U8 |
| 97 | sdram_dec_data[15] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V7 |
| 98 | sdram_dec_data[14] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W7 |
| 99 | sdram_dec_data[13] | DMIU | Decoder DRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y7 |
| 100 | sdram_dec_data[12] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U9 |
| 101 | sdram_dec_data[11] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V8 |
| 102 | sdram_dec_data[10] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W8 |
| 103 | sdram_dec_data[ 9] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y8 |
| 104 | sdram_dec_data[ 8] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T9 |
| 105 | sdram_dec_data[ 7] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V9 |
| 106 | sdram_dec_data[ 6] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W9 |
| 107 | sdram_dec_data[ 5] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y9 |
| 108 | sdram_dec_data[ 4] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U10 |
| 109 | sdram_dec_data[ 3] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V10 |
| 110 | sdram_dec_data[ 2] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W10 |
| 111 | sdram_dec_data[ 1] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y10 |
| 112 | sdram_dec_data[ 0] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T10 |
| 113 | sdram_dec_addr[10] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | V11 |
| 114 | sdram_dec_addr[ 0] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | W11 |
| 115 | sdram_dec_addr[ 9] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | Y11 |
| 116 | sdram_dec_addr[ 1] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | U11 |
| 117 | sdram_dec_addr[ 8] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | Y12 |
| 118 | sdram_dec_addr[ 2] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | W12 |
| 119 | sdram_dec_addr[ 7] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | V12 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 120 | sdram_dec_addr[ 3] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | T11 |
| 121 | sdram_dec_addr[ 6] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | Y13 |
| 122 | sdram_dec_addr[ 4] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | W13 |
| 123 | sdram_dec_addr[ 5] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | V13 |
| 124 | sdram_dec_ba[0] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | U12 |
| 125 | sdram_dec_we_ | DMIU | Decoder SDRAM write enable | Output | 8 | Slew rate cont. | Y14 |
| 126 | sdram_dec_cke | DMIU | Decoder SDRAM clock enable | Output | 8 | Slew rate cont. | W14 |
| 127 | sdram_dec_clk | DMIU | Decoder SDRAM clock | Bi-Dir | 24 | | V14 |
| 128 | sdram_dec_cs_ | DMIU | Decoder SDRAM chip select | Output | 8 | Slew rate cont. | T12 |
| 129 | sdram_dec_dqm[0] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | Y15 |
| 130 | sdram_dec_dqm[1] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | W15 |
| 131 | sdram_dec_dqm[2] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | Y16 |
| 132 | sdram_dec_dqm[3] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | U13 |
| 133 | sdram_dec_ras_ | DMIU | Decoder SDRAM row address strobe | Output | 8 | Slew rate cont. | V15 |
| 135 | sdram_dec_cas_ | DMIU | Decoder SDRAM column address strobe | Output | 8 | Slew rate cont. | W16 |
| 136 | scl | ICI | ICI clock | Bi-Dir | 4 | Schmitt trig. | U14 |
| 137 | sda | ICI | ICI data | Bi-Dir | 4 | Schmitt trig. | Y17 |
| 138 | sdram_dec_ba[1] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | Y18 |
| 139 | pio[11] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | V16 |
| 140 | pio[10] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | U15 |
| 142 | pio[ 9] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | W17 |
| 143 | pio[ 8] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | Y19 |
| 144 | pio[ 7] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | U16 |
| 145 | pio[ 6] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | V17 |
| 146 | pio[ 5] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | W18 |
| 147 | pio[ 4] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | T15 |
| 148 | pio[ 3] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | W19 |
| 149 | pio[ 2] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | U17 |
| 150 | pio[ 1] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | T16 |
| 151 | pio[ 0] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | V18 |
| 152 | sdram_enc_data[31] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | Y20 |
| 153 | sdram_enc_data[30] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | W20 |
| 154 | sdram_enc_data[29] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V19 |
| 155 | sdram_enc_data[28] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U18 |
| 156 | sdram_enc_data[27] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | V20 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 157 | sdram_enc_data[26] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U19 |
| 158 | sdram_enc_data[25] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T17 |
| 159 | sdram_enc_data[24] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T18 |
| 160 | sdram_enc_data[23] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | U20 |
| 161 | sdram_enc_data[22] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T19 |
| 162 | sdram_enc_data[21] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | R17 |
| 163 | sdram_enc_data[20] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | T20 |
| 164 | sdram_enc_data[19] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | R16 |
| 166 | sdram_enc_data[18] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | P17 |
| 167 | sdram_enc_data[17] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | R18 |
| 168 | sdram_enc_data[16] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | R19 |
| 169 | sdram_enc_data[15] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | R20 |
| 170 | sdram_enc_data[14] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | N17 |
| 171 | sdram_enc_data[13] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | N16 |
| 172 | sdram_enc_data[12] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | P18 |
| 173 | sdram_enc_data[11] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | P19 |
| 174 | sdram_enc_data[10] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | P20 |
| 175 | sdram_enc_data[ 9] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | M17 |
| 176 | sdram_enc_data[ 8] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | N18 |
| 177 | sdram_enc_data[ 7] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | N19 |
| 178 | sdram_enc_data[ 6] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | N20 |
| 179 | sdram_enc_data[ 5] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | M16 |
| 180 | sdram_enc_data[ 4] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | M18 |
| 181 | sdram_enc_data[ 3] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | M19 |
| 182 | sdram_enc_data[ 2] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | M20 |
| 183 | sdram_enc_data[ 1] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | L17 |
| 184 | sdram_enc_data[ 0] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | L18 |
| 185 | sdram_enc_clk | EMIU | Encoder SDRAM clock | Bi-Dir | 24 | | L19 |
| 186 | sdram_enc_cke | EMIU | Encoder SDRAM clock enable | Output | 8 | Slew rate cont. | L20 |
| 187 | sdram_enc_cs_ | EMIU | Encoder SDRAM chip select | Output | 8 | Slew rate cont. | L16 |
| 188 | sdram_enc_dqm[0] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | K18 |
| 189 | sdram_enc_dqm[1] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | K19 |
| 190 | sdram_enc_dqm[2] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | K20 |
| 191 | sdram_enc_dqm[3] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | K17 |
| 192 | sdram_enc_addr[10] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | J20 |
| 193 | sdram_enc_addr[ 0] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | J19 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 194 | sdram_enc_addr[ 9] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | J18 |
| 195 | sdram_enc_addr[ 1] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | K16 |
| 196 | sdram_enc_addr[ 8] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | H20 |
| 197 | sdram_enc_addr[ 2] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | H19 |
| 198 | sdram_enc_addr[ 7] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | H18 |
| 199 | sdram_enc_addr[ 3] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | J17 |
| 200 | sdram_enc_addr[ 6] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | G20 |
| 201 | sdram_enc_addr[ 4] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | G19 |
| 202 | sdram_enc_addr[ 5] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | G18 |
| 203 | vbi_data[7] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | J16 |
| 204 | vbi_data[6] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | F20 |
| 205 | ejtag_pcst4[2] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | F19 |
| 205 | vbi_data[5] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | F19 |
| 206 | ejtag_pcst4[1] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | H17 |
| 206 | vbi_data[4] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | H17 |
| 207 | ejtag_pcst4[0] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | E20 |
| 207 | vbi_data[3] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | E20 |
| 208 | ejtag_pcst3[2] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | H16 |
| 208 | vbi_data[2] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | H16 |
| 209 | ejtag_pcst3[1] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | F18 |
| 209 | vbi_data[1] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | F18 |
| 210 | ejtag_pcst3[0] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | E19 |
| 210 | vbi_data[0] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | E19 |
| 211 | vbi_data_en | VIU | VBI data enable | Input | | Pull-up | G17 |
| 212 | amclk_enc | AIU | Audio in master clock | Output | 8 | | D20 |
| 213 | PLL_amclk_enc | AIU | External audio in master clock | Input | | | C20 |
| 226 | clk_vbi | VIU | External VBI clock 27 MHz | Input | | Pull-up | E15 |
| 227 | sdram_enc_ras_ | EMIU | Encoder SDRAM row address strobe | Output | 8 | Slew rate cont. | C18 |
| 228 | sdram_enc_cas_ | EMIU | Encoder SDRAM column address strobe | Output | 8 | Slew rate cont. | A20 |
| 229 | sdram_enc_ba[0] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | A19 |
| 230 | sdram_enc_ba[1] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | B18 |
| 231 | sdram_enc_we_ | EMIU | Encoder SDRAM write enable | Output | 8 | Slew rate cont. | C17 |
| 232 | cdo[7] | Mux | Compressed data out [7:0] | Output | 8 | | A18 |
| 232 | rom_addr[19] | ROM | ROM address [21:0] | Output | 8 | | A18 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 233 | cdo[6] | Mux | Compressed data out [7:0] | Output | 8 | | B17 |
| 233 | rom_addr[18] | ROM | ROM address [21:0] | Output | 8 | | B17 |
| 234 | cdo[5] | Mux | Compressed data out [7:0] | Output | 8 | | D16 |
| 234 | rom_addr[17] | ROM | ROM address [21:0] | Output | 8 | | D16 |
| 235 | cdo[4] | Mux | Compressed data out [7:0] | Output | 8 | | C16 |
| 235 | rom_addr[16] | ROM | ROM address [21:0] | Output | 8 | | C16 |
| 236 | cdo[3] | Mux | Compressed data out [7:0] | Output | 8 | | A17 |
| 236 | rom_addr[15] | ROM | ROM address [21:0] | Output | 8 | | A17 |
| 237 | cdo[2] | Mux | Compressed data out [7:0] | Output | 8 | | B16 |
| 237 | rom_addr[14] | ROM | ROM address [21:0] | Output | 8 | | B16 |
| 238 | cdo[1] | Mux | Compressed data out [7:0] | Output | 8 | | D15 |
| 238 | rom_addr[13] | ROM | ROM address [21:0] | Output | 8 | | D15 |
| 239 | cdo[0] | Mux | Compressed data out [7:0] | Output | 8 | | A16 |
| 239 | rom_addr[12] | ROM | ROM address [21:0] | Output | 8 | | A16 |
| 240 | cdo_clk | Mux | Compressed data out clock | Output | 8 | | D14 |
| 240 | rom_addr[11] | ROM | ROM address [21:0] | Output | 8 | | D14 |
| 242 | cdo_sop | Mux | Compressed data start of packet | Output | 8 | | C15 |
| 242 | rom_addr[10] | ROM | ROM address [21:0] | Output | 8 | | C15 |
| 243 | excd_clk | Mux | External compressed data clock | Input | | Pull-down | B15 |
| 244 | excd_rd | Mux | External compressed data read | Input | | Pull-up | A15 |
| 246 | cdo_valid | Mux | Compressed data out valid | Output | 8 | | D13 |
| 246 | rom_addr[ 9] | ROM | ROM address [21:0] | Output | 8 | | D13 |
| 247 | fifo_level | Mux | Mux FIFO level | Output | 8 | | C14 |
| 247 | rom_addr[ 8] | ROM | ROM address [21:0] | Output | 8 | | C14 |
| 248 | sd0_enc | AIU | $I^2S$ Audio in channel 1 | Input | | Pull-up | B14 |
| 249 | sd1_enc | AIU | $I^2S$ Audio in channel 2 | Input | | Pull-up | A14 |
| 250 | sck_enc | AIU | $I^2S$ Audio in clock | Bi-Dir | 8 | Pull-up | D12 |
| 251 | ws_enc | AIU | $I^2S$ Audio in channel select | Bi-Dir | 8 | Pull-up | C13 |
| 252 | vpo[7] | VIU | Video input data [7:0] | Input | | | B13 |
| 253 | vpo[6] | VIU | Video input data [7:0] | Input | | | A13 |
| 254 | vpo[5] | VIU | Video input data [7:0] | Input | | | E12 |
| 255 | vpo[4] | VIU | Video input data [7:0] | Input | | | C12 |
| 256 | vpo[3] | VIU | Video input data [7:0] | Input | | | B12 |
| 257 | vpo[2] | VIU | Video input data [7:0] | Input | | | A12 |
| 258 | vpo[1] | VIU | Video input data [7:0] | Input | | | D11 |
| 259 | vpo[0] | VIU | Video input data [7:0] | Input | | | C11 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 260 | clk_27 | VIU | Video input clock 27 MHz | Input | | | A11 |
| 261 | pcr_clk | Chip | PCR clock | Input | | | E11 |
| 262 | reset_ | Chip | Global reset | Input | | Schmitt trig. | B11 |
| 263 | rom_data[7] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | A10 |
| 264 | rom_data[6] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | B10 |
| 265 | rom_data[5] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | A9 |
| 266 | rom_data[4] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | D10 |
| 267 | rom_data[3] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | C10 |
| 268 | rom_data[2] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | B9 |
| 269 | rom_data[1] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | E10 |
| 270 | rom_data[0] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | A8 |
| 271 | vou_clk | VOU | Video output clock 27 MHz | Output | 8 | | A7 |
| 272 | rom_addr[ 7] | ROM | ROM address [21:0] | Output | 8 | | C9 |
| 272 | vou_vpo[7] | VOU | Video output data [7:0] | Output | 8 | | C9 |
| 273 | rom_addr[ 6] | ROM | ROM address [21:0] | Output | 8 | | B8 |
| 273 | vou_vpo[6] | VOU | Video output data [7:0] | Output | 8 | | B8 |
| 274 | rom_addr[ 5] | ROM | ROM address [21:0] | Output | 8 | | D9 |
| 274 | vou_vpo[5] | VOU | Video output data [7:0] | Output | 8 | | D9 |
| 275 | rom_addr[ 4] | ROM | ROM address [21:0] | Output | 8 | | A6 |
| 275 | vou_vpo[4] | VOU | Video output data [7:0] | Output | 8 | | A6 |
| 276 | rom_addr[ 3] | ROM | ROM address [21:0] | Output | 8 | | E9 |
| 276 | vou_vpo[3] | VOU | Video output data [7:0] | Output | 8 | | E9 |
| 277 | rom_addr[ 2] | ROM | ROM address [21:0] | Output | 8 | | B7 |
| 277 | vou_vpo[2] | VOU | Video output data [7:0] | Output | 8 | | B7 |
| 278 | rom_ce_ | ROM | ROM chip enable | Output | 8 | | C7 |
| 279 | rom_addr[ 1] | ROM | ROM address [21:0] | Output | 8 | | D8 |
| 279 | vou_vpo[1] | VOU | Video output data [7:0] | Output | 8 | | D8 |
| 280 | rom_addr[ 0] | ROM | ROM address [21:0] | Output | 8 | | C8 |
| 280 | vou_vpo[0] | VOU | Video output data [7:0] | Output | 8 | | C8 |
| 281 | rom_oe_ | ROM | ROM output enable | Output | 8 | | A5 |
| 281 | ws_dec | AOU | Audio out channel select | Output | 8 | | A5 |
| 282 | rom_we_ | ROM | ROM write enable | Output | 8 | | B6 |
| 282 | sck_dec | AOU | Audio out clock | Output | 8 | | B6 |
| 284 | rom_addr[21] | ROM | ROM address [21:0] | Output | 8 | | B5 |
| 284 | sd0_dec | AOU | Audio out channel 1 - $I^2S$ | Output | 8 | | B5 |

**Table 9 I/O Signals, Sorted by Pad Number (Continued)**

| Pad No. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Ball Coord. |
|---|---|---|---|---|---|---|---|
| 285 | rom_addr[20] | ROM | ROM address [21:0] | Output | 8 | | C6 |
| 285 | sd1_dec | AOU | Audio out channel 2 - S/P-DIF | Output | 8 | | C6 |
| 286 | amclk_dec | AOU | Audio out master clock | Output | 8 | | A4 |
| 300 | PLL_amclk_dec | AOU | External audio out master clock | Input | | | A1 |

### Table 10 I/O Signals, Sorted by BGA Coordinates

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| A1 | PLL_amclk_dec | AOU | External audio out master clock | Input | | | 300 |
| A4 | amclk_dec | AOU | Audio out master clock | Output | 8 | | 286 |
| A5 | rom_oe_ | ROM | ROM output enable | Output | 8 | | 281 |
| A5 | ws_dec | AOU | Audio out channel select | Output | 8 | | 281 |
| A6 | rom_addr[4] | ROM | ROM address [21:0] | Output | 8 | | 275 |
| A6 | vou_vpo[4] | VOU | Video output data [7:0] | Output | 8 | | 275 |
| A7 | vou_clk | VOU | Video output clock 27 MHz | Output | 8 | | 271 |
| A8 | rom_data[0] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 270 |
| A9 | rom_data[5] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 265 |
| A10 | rom_data[7] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 263 |
| A11 | clk_27 | VIU | Video input clock 27 MHz | Input | | | 260 |
| A12 | vpo[2] | VIU | Video input data [7:0] | Input | | | 257 |
| A13 | vpo[6] | VIU | Video input data [7:0] | Input | | | 253 |
| A14 | sd1_enc | AIU | $I^2S$ Audio in channel 2 | Input | | Pull-up | 249 |
| A15 | excd_rd | Mux | External compressed data read | Input | | Pull-up | 244 |
| A16 | cdo[0] | Mux | Compressed data out [7:0] | Output | 8 | | 239 |
| A16 | rom_addr[12] | ROM | ROM address [21:0] | Output | 8 | | 239 |
| A17 | cdo[3] | Mux | Compressed data out [7:0] | Output | 8 | | 236 |
| A17 | rom_addr[15] | ROM | ROM address [21:0] | Output | 8 | | 236 |
| A18 | cdo[7] | Mux | Compressed data out [7:0] | Output | 8 | | 232 |
| A18 | rom_addr[19] | ROM | ROM address [21:0] | Output | 8 | | 232 |
| A19 | sdram_enc_ba[0] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 229 |
| A20 | sdram_enc_cas_ | EMIU | Encoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 228 |
| B1 | cdi[5] | Demux | Compressed data in [7:0] | Input | | Pull-up | 3 |
| B5 | rom_addr[21] | ROM | ROM address [21:0] | Output | 8 | | 284 |
| B5 | sd0_dec | AOU | Audio out channel 1 - $I^2S$ | Output | 8 | | 284 |
| B6 | rom_we_ | ROM | ROM write enable | Output | 8 | | 282 |
| B6 | sck_dec | AOU | Audio out clock | Output | 8 | | 282 |
| B7 | rom_addr[2] | ROM | ROM address [21:0] | Output | 8 | | 277 |
| B7 | vou_vpo[2] | VOU | Video output data [7:0] | Output | 8 | | 277 |
| B8 | rom_addr[6] | ROM | ROM address [21:0] | Output | 8 | | 273 |
| B8 | vou_vpo[6] | VOU | Video output data [7:0] | Output | 8 | | 273 |
| B9 | rom_data[2] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 268 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| B10 | rom_data[6] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 264 |
| B11 | reset_ | Chip | Global reset | Input | | Schmitt trig. | 262 |
| B12 | vpo[3] | VIU | Video input data [7:0] | Input | | | 256 |
| B13 | vpo[7] | VIU | Video input data [7:0] | Input | | | 252 |
| B14 | sd0_enc | AIU | $I^2S$ Audio in channel 1 | Input | | Pull-up | 248 |
| B15 | excd_clk | Mux | External compressed data clock | Input | | Pull-down | 243 |
| B16 | cdo[2] | Mux | Compressed data out [7:0] | Output | 8 | | 237 |
| B16 | rom_addr[14] | ROM | ROM address [21:0] | Output | 8 | | 237 |
| B17 | cdo[6] | Mux | Compressed data out [7:0] | Output | 8 | | 233 |
| B17 | rom_addr[18] | ROM | ROM address [21:0] | Output | 8 | | 233 |
| B18 | sdram_enc_ba[1] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 230 |
| C1 | cdi[3] | Demux | Compressed data in [7:0] | Input | | Pull-up | 5 |
| C2 | cdi[4] | Demux | Compressed data in [7:0] | Input | | Pull-up | 4 |
| C3 | cdi[6] | Demux | Compressed data in [7:0] | Input | | Pull-up | 2 |
| C6 | rom_addr[20] | ROM | ROM address [21:0] | Output | 8 | | 285 |
| C6 | sd1_dec | AOU | Audio out channel 2 - S/P-DIF | Output | 8 | | 285 |
| C7 | rom_ce_ | ROM | ROM chip enable | Output | 8 | | 278 |
| C8 | rom_addr[0] | ROM | ROM address [21:0] | Output | 8 | | 280 |
| C8 | vou_vpo[0] | VOU | Video output data [7:0] | Output | 8 | | 280 |
| C9 | rom_addr[7] | ROM | ROM address [21:0] | Output | 8 | | 272 |
| C9 | vou_vpo[7] | VOU | Video output data [7:0] | Output | 8 | | 272 |
| C10 | ejtag_enable | EJTAG | Enable EJTAG ports | Bi-Dir | 4 | Pull-up | 267 |
| C10 | rom_data[3] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 267 |
| C11 | vpo[0] | VIU | Video input data [7:0] | Input | | | 259 |
| C12 | vpo[4] | VIU | Video input data [7:0] | Input | | | 255 |
| C13 | ws_enc | AIU | $I^2S$ Audio in channel select | Bi-Dir | 8 | Pull-up | 251 |
| C14 | fifo_level | Mux | Mux FIFO level | Output | 8 | | 247 |
| C14 | rom_addr[8] | ROM | ROM address [21:0] | Output | 8 | | 247 |
| C15 | cdo_sop | Mux | Compressed data start of packet | Output | 8 | | 242 |
| C15 | rom_addr[10] | ROM | ROM address [21:0] | Output | 8 | | 242 |
| C16 | cdo[4] | Mux | Compressed data out [7:0] | Output | 8 | | 235 |
| C16 | rom_addr[16] | ROM | ROM address [21:0] | Output | 8 | | 235 |
| C17 | sdram_enc_we_ | EMIU | Encoder SDRAM write enable | Output | 8 | Slew rate cont. | 231 |
| C18 | sdram_enc_ras_ | EMIU | Encoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 227 |
| C20 | PLL_amclk_enc | AIU | External audio in master clock | Input | | | 213 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| D1 | cdi[1] | Demux | Compressed data in [7:0] | Input | | Pull-up | 7 |
| D2 | cdi[2] | Demux | Compressed data in [7:0] | Input | | Pull-up | 6 |
| D3 | cdi[0] | Demux | Compressed data in [7:0] | Input | | Pull-up | 8 |
| D4 | cdi[7] | Demux | Compressed data in [7:0] | Input | | Pull-up | 1 |
| D8 | rom_addr[1] | ROM | ROM address [21:0] | Output | 8 | | 279 |
| D8 | vou_vpo[1] | VOU | Video output data [7:0] | Output | 8 | | 279 |
| D9 | rom_addr[5] | ROM | ROM address [21:0] | Output | 8 | | 274 |
| D9 | vou_vpo[5] | VOU | Video output data [7:0] | Output | 8 | | 274 |
| D10 | rom_data[4] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 266 |
| D11 | vpo[1] | VIU | Video input data [7:0] | Input | | | 258 |
| D12 | sck_enc | AIU | $I^2S$ Audio in clock | Bi-Dir | 8 | Pull-up | 250 |
| D13 | cdo_valid | Mux | Compressed data out valid | Output | 8 | | 246 |
| D13 | rom_addr[9] | ROM | ROM address [21:0] | Output | 8 | | 246 |
| D14 | cdo_clk | Mux | Compressed data out clock | Output | 8 | | 240 |
| D14 | rom_addr[11] | ROM | ROM address [21:0] | Output | 8 | | 240 |
| D15 | cdo[1] | Mux | Compressed data out [7:0] | Output | 8 | | 238 |
| D15 | rom_addr[13] | ROM | ROM address [21:0] | Output | 8 | | 238 |
| D16 | cdo[5] | Mux | Compressed data out [7:0] | Output | 8 | | 234 |
| D16 | rom_addr[17] | ROM | ROM address [21:0] | Output | 8 | | 234 |
| D20 | amclk_enc | AIU | Audio in master clock | Output | 8 | | 212 |
| E1 | pci_req_ | HIU / PCI | PCI bus request | Bi-Dir | PCI | Tri-state | 13 |
| E2 | pci_clk | HIU / PCI | PCI clock | Input | PCI | | 12 |
| E3 | int_ | HIU / Moto | Host interrupt | Output | PCI | Open-drain | 11 |
| E3 | int_ | HIU / Intel | Host interrupt | Output | PCI | Open-drain | 11 |
| E3 | pci_inta_ | HIU / PCI | PCI interrupt A | Output | PCI | Open-drain | 11 |
| E4 | cdi_valid | Demux | Compressed data in enable | Input | | Pull-up | 9 |
| E9 | rom_addr[3] | ROM | ROM address [21:0] | Output | 8 | | 276 |
| E9 | vou_vpo[3] | VOU | Video output data [7:0] | Output | 8 | | 276 |
| E10 | rom_data[1] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 269 |
| E11 | pcr_clk | Chip | PCR clock | Input | | | 261 |
| E12 | vpo[5] | VIU | Video input data [7:0] | Input | | | 254 |
| E15 | clk_vbi | VIU | External VBI clock 27 MHz | Input | | Pull-up | 226 |
| E19 | ejtag_pcst3[0] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 210 |
| E19 | vbi_data[0] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 210 |
| E20 | ejtag_pcst4[0] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 207 |
| E20 | vbi_data[3] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 207 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| F1 | host_hiu_addr[11] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 19 |
| F1 | pci_ad[27] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 19 |
| F2 | host_hiu_addr[12] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 18 |
| F2 | pci_ad[28] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 18 |
| F3 | host_hiu_addr[13] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 17 |
| F3 | pci_ad[29] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 17 |
| F4 | cdi_clk | Demux | Compressed data in clock | Input | | Pull-up | 10 |
| F18 | ejtag_pcst3[1] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 209 |
| F18 | vbi_data[1] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 209 |
| F19 | ejtag_pcst4[2] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 205 |
| F19 | vbi_data[5] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 205 |
| F20 | vbi_data[6] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 204 |
| G1 | host_hiu_addr[8] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 24 |
| G1 | pci_ad[24] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 24 |
| G2 | pci_idsel | HIU / PCI | PCI init. device select | Input | PCI | | 23 |
| G3 | hiu_host_cdo_req_ | HIU / Moto | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 |
| G3 | intel_cdo_req_ | HIU / Intel | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 |
| G3 | pci_cbe_[3] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 22 |
| G4 | host_hiu_addr[14] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 16 |
| G4 | pci_ad[30] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 16 |
| G5 | host_hiu_addr[15] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 15 |
| G5 | pci_ad[31] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 15 |
| G17 | vbi_data_en | VIU | VBI data enable | Input | | Pull-up | 211 |
| G18 | sdram_enc_addr[5] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 202 |
| G19 | sdram_enc_addr[4] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 201 |
| G20 | sdram_enc_addr[6] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 200 |
| H1 | host_hiu_addr[4] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 28 |
| H1 | pci_ad[20] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 28 |
| H2 | host_hiu_addr[5] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 27 |
| H2 | pci_ad[21] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 27 |
| H3 | host_hiu_addr[6] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 26 |
| H3 | pci_ad[22] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 26 |
| H4 | host_hiu_addr[9] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 21 |
| H4 | pci_ad[25] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 21 |
| H5 | host_hiu_addr[10] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 20 |
| H5 | pci_ad[26] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 20 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| H16 | ejtag_pcst3[2] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 208 |
| H16 | vbi_data[2] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 208 |
| H17 | ejtag_pcst4[1] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 206 |
| H17 | vbi_data[4] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 206 |
| H18 | sdram_enc_addr[7] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 198 |
| H19 | sdram_enc_addr[2] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 197 |
| H20 | sdram_enc_addr[8] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 196 |
| J1 | host_hiu_rw_ | HIU / Moto | Host read/write | Bi-Dir | PCI | Tri-state | 32 |
| J1 | intel_wr_ | HIU / Intel | Host write | Bi-Dir | PCI | Tri-state | 32 |
| J1 | pci_cbe_[2] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 32 |
| J2 | host_hiu_addr[1] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 31 |
| J2 | pci_ad[17] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 31 |
| J3 | host_hiu_addr[2] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 30 |
| J3 | pci_ad[18] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 30 |
| J4 | host_hiu_addr[7] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 25 |
| J4 | pci_ad[23] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 25 |
| J5 | host_hiu_addr[3] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 29 |
| J5 | pci_ad[19] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 29 |
| J16 | vbi_data[7] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 203 |
| J17 | sdram_enc_addr[3] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 199 |
| J18 | sdram_enc_addr[9] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 194 |
| J19 | sdram_enc_addr[0] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 193 |
| J20 | sdram_enc_addr[10] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 192 |
| K1 | host_hiu_cdi_ack_ | HIU / Moto | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 |
| K1 | intel_cdi_ack_ | HIU / Intel | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 |
| K1 | pci_devsel_ | HIU / PCI | PCI device select | Bi-Dir | PCI | Tri-state | 36 |
| K2 | pci_trdy_ | HIU / PCI | PCI target ready | Bi-Dir | PCI | Tri-state | 35 |
| K3 | pci_irdy_ | HIU / PCI | PCI initiator ready | Bi-Dir | PCI | Tri-state | 34 |
| K4 | intel_rd_ | HIU / Intel | Host read | Bi-Dir | PCI | Tri-state | 33 |
| K4 | pci_frame_ | HIU / PCI | PCI cycle frame / transaction | Bi-Dir | PCI | Tri-state | 33 |
| K5 | hiu_host_cdi_req_ | HIU / Moto | Host CDI request | Bi-Dir | PCI | Tri-state | 37 |
| K5 | intel_cdi_req_ | HIU / Intel | Host CDI request | Bi-Dir | PCI | Tri-state | 37 |
| K5 | pci_stop_ | HIU / PCI | PCI stop transaction | Bi-Dir | PCI | Tri-state | 37 |
| K16 | sdram_enc_addr[1] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 195 |
| K17 | sdram_enc_dqm[3] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 191 |
| K18 | sdram_enc_dqm[0] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 188 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| K19 | sdram_enc_dqm[1] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 189 |
| K20 | sdram_enc_dqm[2] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 190 |
| L1 | hiu_host_dtack_ | HIU / Moto | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 |
| L1 | intel_dtack_ | HIU / Intel | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 |
| L1 | pci_serr_ | HIU / PCI | PCI system error | Bi-Dir | PCI | Open-drain | 40 |
| L2 | host_hiu_cdo_ack_ | HIU / Moto | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 |
| L2 | intel_cdo_ack_ | HIU / Intel | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 |
| L2 | pci_perr_ | HIU / PCI | PCI parity error | Bi-Dir | PCI | Tri-state | 39 |
| L3 | pci_gnt_ | HIU / PCI | PCI grant | Input | PCI | Tri-state | 38 |
| L4 | pci_par | HIU / PCI | PCI parity | Bi-Dir | PCI | Tri-state | 41 |
| L5 | host_hiu_data[14] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 45 |
| L5 | intel_ad[14] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 45 |
| L5 | pci_ad[14] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 45 |
| L16 | sdram_enc_cs_ | EMIU | Encoder SDRAM chip select | Output | 8 | Slew rate cont. | 187 |
| L17 | sdram_enc_data[1] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 183 |
| L18 | sdram_enc_data[0] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 184 |
| L19 | sdram_enc_clk | EMIU | Encoder SDRAM clock | Bi-Dir | 24 | | 185 |
| L20 | sdram_enc_cke | EMIU | Encoder SDRAM clock enable | Output | 8 | Slew rate cont. | 186 |
| M1 | host_hiu_cs_ | HIU / Moto | Host chip select | Bi-Dir | PCI | Tri-state | 42 |
| M1 | intel_cs_ | HIU / Intel | Host chip select | Bi-Dir | PCI | Tri-state | 42 |
| M1 | pci_cbe_[1] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 42 |
| M2 | host_hiu_addr[0] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 43 |
| M2 | pci_ad[16] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 43 |
| M3 | host_hiu_data[15] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 44 |
| M3 | intel_ad[15] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 44 |
| M3 | pci_ad[15] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 44 |
| M4 | host_hiu_data[10] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 49 |
| M4 | intel_ad[10] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 49 |
| M4 | pci_ad[10] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 49 |
| M5 | host_hiu_data[7] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 53 |
| M5 | intel_ad[7] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 53 |
| M5 | pci_ad[7] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 53 |
| M16 | sdram_enc_data[5] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 179 |
| M17 | sdram_enc_data[9] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 175 |
| M18 | sdram_enc_data[4] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 180 |
| M19 | sdram_enc_data[3] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 181 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| M20 | sdram_enc_data[2] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 182 |
| N1 | host_hiu_data[13] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 46 |
| N1 | intel_ad[13] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 46 |
| N1 | pci_ad[13] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 46 |
| N2 | host_hiu_data[12] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 47 |
| N2 | intel_ad[12] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 47 |
| N2 | pci_ad[12] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 47 |
| N3 | host_hiu_data[11] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 48 |
| N3 | intel_ad[11] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 48 |
| N3 | pci_ad[11] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 48 |
| N4 | host_hiu_data[3] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 57 |
| N4 | intel_ad[3] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 57 |
| N4 | pci_ad[3] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 57 |
| N5 | host_hiu_data[1] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 59 |
| N5 | intel_ad[1] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 59 |
| N5 | pci_ad[1] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 59 |
| N16 | sdram_enc_data[13] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 171 |
| N17 | sdram_enc_data[14] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 170 |
| N18 | sdram_enc_data[8] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 176 |
| N19 | sdram_enc_data[7] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 177 |
| N20 | sdram_enc_data[6] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 178 |
| P1 | host_hiu_data[9] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 50 |
| P1 | intel_ad[9] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 50 |
| P1 | pci_ad[9] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 50 |
| P2 | host_hiu_data[8] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 51 |
| P2 | intel_ad[8] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 51 |
| P2 | pci_ad[8] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 51 |
| P3 | host_hiu_as_ | HIU / Moto | Host address select | Bi-Dir | PCI | Tri-state | 52 |
| P3 | intel_as_ale_ | HIU / Intel | Host address select / address latch enable | Bi-Dir | PCI | Tri-state | 52 |
| P3 | pci_cbe_[0] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 52 |
| P4 | trst_ | JTAG | Test reset | Input | | Pull-down | 61 |
| P5 | ejtag_dclk | EJTAG | Debug clock | Output | 8 | | 66 |
| P17 | sdram_enc_data[18] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 166 |
| P18 | sdram_enc_data[12] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 172 |
| P19 | sdram_enc_data[11] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 173 |
| P20 | sdram_enc_data[10] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 174 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| R1 | host_hiu_data[6] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 54 |
| R1 | intel_ad[6] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 54 |
| R1 | pci_ad[6] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 54 |
| R2 | host_hiu_data[5] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 55 |
| R2 | intel_ad[5] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 55 |
| R2 | pci_ad[5] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 55 |
| R3 | host_hiu_data[2] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 58 |
| R3 | intel_ad[2] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 58 |
| R3 | pci_ad[2] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 58 |
| R4 | tdo | JTAG | Test data out | Output | 4 | Pull-up/ tri-state | 65 |
| R16 | sdram_enc_data[19] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 164 |
| R17 | sdram_enc_data[21] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 162 |
| R18 | sdram_enc_data[17] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 167 |
| R19 | sdram_enc_data[16] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 168 |
| R20 | sdram_enc_data[15] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 169 |
| T1 | host_hiu_data[4] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 56 |
| T1 | intel_ad[4] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 56 |
| T1 | pci_ad[4] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 56 |
| T2 | host_hiu_data[0] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 60 |
| T2 | intel_ad[0] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 60 |
| T2 | pci_ad[0] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 60 |
| T20 | sdram_enc_data[20] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 163 |
| T3 | tdi | JTAG | Test data in | Input | | Pull-up | 64 |
| T4 | PLL_bypass | mPLL | Main PLL disable / bypass | Input | | | 69 |
| T6 | ejtag_pcst2[1] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 76 |
| T7 | sdram_dec_data[21] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 91 |
| T8 | sdram_dec_data[17] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 95 |
| T9 | sdram_dec_data[8] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 104 |
| T10 | sdram_dec_data[0] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 112 |
| T11 | sdram_dec_addr[3] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 120 |
| T12 | sdram_dec_cs_ | DMIU | Decoder SDRAM chip select | Output | 8 | Slew rate cont. | 128 |
| T15 | pio[4] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 147 |
| T16 | pio[1] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 150 |
| T17 | sdram_enc_data[25] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 158 |
| T18 | sdram_enc_data[24] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 159 |
| T19 | sdram_enc_data[22] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 161 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| U1 | tms | JTAG | Test mode select | Input | | Pull-up | 62 |
| U2 | ejtag_pcst2[0] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 67 |
| U5 | sdram_dec_data[28] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 84 |
| U6 | sdram_dec_data[24] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 88 |
| U7 | sdram_dec_data[22] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 90 |
| U8 | sdram_dec_data[16] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 96 |
| U9 | sdram_dec_data[12] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 100 |
| U10 | sdram_dec_data[4] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 108 |
| U11 | sdram_dec_addr[1] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 116 |
| U12 | sdram_dec_ba[0] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 124 |
| U13 | sdram_dec_dqm[3] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 132 |
| U14 | scl | ICI | ICI clock | Bi-Dir | 4 | Schmitt trig. | 136 |
| U15 | host_pci_grant2 | HIU / Moto | Host bus grant | Bi-Dir | 8 | Pull-up | 140 |
| U15 | intel_pci_grant2 | HIU / Intel | Host bus grant | Bi-Dir | 8 | Pull-up | 140 |
| U15 | pio[10] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 140 |
| U16 | pio[7] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 144 |
| U17 | pio[2] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 149 |
| U18 | sdram_enc_data[28] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 155 |
| U19 | sdram_enc_data[26] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 157 |
| U20 | sdram_enc_data[23] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 160 |
| V1 | tck | JTAG | Test clock | Input | | Pull-up | 63 |
| V3 | ejtag_pcst2[2] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 77 |
| V4 | sdram_dec_data[31] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 81 |
| V5 | sdram_dec_data[27] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 85 |
| V6 | sdram_dec_data[20] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 92 |
| V7 | sdram_dec_data[15] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 97 |
| V8 | sdram_dec_data[11] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 101 |
| V9 | sdram_dec_data[7] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 105 |
| V10 | sdram_dec_data[3] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 109 |
| V11 | sdram_dec_addr[10] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 113 |
| V12 | sdram_dec_addr[7] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 119 |
| V13 | sdram_dec_addr[5] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 123 |
| V14 | sdram_dec_clk | DMIU | Decoder SDRAM clock | Bi-Dir | 24 | | 127 |
| V15 | sdram_dec_ras_ | DMIU | Decoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 133 |
| V16 | host_pci_req2 | HIU /Moto | Host bus request | Bi-Dir | 8 | Pull-up | 139 |
| V16 | intel_pci_req2 | HIU / Intel | Host bus request | Bi-Dir | 8 | Pull-up | 139 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| V16 | pio[11] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 139 |
| V17 | pio[6] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 145 |
| V18 | pio[0] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 151 |
| V19 | sdram_enc_data[29] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 154 |
| V20 | sdram_enc_data[27] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 156 |
| W1 | PLL_clock | mPLL | Main PLL clock | Input | | | 68 |
| W3 | ejtag_pcst[2] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 80 |
| W4 | sdram_dec_data[29] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 83 |
| W5 | sdram_dec_data[25] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 87 |
| W6 | sdram_dec_data[19] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 93 |
| W7 | sdram_dec_data[14] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 98 |
| W8 | sdram_dec_data[10] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 102 |
| W9 | sdram_dec_data[6] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 106 |
| W10 | sdram_dec_data[2] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 110 |
| W11 | sdram_dec_addr[0] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 114 |
| W12 | sdram_dec_addr[2] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 118 |
| W13 | sdram_dec_addr[4] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 122 |
| W14 | sdram_dec_cke | DMIU | Decoder SDRAM clock enable | Output | 8 | Slew rate cont. | 126 |
| W15 | sdram_dec_dqm[1] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 130 |
| W16 | sdram_dec_cas_ | DMIU | Decoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 135 |
| W17 | pio[9] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 142 |
| W18 | pio[5] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 146 |
| W19 | pio[3] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 148 |
| W20 | sdram_enc_data[30] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 153 |
| Y1 | ejtag_pcst[0] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 78 |
| Y2 | ejtag_pcst[1] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 79 |
| Y3 | sdram_dec_data[30] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 82 |
| Y4 | sdram_dec_data[26] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 86 |
| Y5 | sdram_dec_data[23] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 89 |
| Y6 | sdram_dec_data[18] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 94 |
| Y7 | sdram_dec_data[13] | DMIU | Decoder DRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 99 |
| Y8 | sdram_dec_data[9] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 103 |
| Y9 | sdram_dec_data[5] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 107 |
| Y10 | sdram_dec_data[1] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 111 |
| Y11 | sdram_dec_addr[9] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 115 |
| Y12 | sdram_dec_addr[8] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 117 |

**Table 10 I/O Signals, Sorted by BGA Coordinates (Continued)**

| Ball Coord. | Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. |
|---|---|---|---|---|---|---|---|
| Y13 | sdram_dec_addr[6] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 121 |
| Y14 | sdram_dec_we_ | DMIU | Decoder SDRAM write enable | Output | 8 | Slew rate cont. | 125 |
| Y15 | sdram_dec_dqm[0] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 129 |
| Y16 | sdram_dec_dqm[2] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 131 |
| Y17 | sda | ICI | ICI data | Bi-Dir | 4 | Schmitt trig. | 137 |
| Y18 | sdram_dec_ba[1] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 138 |
| Y19 | host_pci_int2 | HIU / Moto | Host bus interrupt | Bi-Dir | 8 | Pull-up | 143 |
| Y19 | intel_pci_int2 | HIU / Intel | Host bus interrupt | Bi-Dir | 8 | Pull-up | 143 |
| Y19 | pio[8] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 143 |
| Y20 | sdram_enc_data[31] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 152 |

**Table 11 I/O Signals, Sorted by Module**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| AIU | amclk_enc | Audio in master clock | Output | 8 | | 212 | D20 |
| AIU | PLL_amclk_enc | External audio in master clock | Input | | | 213 | C20 |
| AIU | sck_enc | $I^2S$ Audio in clock | Bi-Dir | 8 | Pull-up | 250 | D12 |
| AIU | sd0_enc | $I^2S$ Audio in channel 1 | Input | | Pull-up | 248 | B14 |
| AIU | sd1_enc | $I^2S$ Audio in channel 2 | Input | | Pull-up | 249 | A14 |
| AIU | ws_enc | $I^2S$ Audio in channel select | Bi-Dir | 8 | Pull-up | 251 | C13 |
| AOU | amclk_dec | Audio out master clock | Output | 8 | | 286 | A4 |
| AOU | PLL_amclk_dec | External audio out master clock | Input | | | 300 | A1 |
| AOU | sck_dec | Audio out clock | Output | 8 | | 282 | B6 |
| AOU | sd0_dec | Audio out channel 1 - $I^2S$ | Output | 8 | | 284 | B5 |
| AOU | sd1_dec | Audio out channel 2 - S/P-DIF | Output | 8 | | 285 | C6 |
| AOU | ws_dec | Audio out channel select | Output | 8 | | 281 | A5 |
| Chip | pcr_clk | PCR clock | Input | | | 261 | E11 |
| Chip | reset_ | Global reset | Input | | Schmitt trig. | 262 | B11 |
| Demux | cdi[0] | Compressed data in [7:0] | Input | | Pull-up | 8 | D3 |
| Demux | cdi[1] | Compressed data in [7:0] | Input | | Pull-up | 7 | D1 |
| Demux | cdi[2] | Compressed data in [7:0] | Input | | Pull-up | 6 | D2 |
| Demux | cdi[3] | Compressed data in [7:0] | Input | | Pull-up | 5 | C1 |
| Demux | cdi[4] | Compressed data in [7:0] | Input | | Pull-up | 4 | C2 |
| Demux | cdi[5] | Compressed data in [7:0] | Input | | Pull-up | 3 | B1 |
| Demux | cdi[6] | Compressed data in [7:0] | Input | | Pull-up | 2 | C3 |
| Demux | cdi[7] | Compressed data in [7:0] | Input | | Pull-up | 1 | D4 |
| Demux | cdi_clk | Compressed data in clock | Input | | Pull-up | 10 | F4 |
| Demux | cdi_valid | Compressed data in enable | Input | | Pull-up | 9 | E4 |
| DMIU | sdram_dec_addr[ 0] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 114 | W11 |
| DMIU | sdram_dec_addr[ 1] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 116 | U11 |
| DMIU | sdram_dec_addr[ 2] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 118 | W12 |
| DMIU | sdram_dec_addr[ 3] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 120 | T11 |
| DMIU | sdram_dec_addr[ 4] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 122 | W13 |
| DMIU | sdram_dec_addr[ 5] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 123 | V13 |
| DMIU | sdram_dec_addr[ 6] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 121 | Y13 |
| DMIU | sdram_dec_addr[ 7] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 119 | V12 |
| DMIU | sdram_dec_addr[ 8] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 117 | Y12 |
| DMIU | sdram_dec_addr[ 9] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 115 | Y11 |
| DMIU | sdram_dec_addr[10] | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 113 | V11 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| DMIU | sdram_dec_ba[0] | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 124 | U12 |
| DMIU | sdram_dec_ba[1] | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 138 | Y18 |
| DMIU | sdram_dec_cas_ | Decoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 135 | W16 |
| DMIU | sdram_dec_cke | Decoder SDRAM clock enable | Output | 8 | Slew rate cont. | 126 | W14 |
| DMIU | sdram_dec_clk | Decoder SDRAM clock | Bi-Dir | 24 | | 127 | V14 |
| DMIU | sdram_dec_cs_ | Decoder SDRAM chip select | Output | 8 | Slew rate cont. | 128 | T12 |
| DMIU | sdram_dec_data[ 0] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 112 | T10 |
| DMIU | sdram_dec_data[ 1] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 111 | Y10 |
| DMIU | sdram_dec_data[ 2] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 110 | W10 |
| DMIU | sdram_dec_data[ 3] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 109 | V10 |
| DMIU | sdram_dec_data[ 4] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 108 | U10 |
| DMIU | sdram_dec_data[ 5] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 107 | Y9 |
| DMIU | sdram_dec_data[ 6] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 106 | W9 |
| DMIU | sdram_dec_data[ 7] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 105 | V9 |
| DMIU | sdram_dec_data[ 8] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 104 | T9 |
| DMIU | sdram_dec_data[ 9] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 103 | Y8 |
| DMIU | sdram_dec_data[10] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 102 | W8 |
| DMIU | sdram_dec_data[11] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 101 | V8 |
| DMIU | sdram_dec_data[12] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 100 | U9 |
| DMIU | sdram_dec_data[13] | Decoder DRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 99 | Y7 |
| DMIU | sdram_dec_data[14] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 98 | W7 |
| DMIU | sdram_dec_data[15] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 97 | V7 |
| DMIU | sdram_dec_data[16] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 96 | U8 |
| DMIU | sdram_dec_data[17] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 95 | T8 |
| DMIU | sdram_dec_data[18] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 94 | Y6 |
| DMIU | sdram_dec_data[19] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 93 | W6 |
| DMIU | sdram_dec_data[20] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 92 | V6 |
| DMIU | sdram_dec_data[21] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 91 | T7 |
| DMIU | sdram_dec_data[22] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 90 | U7 |
| DMIU | sdram_dec_data[23] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 89 | Y5 |
| DMIU | sdram_dec_data[24] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 88 | U6 |
| DMIU | sdram_dec_data[25] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 87 | W5 |
| DMIU | sdram_dec_data[26] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 86 | Y4 |
| DMIU | sdram_dec_data[27] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 85 | V5 |
| DMIU | sdram_dec_data[28] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 84 | U5 |
| DMIU | sdram_dec_data[29] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 83 | W4 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| DMIU | sdram_dec_data[30] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 82 | Y3 |
| DMIU | sdram_dec_data[31] | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 81 | V4 |
| DMIU | sdram_dec_dqm[0] | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 129 | Y15 |
| DMIU | sdram_dec_dqm[1] | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 130 | W15 |
| DMIU | sdram_dec_dqm[2] | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 131 | Y16 |
| DMIU | sdram_dec_dqm[3] | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 132 | U13 |
| DMIU | sdram_dec_ras_ | Decoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 133 | V15 |
| DMIU | sdram_dec_we_ | Decoder SDRAM write enable | Output | 8 | Slew rate cont. | 125 | Y14 |
| EJTAG | ejtag_dclk | Debug clock | Output | 8 | | 66 | P5 |
| EJTAG | ejtag_pcst[0] | Program counter status trace[2:0] | Output | 8 | | 78 | Y1 |
| EJTAG | ejtag_pcst[1] | Program counter status trace[2:0] | Output | 8 | | 79 | Y2 |
| EJTAG | ejtag_pcst[2] | Program counter status trace[2:0] | Output | 8 | | 80 | W3 |
| EJTAG | ejtag_pcst2[0] | Program counter status trace2[2:0] | Output | 8 | | 67 | U2 |
| EJTAG | ejtag_pcst2[1] | Program counter status trace2[2:0] | Output | 8 | | 76 | T6 |
| EJTAG | ejtag_pcst2[2] | Program counter status trace2[2:0] | Output | 8 | | 77 | V3 |
| EJTAG | ejtag_pcst3[0] | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 210 | E19 |
| EJTAG | ejtag_pcst3[1] | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 209 | F18 |
| EJTAG | ejtag_pcst3[2] | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 208 | H16 |
| EJTAG | ejtag_pcst4[0] | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 207 | E20 |
| EJTAG | ejtag_pcst4[1] | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 206 | H17 |
| EJTAG | ejtag_pcst4[2] | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 205 | F19 |
| EMIU | sdram_enc_addr[ 0] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 193 | J19 |
| EMIU | sdram_enc_addr[ 1] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 195 | K16 |
| EMIU | sdram_enc_addr[ 2] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 197 | H19 |
| EMIU | sdram_enc_addr[ 3] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 199 | J17 |
| EMIU | sdram_enc_addr[ 4] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 201 | G19 |
| EMIU | sdram_enc_addr[ 5] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 202 | G18 |
| EMIU | sdram_enc_addr[ 6] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 200 | G20 |
| EMIU | sdram_enc_addr[ 7] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 198 | H18 |
| EMIU | sdram_enc_addr[ 8] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 196 | H20 |
| EMIU | sdram_enc_addr[ 9] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 194 | J18 |
| EMIU | sdram_enc_addr[10] | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 192 | J20 |
| EMIU | sdram_enc_ba[0] | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 229 | A19 |
| EMIU | sdram_enc_ba[1] | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 230 | B18 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| EMIU | sdram_enc_cas_ | Encoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 228 | A20 |
| EMIU | sdram_enc_cke | Encoder SDRAM clock enable | Output | 8 | Slew rate cont. | 186 | L20 |
| EMIU | sdram_enc_clk | Encoder SDRAM clock | Bi-Dir | 24 | | 185 | L19 |
| EMIU | sdram_enc_cs_ | Encoder SDRAM chip select | Output | 8 | Slew rate cont. | 187 | L16 |
| EMIU | sdram_enc_data[ 0] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 184 | L18 |
| EMIU | sdram_enc_data[ 1] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 183 | L17 |
| EMIU | sdram_enc_data[ 2] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 182 | M20 |
| EMIU | sdram_enc_data[ 3] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 181 | M19 |
| EMIU | sdram_enc_data[ 4] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 180 | M18 |
| EMIU | sdram_enc_data[ 5] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 179 | M16 |
| EMIU | sdram_enc_data[ 6] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 178 | N20 |
| EMIU | sdram_enc_data[ 7] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 177 | N19 |
| EMIU | sdram_enc_data[ 8] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 176 | N18 |
| EMIU | sdram_enc_data[ 9] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 175 | M17 |
| EMIU | sdram_enc_data[10] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 174 | P20 |
| EMIU | sdram_enc_data[11] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 173 | P19 |
| EMIU | sdram_enc_data[12] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 172 | P18 |
| EMIU | sdram_enc_data[13] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 171 | N16 |
| EMIU | sdram_enc_data[14] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 170 | N17 |
| EMIU | sdram_enc_data[15] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 169 | R20 |
| EMIU | sdram_enc_data[16] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 168 | R19 |
| EMIU | sdram_enc_data[17] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 167 | R18 |
| EMIU | sdram_enc_data[18] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 166 | P17 |
| EMIU | sdram_enc_data[19] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 164 | R16 |
| EMIU | sdram_enc_data[20] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 163 | T20 |
| EMIU | sdram_enc_data[21] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 162 | R17 |
| EMIU | sdram_enc_data[22] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 161 | T19 |
| EMIU | sdram_enc_data[23] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 160 | U20 |
| EMIU | sdram_enc_data[24] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 159 | T18 |
| EMIU | sdram_enc_data[25] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 158 | T17 |
| EMIU | sdram_enc_data[26] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 157 | U19 |
| EMIU | sdram_enc_data[27] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 156 | V20 |
| EMIU | sdram_enc_data[28] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 155 | U18 |
| EMIU | sdram_enc_data[29] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 154 | V19 |
| EMIU | sdram_enc_data[30] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 153 | W20 |
| EMIU | sdram_enc_data[31] | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 152 | Y20 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| EMIU | sdram_enc_dqm[0] | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 188 | K18 |
| EMIU | sdram_enc_dqm[1] | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 189 | K19 |
| EMIU | sdram_enc_dqm[2] | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 190 | K20 |
| EMIU | sdram_enc_dqm[3] | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 191 | K17 |
| EMIU | sdram_enc_ras_ | Encoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 227 | C18 |
| EMIU | sdram_enc_we_ | Encoder SDRAM write enable | Output | 8 | Slew rate cont. | 231 | C17 |
| GPIO | pio[ 0] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 151 | V18 |
| GPIO | pio[ 1] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 150 | T16 |
| GPIO | pio[ 2] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 149 | U17 |
| GPIO | pio[ 3] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 148 | W19 |
| GPIO | pio[ 4] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 147 | T15 |
| GPIO | pio[ 5] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 146 | W18 |
| GPIO | pio[ 6] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 145 | V17 |
| GPIO | pio[ 7] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 144 | U16 |
| GPIO | pio[ 8] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 143 | Y19 |
| GPIO | pio[ 9] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 142 | W17 |
| GPIO | pio[10] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 140 | U15 |
| GPIO | pio[11] | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 139 | V16 |
| HIU / Intel | int_ | Host interrupt | Output | PCI | Open-drain | 11 | E3 |
| HIU / Intel | intel_ad[ 0] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| HIU / Intel | intel_ad[ 1] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| HIU / Intel | intel_ad[ 2] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| HIU / Intel | intel_ad[ 3] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |
| HIU / Intel | intel_ad[ 4] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| HIU / Intel | intel_ad[ 5] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| HIU / Intel | intel_ad[ 6] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |
| HIU / Intel | intel_ad[ 7] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| HIU / Intel | intel_ad[ 8] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| HIU / Intel | intel_ad[ 9] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| HIU / Intel | intel_ad[10] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| HIU / Intel | intel_ad[11] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| HIU / Intel | intel_ad[12] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| HIU / Intel | intel_ad[13] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| HIU / Intel | intel_ad[14] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| HIU / Intel | intel_ad[15] | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| HIU / Intel | intel_as_ale_ | Host address select / address latch enable | Bi-Dir | PCI | Tri-state | 52 | P3 |
| HIU / Intel | intel_cdi_ack_ | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 | K1 |
| HIU / Intel | intel_cdi_req_ | Host CDI request | Bi-Dir | PCI | Tri-state | 37 | K5 |
| HIU / Intel | intel_cdo_ack_ | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 | L2 |
| HIU / Intel | intel_cdo_req_ | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 | G3 |
| HIU / Intel | intel_cs_ | Host chip select | Bi-Dir | PCI | Tri-state | 42 | M1 |
| HIU / Intel | intel_dtack_ | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 | L1 |
| HIU / Intel | intel_rd_ | Host read | Bi-Dir | PCI | Tri-state | 33 | K4 |
| HIU / Intel | intel_wr_ | Host write | Bi-Dir | PCI | Tri-state | 32 | J1 |
| HIU / Moto | hiu_host_cdi_req_ | Host CDI request | Bi-Dir | PCI | Tri-state | 37 | K5 |
| HIU / Moto | hiu_host_cdo_req_ | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 | G3 |
| HIU / Moto | hiu_host_dtack_ | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 | L1 |
| HIU / Moto | host_hiu_addr[ 0] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 43 | M2 |
| HIU / Moto | host_hiu_addr[ 1] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 31 | J2 |
| HIU / Moto | host_hiu_addr[ 2] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 30 | J3 |
| HIU / Moto | host_hiu_addr[ 3] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 29 | J5 |
| HIU / Moto | host_hiu_addr[ 4] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 28 | H1 |
| HIU / Moto | host_hiu_addr[ 5] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 27 | H2 |
| HIU / Moto | host_hiu_addr[ 6] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 26 | H3 |
| HIU / Moto | host_hiu_addr[ 7] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 25 | J4 |
| HIU / Moto | host_hiu_addr[ 8] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 24 | G1 |
| HIU / Moto | host_hiu_addr[ 9] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 21 | H4 |
| HIU / Moto | host_hiu_addr[10] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 20 | H5 |
| HIU / Moto | host_hiu_addr[11] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 19 | F1 |
| HIU / Moto | host_hiu_addr[12] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 18 | F2 |
| HIU / Moto | host_hiu_addr[13] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 17 | F3 |
| HIU / Moto | host_hiu_addr[14] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 16 | G4 |
| HIU / Moto | host_hiu_addr[15] | Host address [15:0] | Bi-Dir | PCI | Tri-state | 15 | G5 |
| HIU / Moto | host_hiu_as_ | Host address select | Bi-Dir | PCI | Tri-state | 52 | P3 |
| HIU / Moto | host_hiu_cdi_ack_ | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 | K1 |
| HIU / Moto | host_hiu_cdo_ack_ | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 | L2 |
| HIU / Moto | host_hiu_cs_ | Host chip select | Bi-Dir | PCI | Tri-state | 42 | M1 |
| HIU / Moto | host_hiu_data[ 0] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| HIU / Moto | host_hiu_data[ 1] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| HIU / Moto | host_hiu_data[ 2] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| HIU / Moto | host_hiu_data[ 3] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| HIU / Moto | host_hiu_data[ 4] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| HIU / Moto | host_hiu_data[ 5] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| HIU / Moto | host_hiu_data[ 6] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |
| HIU / Moto | host_hiu_data[ 7] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| HIU / Moto | host_hiu_data[ 8] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| HIU / Moto | host_hiu_data[ 9] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| HIU / Moto | host_hiu_data[10] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| HIU / Moto | host_hiu_data[11] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| HIU / Moto | host_hiu_data[12] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| HIU / Moto | host_hiu_data[13] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| HIU / Moto | host_hiu_data[14] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| HIU / Moto | host_hiu_data[15] | Host data [15:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |
| HIU / Moto | host_hiu_rw_ | Host read/write | Bi-Dir | PCI | Tri-state | 32 | J1 |
| HIU / Moto | int_ | Host interrupt | Output | PCI | Open-drain | 11 | E3 |
| HIU / PCI | pci_ad [ 5] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| HIU / PCI | pci_ad[ 0] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| HIU / PCI | pci_ad[ 1] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| HIU / PCI | pci_ad[ 2] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| HIU / PCI | pci_ad[ 3] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |
| HIU / PCI | pci_ad[ 4] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| HIU / PCI | pci_ad[ 6] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |
| HIU / PCI | pci_ad[ 7] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| HIU / PCI | pci_ad[ 8] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| HIU / PCI | pci_ad[ 9] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| HIU / PCI | pci_ad[10] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| HIU / PCI | pci_ad[11] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| HIU / PCI | pci_ad[12] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| HIU / PCI | pci_ad[13] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| HIU / PCI | pci_ad[14] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| HIU / PCI | pci_ad[15] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |
| HIU / PCI | pci_ad[16] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 43 | M2 |
| HIU / PCI | pci_ad[17] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 31 | J2 |
| HIU / PCI | pci_ad[18] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 30 | J3 |
| HIU / PCI | pci_ad[19] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 29 | J5 |
| HIU / PCI | pci_ad[20] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 28 | H1 |
| HIU / PCI | pci_ad[21] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 27 | H2 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| HIU / PCI | pci_ad[22] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 26 | H3 |
| HIU / PCI | pci_ad[23] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 25 | J4 |
| HIU / PCI | pci_ad[24] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 24 | G1 |
| HIU / PCI | pci_ad[25] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 21 | H4 |
| HIU / PCI | pci_ad[26] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 20 | H5 |
| HIU / PCI | pci_ad[27] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 19 | F1 |
| HIU / PCI | pci_ad[28] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 18 | F2 |
| HIU / PCI | pci_ad[29] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 17 | F3 |
| HIU / PCI | pci_ad[30] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 16 | G4 |
| HIU / PCI | pci_ad[31] | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 15 | G5 |
| HIU / PCI | pci_cbe_[0] | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 52 | P3 |
| HIU / PCI | pci_cbe_[1] | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 42 | M1 |
| HIU / PCI | pci_cbe_[2] | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 32 | J1 |
| HIU / PCI | pci_cbe_[3] | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 22 | G3 |
| HIU / PCI | pci_clk | PCI clock | Input | PCI | | 12 | E2 |
| HIU / PCI | pci_devsel_ | PCI device select | Bi-Dir | PCI | Tri-state | 36 | K1 |
| HIU / PCI | pci_frame_ | PCI cycle frame / transaction | Bi-Dir | PCI | Tri-state | 33 | K4 |
| HIU / PCI | pci_gnt_ | PCI grant | Input | PCI | Tri-state | 38 | L3 |
| HIU / PCI | pci_idsel | PCI init. device select | Input | PCI | | 23 | G2 |
| HIU / PCI | pci_inta_ | PCI interrupt A | Output | PCI | Open-drain | 11 | E3 |
| HIU / PCI | pci_irdy_ | PCI initiator ready | Bi-Dir | PCI | Tri-state | 34 | K3 |
| HIU / PCI | pci_par | PCI parity | Bi-Dir | PCI | Tri-state | 41 | L4 |
| HIU / PCI | pci_perr_ | PCI parity error | Bi-Dir | PCI | Tri-state | 39 | L2 |
| HIU / PCI | pci_req_ | PCI bus request | Bi-Dir | PCI | Tri-state | 13 | E1 |
| HIU / PCI | pci_serr_ | PCI system error | Bi-Dir | PCI | Open-drain | 40 | L1 |
| HIU / PCI | pci_stop_ | PCI stop transaction | Bi-Dir | PCI | Tri-state | 37 | K5 |
| HIU / PCI | pci_trdy_ | PCI target ready | Bi-Dir | PCI | Tri-state | 35 | K2 |
| ICI | scl | ICI clock | Bi-Dir | 4 | Schmitt trig. | 136 | U14 |
| ICI | sda | ICI data | Bi-Dir | 4 | Schmitt trig. | 137 | Y17 |
| JTAG | tck | Test clock | Input | | Pull-up | 63 | V1 |
| JTAG | tdi | Test data in | Input | | Pull-up | 64 | T3 |
| JTAG | tdo | Test data out | Output | 4 | Pull-up/ tri-state | 65 | R4 |
| JTAG | tms | Test mode select | Input | | Pull-up | 62 | U1 |
| JTAG | trst_ | Test reset | Input | | Pull-down | 61 | P4 |
| mPLL | PLL_bypass | Main PLL disable / bypass | Input | | | 69 | T4 |
| mPLL | PLL_clock | Main PLL clock | Input | | | 68 | W1 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| Mux | cdo[0] | Compressed data out [7:0] | Output | 8 | | 239 | A16 |
| Mux | cdo[1] | Compressed data out [7:0] | Output | 8 | | 238 | D15 |
| Mux | cdo[2] | Compressed data out [7:0] | Output | 8 | | 237 | B16 |
| Mux | cdo[3] | Compressed data out [7:0] | Output | 8 | | 236 | A17 |
| Mux | cdo[4] | Compressed data out [7:0] | Output | 8 | | 235 | C16 |
| Mux | cdo[5] | Compressed data out [7:0] | Output | 8 | | 234 | D16 |
| Mux | cdo[6] | Compressed data out [7:0] | Output | 8 | | 233 | B17 |
| Mux | cdo[7] | Compressed data out [7:0] | Output | 8 | | 232 | A18 |
| Mux | cdo_clk | Compressed data out clock | Output | 8 | | 240 | D14 |
| Mux | cdo_sop | Compressed data start of packet | Output | 8 | | 242 | C15 |
| Mux | cdo_valid | Compressed data out valid | Output | 8 | | 246 | D13 |
| Mux | excd_clk | External compressed data clock | Input | | Pull-down | 243 | B15 |
| Mux | excd_rd | External compressed data read | Input | | Pull-up | 244 | A15 |
| Mux | fifo_level | Mux FIFO level | Output | 8 | | 247 | C14 |
| ROM | rom_addr[ 0] | ROM address [21:0] | Output | 8 | | 280 | C8 |
| ROM | rom_addr[ 1] | ROM address [21:0] | Output | 8 | | 279 | D8 |
| ROM | rom_addr[ 2] | ROM address [21:0] | Output | 8 | | 277 | B7 |
| ROM | rom_addr[ 3] | ROM address [21:0] | Output | 8 | | 276 | E9 |
| ROM | rom_addr[ 4] | ROM address [21:0] | Output | 8 | | 275 | A6 |
| ROM | rom_addr[ 5] | ROM address [21:0] | Output | 8 | | 274 | D9 |
| ROM | rom_addr[ 6] | ROM address [21:0] | Output | 8 | | 273 | B8 |
| ROM | rom_addr[ 7] | ROM address [21:0] | Output | 8 | | 272 | C9 |
| ROM | rom_addr[ 8] | ROM address [21:0] | Output | 8 | | 247 | C14 |
| ROM | rom_addr[ 9] | ROM address [21:0] | Output | 8 | | 246 | D13 |
| ROM | rom_addr[10] | ROM address [21:0] | Output | 8 | | 242 | C15 |
| ROM | rom_addr[11] | ROM address [21:0] | Output | 8 | | 240 | D14 |
| ROM | rom_addr[12] | ROM address [21:0] | Output | 8 | | 239 | A16 |
| ROM | rom_addr[13] | ROM address [21:0] | Output | 8 | | 238 | D15 |
| ROM | rom_addr[14] | ROM address [21:0] | Output | 8 | | 237 | B16 |
| ROM | rom_addr[15] | ROM address [21:0] | Output | 8 | | 236 | A17 |
| ROM | rom_addr[16] | ROM address [21:0] | Output | 8 | | 235 | C16 |
| ROM | rom_addr[17] | ROM address [21:0] | Output | 8 | | 234 | D16 |
| ROM | rom_addr[18] | ROM address [21:0] | Output | 8 | | 233 | B17 |
| ROM | rom_addr[19] | ROM address [21:0] | Output | 8 | | 232 | A18 |
| ROM | rom_addr[20] | ROM address [21:0] | Output | 8 | | 285 | C6 |
| ROM | rom_addr[21] | ROM address [21:0] | Output | 8 | | 284 | B5 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| ROM | rom_ce_ | ROM chip enable | Output | 8 | | 278 | C7 |
| ROM | rom_data[0] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 270 | A8 |
| ROM | rom_data[1] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 269 | E10 |
| ROM | rom_data[2] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 268 | B9 |
| ROM | rom_data[3] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 267 | C10 |
| ROM | rom_data[4] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 266 | D10 |
| ROM | rom_data[5] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 265 | A9 |
| ROM | rom_data[6] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 264 | B10 |
| ROM | rom_data[7] | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 263 | A10 |
| ROM | rom_oe_ | ROM output enable | Output | 8 | | 281 | A5 |
| ROM | rom_we_ | ROM write enable | Output | 8 | | 282 | B6 |
| VIU | clk_27 | Video input clock 27 MHz | Input | | | 260 | A11 |
| VIU | clk_vbi | External VBI clock 27 MHz | Input | | Pull-up | 226 | E15 |
| VIU | vbi_data[0] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 210 | E19 |
| VIU | vbi_data[1] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 209 | F18 |
| VIU | vbi_data[2] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 208 | H16 |
| VIU | vbi_data[3] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 207 | E20 |
| VIU | vbi_data[4] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 206 | H17 |
| VIU | vbi_data[5] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 205 | F19 |
| VIU | vbi_data[6] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 204 | F20 |
| VIU | vbi_data[7] | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 203 | J16 |
| VIU | vbi_data_en | VBI data enable | Input | | Pull-up | 211 | G17 |
| VIU | vpo[0] | Video input data [7:0] | Input | | | 259 | C11 |
| VIU | vpo[1] | Video input data [7:0] | Input | | | 258 | D11 |
| VIU | vpo[2] | Video input data [7:0] | Input | | | 257 | A12 |
| VIU | vpo[3] | Video input data [7:0] | Input | | | 256 | B12 |
| VIU | vpo[4] | Video input data [7:0] | Input | | | 255 | C12 |
| VIU | vpo[5] | Video input data [7:0] | Input | | | 254 | E12 |
| VIU | vpo[6] | Video input data [7:0] | Input | | | 253 | A13 |
| VIU | vpo[7] | Video input data [7:0] | Input | | | 252 | B13 |
| VOU | vou_clk | Video output clock 27 MHz | Output | 8 | | 271 | A7 |
| VOU | vou_vpo[0] | Video output data [7:0] | Output | 8 | | 280 | C8 |
| VOU | vou_vpo[1] | Video output data [7:0] | Output | 8 | | 279 | D8 |
| VOU | vou_vpo[2] | Video output data [7:0] | Output | 8 | | 277 | B7 |
| VOU | vou_vpo[3] | Video output data [7:0] | Output | 8 | | 276 | E9 |

**Table 11 I/O Signals, Sorted by Module (Continued)**

| Module | Signal Name | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| VOU | vou_vpo[4] | Video output data [7:0] | Output | 8 | | 275 | A6 |
| VOU | vou_vpo[5] | Video output data [7:0] | Output | 8 | | 274 | D9 |
| VOU | vou_vpo[6] | Video output data [7:0] | Output | 8 | | 273 | B8 |
| VOU | vou_vpo[7] | Video output data [7:0] | Output | 8 | | 272 | C9 |

### Table 12 I/O Signals, Sorted by Signal Name

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| amclk_dec | AOU | Audio out master clock | Output | 8 | | 286 | A4 |
| amclk_enc | AIU | Audio in master clock | Output | 8 | | 212 | D20 |
| cdi[0] | Demux | Compressed data in [7:0] | Input | | Pull-up | 8 | D3 |
| cdi[1] | Demux | Compressed data in [7:0] | Input | | Pull-up | 7 | D1 |
| cdi[2] | Demux | Compressed data in [7:0] | Input | | Pull-up | 6 | D2 |
| cdi[3] | Demux | Compressed data in [7:0] | Input | | Pull-up | 5 | C1 |
| cdi[4] | Demux | Compressed data in [7:0] | Input | | Pull-up | 4 | C2 |
| cdi[5] | Demux | Compressed data in [7:0] | Input | | Pull-up | 3 | B1 |
| cdi[6] | Demux | Compressed data in [7:0] | Input | | Pull-up | 2 | C3 |
| cdi[7] | Demux | Compressed data in [7:0] | Input | | Pull-up | 1 | D4 |
| cdi_clk | Demux | Compressed data in clock | Input | | Pull-up | 10 | F4 |
| cdi_valid | Demux | Compressed data in enable | Input | | Pull-up | 9 | E4 |
| cdo[0] | Mux | Compressed data out [7:0] | Output | 8 | | 239 | A16 |
| cdo[1] | Mux | Compressed data out [7:0] | Output | 8 | | 238 | D15 |
| cdo[2] | Mux | Compressed data out [7:0] | Output | 8 | | 237 | B16 |
| cdo[3] | Mux | Compressed data out [7:0] | Output | 8 | | 236 | A17 |
| cdo[4] | Mux | Compressed data out [7:0] | Output | 8 | | 235 | C16 |
| cdo[5] | Mux | Compressed data out [7:0] | Output | 8 | | 234 | D16 |
| cdo[6] | Mux | Compressed data out [7:0] | Output | 8 | | 233 | B17 |
| cdo[7] | Mux | Compressed data out [7:0] | Output | 8 | | 232 | A18 |
| cdo_clk | Mux | Compressed data out clock | Output | 8 | | 240 | D14 |
| cdo_sop | Mux | Compressed data start of packet | Output | 8 | | 242 | C15 |
| cdo_valid | Mux | Compressed data out valid | Output | 8 | | 246 | D13 |
| clk_27 | VIU | Video input clock 27 MHz | Input | | | 260 | A11 |
| clk_vbi | VIU | External VBI clock 27 MHz | Input | | Pull-up | 226 | E15 |
| ejtag_dclk | EJTAG | Debug clock | Output | 8 | | 66 | P5 |
| ejtag_pcst[0] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 78 | Y1 |
| ejtag_pcst[1] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 79 | Y2 |
| ejtag_pcst[2] | EJTAG | Program counter status trace[2:0] | Output | 8 | | 80 | W3 |
| ejtag_pcst2[0] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 67 | U2 |
| ejtag_pcst2[1] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 76 | T6 |
| ejtag_pcst2[2] | EJTAG | Program counter status trace2[2:0] | Output | 8 | | 77 | V3 |
| ejtag_pcst3[0] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 210 | E19 |
| ejtag_pcst3[1] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 209 | F18 |
| ejtag_pcst3[2] | EJTAG | Program counter status trace3[2:0] | Bi-Dir | 8 | Pull-up | 208 | H16 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| ejtag_pcst4[0] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 207 | E20 |
| ejtag_pcst4[1] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 206 | H17 |
| ejtag_pcst4[2] | EJTAG | Program counter status trace4[2:0] | Bi-Dir | 8 | Pull-up | 205 | F19 |
| excd_clk | Mux | External compressed data clock | Input | | Pull-down | 243 | B15 |
| excd_rd | Mux | External compressed data read | Input | | Pull-up | 244 | A15 |
| fifo_level | Mux | Mux FIFO level | Output | 8 | | 247 | C14 |
| hiu_host_cdi_req_ | HIU / Moto | Host CDI request | Bi-Dir | PCI | Tri-state | 37 | K5 |
| hiu_host_cdo_req_ | HIU / Moto | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 | G3 |
| hiu_host_dtack_ | HIU / Moto | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 | L1 |
| host_hiu_addr[ 0] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 43 | M2 |
| host_hiu_addr[ 1] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 31 | J2 |
| host_hiu_addr[ 2] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 30 | J3 |
| host_hiu_addr[ 3] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 29 | J5 |
| host_hiu_addr[ 4] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 28 | H1 |
| host_hiu_addr[ 5] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 27 | H2 |
| host_hiu_addr[ 6] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 26 | H3 |
| host_hiu_addr[ 7] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 25 | J4 |
| host_hiu_addr[ 8] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 24 | G1 |
| host_hiu_addr[ 9] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 21 | H4 |
| host_hiu_addr[10] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 20 | H5 |
| host_hiu_addr[11] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 19 | F1 |
| host_hiu_addr[12] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 18 | F2 |
| host_hiu_addr[13] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 17 | F3 |
| host_hiu_addr[14] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 16 | G4 |
| host_hiu_addr[15] | HIU / Moto | Host address [15:0] | Bi-Dir | PCI | Tri-state | 15 | G5 |
| host_hiu_as_ | HIU / Moto | Host address select | Bi-Dir | PCI | Tri-state | 52 | P3 |
| host_hiu_cdi_ack_ | HIU / Moto | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 | K1 |
| host_hiu_cdo_ack_ | HIU / Moto | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 | L2 |
| host_hiu_cs_ | HIU / Moto | Host chip select | Bi-Dir | PCI | Tri-state | 42 | M1 |
| host_hiu_data[ 0] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| host_hiu_data[ 1] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| host_hiu_data[ 2] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| host_hiu_data[ 3] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |
| host_hiu_data[ 4] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| host_hiu_data[ 5] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| host_hiu_data[ 6] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| host_hiu_data[ 7] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| host_hiu_data[ 8] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| host_hiu_data[ 9] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| host_hiu_data[10] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| host_hiu_data[11] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| host_hiu_data[12] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| host_hiu_data[13] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| host_hiu_data[14] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| host_hiu_data[15] | HIU / Moto | Host data [15:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |
| host_hiu_rw_ | HIU / Moto | Host read/write | Bi-Dir | PCI | Tri-state | 32 | J1 |
| int_ | HIU / Moto | Host interrupt | Output | PCI | Open-drain | 11 | E3 |
| int_ | HIU / Intel | Host interrupt | Output | PCI | Open-drain | 11 | E3 |
| intel_ad[ 0] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| intel_ad[ 1] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| intel_ad[ 2] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| intel_ad[ 3] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |
| intel_ad[ 4] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| intel_ad[ 5] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| intel_ad[ 6] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |
| intel_ad[ 7] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| intel_ad[ 8] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| intel_ad[ 9] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| intel_ad[10] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| intel_ad[11] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| intel_ad[12] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| intel_ad[13] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| intel_ad[14] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| intel_ad[15] | HIU / Intel | Host data / address [15:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |
| intel_as_ale_ | HIU / Intel | Host address select / address latch enable | Bi-Dir | PCI | Tri-state | 52 | P3 |
| intel_cdi_ack_ | HIU / Intel | Host CDI acknowledge | Bi-Dir | PCI | Tri-state | 36 | K1 |
| intel_cdi_req_ | HIU / Intel | Host CDI request | Bi-Dir | PCI | Tri-state | 37 | K5 |
| intel_cdo_ack_ | HIU / Intel | Host CDO acknowledge | Bi-Dir | PCI | Tri-state | 39 | L2 |
| intel_cdo_req_ | HIU / Intel | Compressed data out request | Bi-Dir | PCI | Tri-state | 22 | G3 |
| intel_cs_ | HIU / Intel | Host chip select | Bi-Dir | PCI | Tri-state | 42 | M1 |
| intel_dtack_ | HIU / Intel | Host CDO transfer acknowledge | Bi-Dir | PCI | Open-drain | 40 | L1 |
| intel_rd_ | HIU / Intel | Host read | Bi-Dir | PCI | Tri-state | 33 | K4 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| intel_wr_ | HIU / Intel | Host write | Bi-Dir | PCI | Tri-state | 32 | J1 |
| pci_ad[ 0] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 60 | T2 |
| pci_ad[ 1] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 59 | N5 |
| pci_ad[ 2] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 58 | R3 |
| pci_ad[ 3] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 57 | N4 |
| pci_ad[ 4] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 56 | T1 |
| pci_ad[ 5] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 55 | R2 |
| pci_ad[ 6] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 54 | R1 |
| pci_ad[ 7] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 53 | M5 |
| pci_ad[ 8] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 51 | P2 |
| pci_ad[ 9] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 50 | P1 |
| pci_ad[10] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 49 | M4 |
| pci_ad[11] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 48 | N3 |
| pci_ad[12] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 47 | N2 |
| pci_ad[13] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 46 | N1 |
| pci_ad[14] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 45 | L5 |
| pci_ad[15] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 44 | M3 |
| pci_ad[16] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 43 | M2 |
| pci_ad[17] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 31 | J2 |
| pci_ad[18] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 30 | J3 |
| pci_ad[19] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 29 | J5 |
| pci_ad[20] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 28 | H1 |
| pci_ad[21] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 27 | H2 |
| pci_ad[22] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 26 | H3 |
| pci_ad[23] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 25 | J4 |
| pci_ad[24] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 24 | G1 |
| pci_ad[25] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 21 | H4 |
| pci_ad[26] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 20 | H5 |
| pci_ad[27] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 19 | F1 |
| pci_ad[28] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 18 | F2 |
| pci_ad[29] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 17 | F3 |
| pci_ad[30] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 16 | G4 |
| pci_ad[31] | HIU / PCI | PCI data/address [31:0] | Bi-Dir | PCI | Tri-state | 15 | G5 |
| pci_cbe_[0] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 52 | P3 |
| pci_cbe_[1] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 42 | M1 |
| pci_cbe_[2] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 32 | J1 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| pci_cbe_[3] | HIU / PCI | PCI bus command / byte enables | Bi-Dir | PCI | Tri-state | 22 | G3 |
| pci_clk | HIU / PCI | PCI clock | Input | PCI | | 12 | E2 |
| pci_devsel_ | HIU / PCI | PCI device select | Bi-Dir | PCI | Tri-state | 36 | K1 |
| pci_frame_ | HIU / PCI | PCI cycle frame / transaction | Bi-Dir | PCI | Tri-state | 33 | K4 |
| pci_gnt_ | HIU / PCI | PCI grant | Input | PCI | Tri-state | 38 | L3 |
| pci_idsel | HIU / PCI | PCI init. device select | Input | PCI | | 23 | G2 |
| pci_inta_ | HIU / PCI | PCI interrupt A | Output | PCI | Open-drain | 11 | E3 |
| pci_irdy_ | HIU / PCI | PCI initiator ready | Bi-Dir | PCI | Tri-state | 34 | K3 |
| pci_par | HIU / PCI | PCI parity | Bi-Dir | PCI | Tri-state | 41 | L4 |
| pci_perr_ | HIU / PCI | PCI parity error | Bi-Dir | PCI | Tri-state | 39 | L2 |
| pci_req_ | HIU / PCI | PCI bus request | Bi-Dir | PCI | Tri-state | 13 | E1 |
| pci_serr_ | HIU / PCI | PCI system error | Bi-Dir | PCI | Open-drain | 40 | L1 |
| pci_stop_ | HIU / PCI | PCI stop transaction | Bi-Dir | PCI | Tri-state | 37 | K5 |
| pci_trdy_ | HIU / PCI | PCI target ready | Bi-Dir | PCI | Tri-state | 35 | K2 |
| pcr_clk | Chip | PCR clock | Input | | | 261 | E11 |
| pio[ 0] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 151 | V18 |
| pio[ 1] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 150 | T16 |
| pio[ 2] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 149 | U17 |
| pio[ 3] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 148 | W19 |
| pio[ 4] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 147 | T15 |
| pio[ 5] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 146 | W18 |
| pio[ 6] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 145 | V17 |
| pio[ 7] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 144 | U16 |
| pio[ 8] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 143 | Y19 |
| pio[ 9] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 142 | W17 |
| pio[10] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 140 | U15 |
| pio[11] | GPIO | General purpose I/O [11:0] | Bi-Dir | 8 | Pull-up | 139 | V16 |
| PLL_amclk_dec | AOU | External audio out master clock | Input | | | 300 | A1 |
| PLL_amclk_enc | AIU | External audio in master clock | Input | | | 213 | C20 |
| PLL_bypass | mPLL | Main PLL disable / bypass | Input | | | 69 | T4 |
| PLL_clock | mPLL | Main PLL clock | Input | | | 68 | W1 |
| reset_ | Chip | Global reset | Input | | Schmitt trig. | 262 | B11 |
| rom_addr[ 0] | ROM | ROM address [21:0] | Output | 8 | | 280 | C8 |
| rom_addr[ 1] | ROM | ROM address [21:0] | Output | 8 | | 279 | D8 |
| rom_addr[ 2] | ROM | ROM address [21:0] | Output | 8 | | 277 | B7 |
| rom_addr[ 3] | ROM | ROM address [21:0] | Output | 8 | | 276 | E9 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| rom_addr[ 4] | ROM | ROM address [21:0] | Output | 8 | | 275 | A6 |
| rom_addr[ 5] | ROM | ROM address [21:0] | Output | 8 | | 274 | D9 |
| rom_addr[ 6] | ROM | ROM address [21:0] | Output | 8 | | 273 | B8 |
| rom_addr[ 7] | ROM | ROM address [21:0] | Output | 8 | | 272 | C9 |
| rom_addr[ 8] | ROM | ROM address [21:0] | Output | 8 | | 247 | C14 |
| rom_addr[ 9] | ROM | ROM address [21:0] | Output | 8 | | 246 | D13 |
| rom_addr[10] | ROM | ROM address [21:0] | Output | 8 | | 242 | C15 |
| rom_addr[11] | ROM | ROM address [21:0] | Output | 8 | | 240 | D14 |
| rom_addr[12] | ROM | ROM address [21:0] | Output | 8 | | 239 | A16 |
| rom_addr[13] | ROM | ROM address [21:0] | Output | 8 | | 238 | D15 |
| rom_addr[14] | ROM | ROM address [21:0] | Output | 8 | | 237 | B16 |
| rom_addr[15] | ROM | ROM address [21:0] | Output | 8 | | 236 | A17 |
| rom_addr[16] | ROM | ROM address [21:0] | Output | 8 | | 235 | C16 |
| rom_addr[17] | ROM | ROM address [21:0] | Output | 8 | | 234 | D16 |
| rom_addr[18] | ROM | ROM address [21:0] | Output | 8 | | 233 | B17 |
| rom_addr[19] | ROM | ROM address [21:0] | Output | 8 | | 232 | A18 |
| rom_addr[20] | ROM | ROM address [21:0] | Output | 8 | | 285 | C6 |
| rom_addr[21] | ROM | ROM address [21:0] | Output | 8 | | 284 | B5 |
| rom_ce_ | ROM | ROM chip enable | Output | 8 | | 278 | C7 |
| rom_data[0] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 270 | A8 |
| rom_data[1] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 269 | E10 |
| rom_data[2] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 268 | B9 |
| rom_data[3] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 267 | C10 |
| rom_data[4] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 266 | D10 |
| rom_data[5] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 265 | A9 |
| rom_data[6] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 264 | B10 |
| rom_data[7] | ROM | ROM data [7:0] | Bi-Dir | 4 | Pull-up | 263 | A10 |
| rom_oe_ | ROM | ROM output enable | Output | 8 | | 281 | A5 |
| rom_we_ | ROM | ROM write enable | Output | 8 | | 282 | B6 |
| sck_dec | AOU | Audio out clock | Output | 8 | | 282 | B6 |
| sck_enc | AIU | $I^2S$ Audio in clock | Bi-Dir | 8 | Pull-up | 250 | D12 |
| scl | ICI | ICI clock | Bi-Dir | 4 | Schmitt trig. | 136 | U14 |
| sd0_dec | AOU | Audio out channel 1 - $I^2S$ | Output | 8 | | 284 | B5 |
| sd0_enc | AIU | $I^2S$ Audio in channel 1 | Input | | Pull-up | 248 | B14 |
| sd1_dec | AOU | Audio out channel 2 - S/P-DIF | Output | 8 | | 285 | C6 |
| sd1_enc | AIU | $I^2S$ Audio in channel 2 | Input | | Pull-up | 249 | A14 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| sda | ICI | ICI data | Bi-Dir | 4 | Schmitt trig. | 137 | Y17 |
| sdram_dec_addr[ 0] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 114 | W11 |
| sdram_dec_addr[ 1] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 116 | U11 |
| sdram_dec_addr[ 2] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 118 | W12 |
| sdram_dec_addr[ 3] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 120 | T11 |
| sdram_dec_addr[ 4] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 122 | W13 |
| sdram_dec_addr[ 5] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 123 | V13 |
| sdram_dec_addr[ 6] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 121 | Y13 |
| sdram_dec_addr[ 7] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 119 | V12 |
| sdram_dec_addr[ 8] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 117 | Y12 |
| sdram_dec_addr[ 9] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 115 | Y11 |
| sdram_dec_addr[10] | DMIU | Decoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 113 | V11 |
| sdram_dec_ba[0] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 124 | U12 |
| sdram_dec_ba[1] | DMIU | Decoder SDRAM bank select[1:0] | Output | 8 | Slew rate cont. | 138 | Y18 |
| sdram_dec_cas_ | DMIU | Decoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 135 | W16 |
| sdram_dec_cke | DMIU | Decoder SDRAM clock enable | Output | 8 | Slew rate cont. | 126 | W14 |
| sdram_dec_clk | DMIU | Decoder SDRAM clock | Bi-Dir | 24 | | 127 | V14 |
| sdram_dec_cs_ | DMIU | Decoder SDRAM chip select | Output | 8 | Slew rate cont. | 128 | T12 |
| sdram_dec_data[ 0] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 112 | T10 |
| sdram_dec_data[ 1] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 111 | Y10 |
| sdram_dec_data[ 2] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 110 | W10 |
| sdram_dec_data[ 3] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 109 | V10 |
| sdram_dec_data[ 4] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 108 | U10 |
| sdram_dec_data[ 5] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 107 | Y9 |
| sdram_dec_data[ 6] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 106 | W9 |
| sdram_dec_data[ 7] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 105 | V9 |
| sdram_dec_data[ 8] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 104 | T9 |
| sdram_dec_data[ 9] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 103 | Y8 |
| sdram_dec_data[10] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 102 | W8 |
| sdram_dec_data[11] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 101 | V8 |
| sdram_dec_data[12] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 100 | U9 |
| sdram_dec_data[13] | DMIU | Decoder DRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 99 | Y7 |
| sdram_dec_data[14] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 98 | W7 |
| sdram_dec_data[15] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 97 | V7 |
| sdram_dec_data[16] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 96 | U8 |
| sdram_dec_data[17] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 95 | T8 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| sdram_dec_data[18] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 94 | Y6 |
| sdram_dec_data[19] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 93 | W6 |
| sdram_dec_data[20] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 92 | V6 |
| sdram_dec_data[21] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 91 | T7 |
| sdram_dec_data[22] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 90 | U7 |
| sdram_dec_data[23] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 89 | Y5 |
| sdram_dec_data[24] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 88 | U6 |
| sdram_dec_data[25] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 87 | W5 |
| sdram_dec_data[26] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 86 | Y4 |
| sdram_dec_data[27] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 85 | V5 |
| sdram_dec_data[28] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 84 | U5 |
| sdram_dec_data[29] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 83 | W4 |
| sdram_dec_data[30] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 82 | Y3 |
| sdram_dec_data[31] | DMIU | Decoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 81 | V4 |
| sdram_dec_dqm[0] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 129 | Y15 |
| sdram_dec_dqm[1] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 130 | W15 |
| sdram_dec_dqm[2] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 131 | Y16 |
| sdram_dec_dqm[3] | DMIU | Decoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 132 | U13 |
| sdram_dec_ras_ | DMIU | Decoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 133 | V15 |
| sdram_dec_we_ | DMIU | Decoder SDRAM write enable | Output | 8 | Slew rate cont. | 125 | Y14 |
| sdram_enc_addr[ 0] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 193 | J19 |
| sdram_enc_addr[ 1] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 195 | K16 |
| sdram_enc_addr[ 2] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 197 | H19 |
| sdram_enc_addr[ 3] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 199 | J17 |
| sdram_enc_addr[ 4] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 201 | G19 |
| sdram_enc_addr[ 5] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 202 | G18 |
| sdram_enc_addr[ 6] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 200 | G20 |
| sdram_enc_addr[ 7] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 198 | H18 |
| sdram_enc_addr[ 8] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 196 | H20 |
| sdram_enc_addr[ 9] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 194 | J18 |
| sdram_enc_addr[10] | EMIU | Encoder SDRAM address [10:0] | Output | 8 | Slew rate cont. | 192 | J20 |
| sdram_enc_ba[0] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 229 | A19 |
| sdram_enc_ba[1] | EMIU | Encoder SDRAM bank select [1:0] | Output | 8 | Slew rate cont. | 230 | B18 |
| sdram_enc_cas_ | EMIU | Encoder SDRAM column address strobe | Output | 8 | Slew rate cont. | 228 | A20 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| sdram_enc_cke | EMIU | Encoder SDRAM clock enable | Output | 8 | Slew rate cont. | 186 | L20 |
| sdram_enc_clk | EMIU | Encoder SDRAM clock | Bi-Dir | 24 | | 185 | L19 |
| sdram_enc_cs_ | EMIU | Encoder SDRAM chip select | Output | 8 | Slew rate cont. | 187 | L16 |
| sdram_enc_data[ 0] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 184 | L18 |
| sdram_enc_data[ 1] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 183 | L17 |
| sdram_enc_data[ 2] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 182 | M20 |
| sdram_enc_data[ 3] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 181 | M19 |
| sdram_enc_data[ 4] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 180 | M18 |
| sdram_enc_data[ 5] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 179 | M16 |
| sdram_enc_data[ 6] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 178 | N20 |
| sdram_enc_data[ 7] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 177 | N19 |
| sdram_enc_data[ 8] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 176 | N18 |
| sdram_enc_data[ 9] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 175 | M17 |
| sdram_enc_data[10] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 174 | P20 |
| sdram_enc_data[11] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 173 | P19 |
| sdram_enc_data[12] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 172 | P18 |
| sdram_enc_data[13] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 171 | N16 |
| sdram_enc_data[14] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 170 | N17 |
| sdram_enc_data[15] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 169 | R20 |
| sdram_enc_data[16] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 168 | R19 |
| sdram_enc_data[17] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 167 | R18 |
| sdram_enc_data[18] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 166 | P17 |
| sdram_enc_data[19] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 164 | R16 |
| sdram_enc_data[20] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 163 | T20 |
| sdram_enc_data[21] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 162 | R17 |
| sdram_enc_data[22] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 161 | T19 |
| sdram_enc_data[23] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 160 | U20 |
| sdram_enc_data[24] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 159 | T18 |
| sdram_enc_data[25] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 158 | T17 |
| sdram_enc_data[26] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 157 | U19 |
| sdram_enc_data[27] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 156 | V20 |
| sdram_enc_data[28] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 155 | U18 |
| sdram_enc_data[29] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 154 | V19 |
| sdram_enc_data[30] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 153 | W20 |
| sdram_enc_data[31] | EMIU | Encoder SDRAM data [31:0] | Bi-Dir | 8 | Slew rate cont. | 152 | Y20 |
| sdram_enc_dqm[0] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 188 | K18 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| sdram_enc_dqm[1] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 189 | K19 |
| sdram_enc_dqm[2] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 190 | K20 |
| sdram_enc_dqm[3] | EMIU | Encoder SDRAM I/O mask [3:0] | Output | 8 | Slew rate cont. | 191 | K17 |
| sdram_enc_ras_ | EMIU | Encoder SDRAM row address strobe | Output | 8 | Slew rate cont. | 227 | C18 |
| sdram_enc_we_ | EMIU | Encoder SDRAM write enable | Output | 8 | Slew rate cont. | 231 | C17 |
| tck | JTAG | Test clock | Input | | Pull-up | 63 | V1 |
| tdi | JTAG | Test data in | Input | | Pull-up | 64 | T3 |
| tdo | JTAG | Test data out | Output | 4 | Pull-up/ tri-state | 65 | R4 |
| tms | JTAG | Test mode select | Input | | Pull-up | 62 | U1 |
| trst_ | JTAG | Test reset | Input | | Pull-down | 61 | P4 |
| vbi_data[0] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 210 | E19 |
| vbi_data[1] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 209 | F18 |
| vbi_data[2] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 208 | H16 |
| vbi_data[3] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 207 | E20 |
| vbi_data[4] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 206 | H17 |
| vbi_data[5] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 205 | F19 |
| vbi_data[6] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 204 | F20 |
| vbi_data[7] | VIU | VBI data in [7:0] | Bi-Dir | 8 | Pull-up | 203 | J16 |
| vbi_data_en | VIU | VBI data enable | Input | | Pull-up | 211 | G17 |
| vou_clk | VOU | Video output clock 27 MHz | Output | 8 | | 271 | A7 |
| vou_vpo[0] | VOU | Video output data [7:0] | Output | 8 | | 280 | C8 |
| vou_vpo[1] | VOU | Video output data [7:0] | Output | 8 | | 279 | D8 |
| vou_vpo[2] | VOU | Video output data [7:0] | Output | 8 | | 277 | B7 |
| vou_vpo[3] | VOU | Video output data [7:0] | Output | 8 | | 276 | E9 |
| vou_vpo[4] | VOU | Video output data [7:0] | Output | 8 | | 275 | A6 |
| vou_vpo[5] | VOU | Video output data [7:0] | Output | 8 | | 274 | D9 |
| vou_vpo[6] | VOU | Video output data [7:0] | Output | 8 | | 273 | B8 |
| vou_vpo[7] | VOU | Video output data [7:0] | Output | 8 | | 272 | C9 |
| vpo[0] | VIU | Video input data [7:0] | Input | | | 259 | C11 |
| vpo[1] | VIU | Video input data [7:0] | Input | | | 258 | D11 |
| vpo[2] | VIU | Video input data [7:0] | Input | | | 257 | A12 |
| vpo[3] | VIU | Video input data [7:0] | Input | | | 256 | B12 |
| vpo[4] | VIU | Video input data [7:0] | Input | | | 255 | C12 |
| vpo[5] | VIU | Video input data [7:0] | Input | | | 254 | E12 |

**Table 12 I/O Signals, Sorted by Signal Name (Continued)**

| Signal Name | Module | Description | I / O | Drive (ma) | Drive Attributes | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|
| vpo[6] | VIU | Video input data [7:0] | Input | | | 253 | A13 |
| vpo[7] | VIU | Video input data [7:0] | Input | | | 252 | B13 |
| ws_dec | AOU | Audio out channel select | Output | 8 | | 281 | A5 |
| ws_enc | AIU | $I^2S$ Audio in channel select | Bi-Dir | 8 | Pull-up | 251 | C13 |

**Table 13 Power and Ground Connections**

| Signal Name | Module | Ball Coord | Pad No. | Drive (ma) | I / O | Description |
|---|---|---|---|---|---|---|
| CORE VDD | | D7 | 287 | | VDD | 1.8V |
| CORE VDD | | E13 | 245 | | VDD | 1.8V |
| CORE VDD | | E14 | 241 | | VDD | 1.8V |
| CORE VDD | | E8 | 283 | | VDD | 1.8V |
| CORE VDD | | F10 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | F12 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | F5 | 14 | | VDD | 1.8V |
| CORE VDD | | H15 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | H6 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | K15 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | L6 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | M15 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | N6 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | P16 | 165 | | VDD | 1.8V |
| CORE VDD | | P6 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | R11 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | R13 | P1 | | VDD | IVDD power ring 1.8V |
| CORE VDD | | R9 | P1 | | VDD | IVDD power ring 1.8V |
| d1PLL_dvdd | dPLL | E6 | 295 | 1 | AVDD | PVDD1P PLL 1.8V |
| d1PLL_dvss | dPLL | C4 | 294 | 1 | AVSS | PVSS1P PLL Ground |
| d1PLL_avdd | dPLL | E5 | 297 | 1 | AVDD | PVDD1P PLL 1.8V |
| d1PLL_avss | dPLL | B3 | 296 | 1 | AVSS | PVSS1P PLL Ground |
| d1PLL_pvdd | dPLL | B2 | 299 | 5 | PVDD | PVDD5P PLL Pad Ring 1.8V |
| d1PLL_pvss | dPLL | A2 | 298 | 5 | PVSS | PVSS5P PLL Pad Ring Ground |
| d2PLL_dvdd | dPLL | E7 | 289 | 1 | AVDD | PVDD1P PLL 1.8V |
| d2PLL_dvss | dPLL | D6 | 288 | 1 | AVSS | PVSS1P PLL Ground |
| d2PLL_avdd | dPLL | B4 | 291 | 1 | AVDD | PVDD1P PLL 1.8V |

**Table 13 Power and Ground Connections (Continued)**

| Signal Name | Module | Ball Coord | Pad No. | Drive (ma) | I / O | Description |
|---|---|---|---|---|---|---|
| d2PLL_avss | dPLL | C5 | 290 | 1 | AVSS | PVSS1P PLL Ground |
| d2PLL_pvdd | dPLL | D5 | 293 | 5 | PVDD | PVDD5P PLL Pad Ring 1.8V |
| d2PLL_pvss | dPLL | A3 | 292 | 5 | PVSS | PVSS5P PLL Pad Ring Ground |
| e1PLL_dvdd | ePLL | F17 | 215 | 1 | AVDD | PVDD1P PLL 1.8V |
| e1PLL_dvss | ePLL | E18 | 214 | 1 | AVSS | PVSS1P PLL Ground |
| e1PLL_avdd | ePLL | D19 | 217 | 1 | AVDD | PVDD1P PLL 1.8V |
| e1PLL_avss | ePLL | G16 | 216 | 1 | AVSS | PVSS1P PLL Ground |
| e1PLL_pvdd | ePLL | E17 | 219 | 5 | PVDD | PVDD5P PLL Pad Ring 1.8V |
| e1PLL_pvss | ePLL | B20 | 218 | 5 | PVSS | PVSS5P PLL Pad Ring Ground |
| e2PLL_dvdd | ePLL | F16 | 221 | 1 | AVDD | PVDD1P PLL 1.8V |
| e2PLL_dvss | ePLL | D18 | 220 | 1 | AVSS | PVSS1P PLL Ground |
| e2PLL_avdd | ePLL | B19 | 223 | 1 | AVDD | PVDD1P PLL 1.8V |
| e2PLL_avss | ePLL | C19 | 222 | 1 | AVSS | PVSS1P PLL Ground |
| e2PLL_pvdd | ePLL | E16 | 225 | 5 | PVDD | PVDD5P PLL Pad Ring 1.8V |
| e2PLL_pvss | ePLL | D17 | 224 | 5 | PVSS | PVSS5P PLL Pad Ring Ground |
| I/O VDD | | F11 | P4 | | VDD | OVDD3 power ring 3.3V |
| I/O VDD | | F13 | P4 | | VDD | OVDD3 power ring 3.3V |
| I/O VDD | | F15 | P5 | | VDD | PVDD power ring 3.3V |
| I/O VDD | | F6 | P5 | | VDD | PVDD power ring 3.3V |
| I/O VDD | | F8 | P4 | | VDD | OVDD3 power ring 3.3V |
| I/O VDD | | F9 | P4 | | VDD | OVDD3 power ring 3.3V |
| I/O VDD | | J15 | P3 | | VDD | OVDDM power ring 3.3V |
| I/O VDD | | J6 | P2 | | VDD | OVDDA power ring 3.3V |
| I/O VDD | | K6 | P2 | | VDD | OVDDA power ring 3.3V |
| I/O VDD | | L15 | P3 | | VDD | OVDDM power ring 3.3V |
| I/O VDD | | M6 | P2 | | VDD | OVDDA power ring 3.3V |
| I/O VDD | | N15 | P3 | | VDD | OVDDM power ring 3.3V |
| I/O VDD | | R10 | P3 | | VDD | OVDDM power ring 3.3V |

**Table 13 Power and Ground Connections (Continued)**

| Signal Name | Module | Ball Coord | Pad No. | Drive (ma) | I / O | Description |
|---|---|---|---|---|---|---|
| I/O VDD | | R12 | P3 | | VDD | OVDDM power ring 3.3V |
| I/O VDD | | R15 | P5 | | VDD | PVDD power ring 3.3V |
| I/O VDD | | R6 | P5 | | VDD | PVDD power ring 3.3V |
| I/O VDD | | R8 | P3 | | VDD | OVDDM power ring 3.3V |
| I/O VDD | | T13 | 134 | | VDD | 3.3V |
| I/O VDD | | T14 | 141 | | VDD | 3.3V |
| mPLL_dvdd | mPLL | V2 | 71 | 1 | AVDD | PVDD1P PLL 1.8V |
| mPLL_dvss | mPLL | U3 | 70 | 1 | AVSS | PVSS1P PLL Ground |
| mPLL_avdd | mPLL | W2 | 73 | 1 | AVDD | PVDD1P PLL 1.8V |
| mPLL_avss | mPLL | R5 | 72 | 1 | AVSS | PVSS1P PLL Ground |
| mPLL_pvdd | mPLL | T5 | 75 | 5 | PVDD | PVDD5P PLL Pad Ring 1.8V |
| mPLL_pvss | mPLL | U4 | 74 | 5 | PVSS | PVSS5P PLL Pad Ring Ground |
| VSS | | H10 | | | VSS | Ground / Thermal |
| VSS | | H11 | | | VSS | Ground / Thermal |
| VSS | | H12 | | | VSS | Ground / Thermal |
| VSS | | H13 | | | VSS | Ground / Thermal |
| VSS | | H8 | | | VSS | Ground / Thermal |
| VSS | | H9 | | | VSS | Ground / Thermal |
| VSS | | J10 | | | VSS | Ground / Thermal |
| VSS | | J11 | | | VSS | Ground / Thermal |
| VSS | | J12 | | | VSS | Ground / Thermal |
| VSS | | J13 | | | VSS | Ground / Thermal |
| VSS | | J8 | | | VSS | Ground / Thermal |
| VSS | | J9 | | | VSS | Ground / Thermal |
| VSS | | K10 | | | VSS | Ground / Thermal |
| VSS | | K11 | | | VSS | Ground / Thermal |
| VSS | | K12 | | | VSS | Ground / Thermal |
| VSS | | K13 | | | VSS | Ground / Thermal |

**Table 13 Power and Ground Connections (Continued)**

| Signal Name | Module | Ball Coord | Pad No. | Drive (ma) | I / O | Description |
|---|---|---|---|---|---|---|
| VSS | | K8 | | | VSS | Ground / Thermal |
| VSS | | K9 | | | VSS | Ground / Thermal |
| VSS | | L10 | | | VSS | Ground / Thermal |
| VSS | | L11 | | | VSS | Ground / Thermal |
| VSS | | L12 | | | VSS | Ground / Thermal |
| VSS | | L13 | | | VSS | Ground / Thermal |
| VSS | | L8 | | | VSS | Ground / Thermal |
| VSS | | L9 | | | VSS | Ground / Thermal |
| VSS | | M10 | | | VSS | Ground / Thermal |
| VSS | | M11 | | | VSS | Ground / Thermal |
| VSS | | M12 | | | VSS | Ground / Thermal |
| VSS | | M13 | | | VSS | Ground / Thermal |
| VSS | | M8 | | | VSS | Ground / Thermal |
| VSS | | M9 | | | VSS | Ground / Thermal |
| VSS | | N10 | | | VSS | Ground / Thermal |
| VSS | | N11 | | | VSS | Ground / Thermal |
| VSS | | N12 | | | VSS | Ground / Thermal |
| VSS | | N13 | | | VSS | Ground / Thermal |
| VSS | | N8 | | | VSS | Ground / Thermal |
| VSS | | N9 | | | VSS | Ground / Thermal |

**Table 14 Signal Multiplexing Scheme[1]**

| Signal Name | Signal Name 2 | Module | Module 2 | Pad No. | Ball Coord. |
|---|---|---|---|---|---|
| cdo[0] | rom_addr[12] | Mux | ROM | 239 | A16 |
| cdo[1] | rom_addr[13] | Mux | ROM | 238 | D15 |
| cdo[2] | rom_addr[14] | Mux | ROM | 237 | B16 |
| cdo[3] | rom_addr[15] | Mux | ROM | 236 | A17 |
| cdo[4] | rom_addr[16] | Mux | ROM | 235 | C16 |
| cdo[5] | rom_addr[17] | Mux | ROM | 234 | D16 |
| cdo[6] | rom_addr[18] | Mux | ROM | 233 | B17 |
| cdo[7] | rom_addr[19] | Mux | ROM | 232 | A18 |
| cdo_clk | rom_addr[11] | Mux | ROM | 240 | D14 |
| cdo_sop | rom_addr[10] | Mux | ROM | 242 | C15 |
| cdo_valid | rom_addr[9] | Mux | ROM | 246 | D13 |
| fifo_level | rom_addr[8] | Mux | ROM | 247 | C14 |
| sck_dec | rom_we_ | AOU | ROM | 282 | B6 |
| sd0_dec | rom_addr[21] | AOU | ROM | 284 | B5 |
| sd1_dec | rom_addr[20] | AOU | ROM | 285 | C6 |
| vbi_data[0] | ejtag_pcst3[0] | VIU | EJTAG | 210 | E19 |
| vbi_data[1] | ejtag_pcst3[1] | VIU | EJTAG | 209 | F18 |
| vbi_data[2] | ejtag_pcst3[2] | VIU | EJTAG | 208 | H16 |
| vbi_data[3] | ejtag_pcst4[0] | VIU | EJTAG | 207 | E20 |
| vbi_data[4] | ejtag_pcst4[1] | VIU | EJTAG | 206 | H17 |
| vbi_data[5] | ejtag_pcst4[2] | VIU | EJTAG | 205 | F19 |
| vou_vpo[0] | rom_addr[0] | VOU | ROM | 280 | C8 |
| vou_vpo[1] | rom_addr[1] | VOU | ROM | 279 | D8 |
| vou_vpo[2] | rom_addr[2] | VOU | ROM | 277 | B7 |
| vou_vpo[3] | rom_addr[3] | VOU | ROM | 276 | E9 |
| vou_vpo[4] | rom_addr[4] | VOU | ROM | 275 | A6 |
| vou_vpo[5] | rom_addr[5] | VOU | ROM | 274 | D9 |
| vou_vpo[6] | rom_addr[6] | VOU | ROM | 273 | B8 |
| vou_vpo[7] | rom_addr[7] | VOU | ROM | 272 | C9 |
| ws_dec | rom_oe_ | AOU | ROM | 281 | A5 |

1. Except host interface signals. See Table 16 on page 144, Table 17 on page 145.

**Table 15 Board-Level Requirements for Unused Input Pins [1]**

| Pad No. | Ball Coord. | Signal Name | Drive Attributes | External Connection (if pin is not used) |
|---|---|---|---|---|
| 1 | D4 | cdi[7] | Pull-up | OK to leave floating (no-connect) |
| 2 | C3 | cdi[6] | Pull-up | OK to leave floating (no-connect) |
| 3 | B1 | cdi[5] | Pull-up | OK to leave floating (no-connect) |
| 4 | C2 | cdi[4] | Pull-up | OK to leave floating (no-connect) |
| 5 | C1 | cdi[3] | Pull-up | OK to leave floating (no-connect) |
| 6 | D2 | cdi[2] | Pull-up | OK to leave floating (no-connect) |
| 7 | D1 | cdi[1] | Pull-up | OK to leave floating (no-connect) |
| 8 | D3 | cdi[0] | Pull-up | OK to leave floating (no-connect) |
| 9 | E4 | cdi_valid | Pull-up | OK to leave floating (no-connect) |
| 10 | F4 | cdi_clk | Pull-up | OK to leave floating (no-connect) |
| 61 | P4 | trst_ | Pull-down | As required by emulator |
| 62 | U1 | tms | Pull-up | As required by emulator |
| 63 | V1 | tck | Pull-up | As required by emulator |
| 64 | T3 | tdi | Pull-up | As required by emulator |
| 68 | W1 | PLL_clk | | External pull-down |
| 69 | T4 | PLL_bypass | | External pull-down |
| 203 | J16 | vbi_data[7] | Pull-up | OK to leave floating (no-connect) |
| 204 | F20 | vbi_data[6] | Pull-up | OK to leave floating (no-connect) |
| 205 | F19 | vbi_data[5] | Pull-up | OK to leave floating (no-connect) |
| 206 | H17 | vbi_data[4] | Pull-up | OK to leave floating (no-connect) |
| 207 | E20 | vbi_data[3] | Pull-up | OK to leave floating (no-connect) |
| 208 | H16 | vbi_data[2] | Pull-up | OK to leave floating (no-connect) |
| 209 | F18 | vbi_data[1] | Pull-up | OK to leave floating (no-connect) |
| 210 | E19 | vbi_data[0] | Pull-up | OK to leave floating (no-connect) |
| 211 | G17 | vbi_data_en | Pull-up | OK to leave floating (no-connect) |
| 213 | C20 | PLL_amclk_enc | | Tie to ground |
| 226 | E15 | clk_vbi | Pull-up | OK to leave floating (no-connect) |
| 243 | B15 | excd_clk | Pull-down | OK to leave floating (no-connect) |
| 244 | A15 | excd_rd | Pull-up | OK to leave floating (no-connect) |
| 248 | B14 | sd0_enc | Pull-up | OK to leave floating (no-connect) |
| 249 | A14 | sd1_enc | Pull-up | OK to leave floating (no-connect) |
| 252 | B13 | vpo[7] | | Tie to ground |
| 253 | A13 | vpo[6] | | Tie to ground |
| 254 | E12 | vpo[5] | | Tie to ground |
| 255 | C12 | vpo[4] | | Tie to ground |

**Table 15 Board-Level Requirements for Unused Input Pins [1] (Continued)**

| Pad No. | Ball Coord. | Signal Name | Drive Attributes | External Connection (if pin is not used) |
|---|---|---|---|---|
| 256 | B12 | vpo[3] | | Tie to ground |
| 257 | A12 | vpo[2] | | Tie to ground |
| 258 | D11 | vpo[1] | | Tie to ground |
| 259 | C11 | vpo[0] | | Tie to ground |
| 260 | A11 | clk_27 | | Tie to ground |
| 261 | E11 | pcr_clk | | Tie to ground |
| 262 | B11 | reset_ | | Tie to Vcc |
| 300 | A1 | PLL_amclk_dec | | Tie to ground |

1. Except host interface signals. See Table 16 on page 144, Table 17 on page 145.

**Table 16 Host Interface, Address/Data Bus**

| Host Interface Mode | | | | | | Pad No. | Ball Coord. | What to do with Unused Pin |
|---|---|---|---|---|---|---|---|---|
| PCI | Dir. | Motorola | Dir. | Intel | Dir. | | | |
| pci_ad[0] | I/O | host_hiu_data[0] | I/O | intel_ad[0] | I/O | 60 | T2 | Tie to ground |
| pci_ad[1] | I/O | host_hiu_data[1] | I/O | intel_ad[1] | I/O | 59 | N5 | Tie to ground |
| pci_ad[2] | I/O | host_hiu_data[2] | I/O | intel_ad[2] | I/O | 58 | R3 | Tie to ground |
| pci_ad[3] | I/O | host_hiu_data[3] | I/O | intel_ad[3] | I/O | 57 | N4 | Tie to ground |
| pci_ad[4] | I/O | host_hiu_data[4] | I/O | intel_ad[4] | I/O | 56 | T1 | Tie to ground |
| pci_ad[5] | I/O | host_hiu_data[5] | I/O | intel_ad[5] | I/O | 55 | R2 | Tie to ground |
| pci_ad[6] | I/O | host_hiu_data[6] | I/O | intel_ad[6] | I/O | 54 | R1 | Tie to ground |
| pci_ad[7] | I/O | host_hiu_data[7] | I/O | intel_ad[7] | I/O | 53 | M5 | Tie to ground |
| pci_ad[8] | I/O | host_hiu_data[8] | I/O | intel_ad[8] | I/O | 51 | P2 | Tie to ground |
| pci_ad[9] | I/O | host_hiu_data[9] | I/O | intel_ad[9] | I/O | 50 | P1 | Tie to ground |
| pci_ad[10] | I/O | host_hiu_data[10] | I/O | intel_ad[10] | I/O | 49 | M4 | Tie to ground |
| pci_ad[11] | I/O | host_hiu_data[11] | I/O | intel_ad[11] | I/O | 48 | N3 | Tie to ground |
| pci_ad[12] | I/O | host_hiu_data[12] | I/O | intel_ad[12] | I/O | 47 | N2 | Tie to ground |
| pci_ad[13] | I/O | host_hiu_data[13] | I/O | intel_ad[13] | I/O | 46 | N1 | Tie to ground |
| pci_ad[14] | I/O | host_hiu_data[14] | I/O | intel_ad[14] | I/O | 45 | L5 | Tie to ground |
| pci_ad[15] | I/O | host_hiu_data[15] | I/O | intel_ad[15] | I/O | 44 | M3 | Tie to ground |
| pci_ad[16] | I/O | host_hiu_addr[0] | In | | | 43 | M2 | Tie to ground |
| pci_ad[17] | I/O | host_hiu_addr[1] | In | | | 31 | J2 | Tie to ground |
| pci_ad[18] | I/O | host_hiu_addr[2] | In | | | 30 | J3 | Tie to ground |
| pci_ad[19] | I/O | host_hiu_addr[3] | In | | | 29 | J5 | Tie to ground |
| pci_ad[20] | I/O | host_hiu_addr[4] | In | | | 28 | H1 | Tie to ground |
| pci_ad[21] | I/O | host_hiu_addr[5] | In | | | 27 | H2 | Tie to ground |
| pci_ad[22] | I/O | host_hiu_addr[6] | In | | | 26 | H3 | Tie to ground |
| pci_ad[23] | I/O | host_hiu_addr[7] | In | | | 25 | J4 | Tie to ground |
| pci_ad[24] | I/O | host_hiu_addr[8] | In | | | 24 | G1 | Tie to ground |
| pci_ad[25] | I/O | host_hiu_addr[9] | In | | | 21 | H4 | Tie to ground |
| pci_ad[26] | I/O | host_hiu_addr[10] | In | | | 20 | H5 | Tie to ground |
| pci_ad[27] | I/O | host_hiu_addr[11] | In | | | 19 | F1 | Tie to ground |
| pci_ad[28] | I/O | host_hiu_addr[12] | In | | | 18 | F2 | Tie to ground |
| pci_ad[29] | I/O | host_hiu_addr[13] | In | | | 17 | F3 | Tie to ground |
| pci_ad[30] | I/O | host_hiu_addr[14] | In | | | 16 | G4 | Tie to ground |
| pci_ad[31] | I/O | host_hiu_addr[15] | In | | | 15 | G5 | Tie to ground |

### Table 17 Host Interface Bus Control Signals [1]

| Host Interface Mode | | | | | | | | | Pad No. | Ball Coord. |
|---|---|---|---|---|---|---|---|---|---|---|
| PCI | | | Motorola | | | Intel | | | | |
| Signal | Dir. | Tie to | Signal | Dir. | Tie to | Signal | Dir. | Tie to | | |
| pci_cbe_[0] | I/O | Vcc | host_hiu_as_ | In | Vcc | intel_as_ale_ | In | Vcc | 52 | P3 |
| pci_cbe_[1] | I/O | Vcc | host_hiu_cs_ | In | Vcc | intel_cs_ | In | Vcc | 42 | M1 |
| pci_cbe_[2] | I/O | Vcc | host_hiu_rw_ | In | Vcc | intel_wr_ | Int | Vcc | 32 | J1 |
| pci_cbe_[3] | I/O | Vcc | hiu_host_cdo_req_ | Out | - | intel_cdo_req_ | Out | - | 22 | G3 |
| pci_clk | In | gnd | | | gnd | | | gnd | 12 | E2 |
| pci_devsel_ | I/O | Vcc | host_hiu_cdi_ack_ | In | Vcc | intel_cdi_ack_ | In | Vcc | 36 | K1 |
| pci_frame_ | I/O | Vcc | | | Vcc | intel_rd_ | In | Vcc | 33 | K4 |
| pci_gnt_ | In | Vcc | | | Vcc | | | Vcc | 38 | L3 |
| pci_idsel | In | gnd | | | gnd | | | gnd | 23 | G2 |
| pci_inta_ | Out | Vcc | int_ | Out | - | int_ | Out | - | 11 | E3 |
| pci_irdy_ | I/O | Vcc | | | Vcc | | | Vcc | 34 | K3 |
| pci_par | I/O | gnd | | | gnd | | | gnd | 41 | L4 |
| pci_perr_ | I/O | Vcc | host_hiu_cdo_ack_ | In | Vcc | intel_cdo_ack_ | In | Vcc | 39 | L2 |
| pci_req_ | I/O | Vcc | | | Vcc | | | Vcc | 13 | E1 |
| pci_serr_ | I/O | Vcc | hiu_host_dtack_ | Out | - | intel_dtack_ | Out | - | 40 | L1 |
| pci_stop_ | I/O | Vcc | hiu_host_cdi_req_ | Out | - | intel_cdi_req_ | Out | - | 37 | K5 |
| pci_trdy_ | I/O | Vcc | | | Vcc | | | Vcc | 35 | K2 |

1. **In PCI mode:**
   Normally, all pins are used.
   However,
   Unused input-only pins (if any) must be tied inactive (tied to ground if active high, tied to Vcc if active low).
   Unused I/O pins (if any) may be tied inactive or left floating (pins are tri-state)
   **In Motorola or Intel mode:**
   Unused input-only pins must be tied inactive (tied to ground if active high, tied to Vcc if active low).
   Unused outputs are left floating.
   Unused PCI-only, input-only pins must be tied inactive (for example, pci_clk must be tied to ground).
   Unused PCI-only I/O pins may be tied inactive or left floating (e.g., pci_irdy_ may be tied to Vcc, pci_par. may be tied to ground).
   **In no-host mode:**
   that is, when the chip is booted from ROM and is not connected to an external host,
   The rom_data pins must be set to boot from ROM (see Table 5 on page 49), and
   The unused pins of the host interface must be set as shown in Table 16 on page 144 and in the Motorola or Intel column above.

# CHAPTER 10 Electrical Characteristics

This chapter summarizes the following information about the VW2010 chip's electrical properties:

- Maximum input power and environmental ratings
- DC Characteristics
- AC timing diagrams and parameters

*Note:* The following information is preliminary and subject to change based on simulation data and actual measurements for the final version of this document.



## Absolute Maximum Ratings

The following table shows the maximum ratings of the VW2010. Exposure beyond the settings in the following table will result in unpredictable behavior.

**Table 18 Maximum Ratings**

| Parameter | Value |
|---|---|
| I/O supply voltage ($V_{DD}$) | 3.3V ± 10% |
| Core voltage ($V_{CORE}$) | 1.8V ± 10% |
| PLL analog supply voltage | 3.3V ± 10% |
| PLL digital supply voltage | 3.3V ± 10% |
| Storage temperature range | -55 to 120°C |

**Table 18 Maximum Ratings (Continued)**

| | |
|---|---|
| Operating temperature range | 0 to 75°C |
| Soldering reflow temperature | 200°C for 5 seconds |
| Power Consumption - Encoder only | 0.8 W |
| Power Consumption - Encoder + Decoder | 1.6 W |

b

***Power-On Sequence***

The proper power-on sequence is as follows:

- Power on the core voltage Core voltage ($V_{CORE}$), 1.8 VDC first.
- Then power on the I/O supply voltage ($V_{DD}$), 3.3 VDC.
- The delay between $V_{CORE}$ and $V_{DD}$ should be about a millisecond.

***Power-Off Sequence***

The proper power-off sequence is as follows:

- Power off the I/O supply voltage ($V_{DD}$), 3.3 VDC first.
- Then power off the core voltage Core voltage ($V_{CORE}$), 1.8 VDC.
- The delay between $V_{DD}$ and $V_{CORE}$ should be about a millisecond.



## DC Characteristics

The following table shows the DC limits of the VW2010.

*Note:* The parameters and limits are not 100% tested; they are guaranteed by design characterization.

**Table 19 DC Characteristics**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Leakage current | Hi-Z output driven to 0.0V and 5.25V | (-10) | | (10) | ìA |
| $V_{OH}$ | High-level output voltage | $V_{DD}$=3.3V, $I_{OH}$= -2ma | 2.4 | - | - | V |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$=MIN $I_{OL}$=2ma | - | - | 0.4 | V |
| $V_{IH}$ | High-level input voltage | $V_{DD}$=min | 2.4 | - | - | V |
| $V_{IL}$ | Low-level input voltage | $V_{DD}$= max | - | - | 0.8 | V |

## AC Timing Characteristics

The following sections specify the AC timing characteristics of the VW2010; see:

## HIU-Motorola Mode

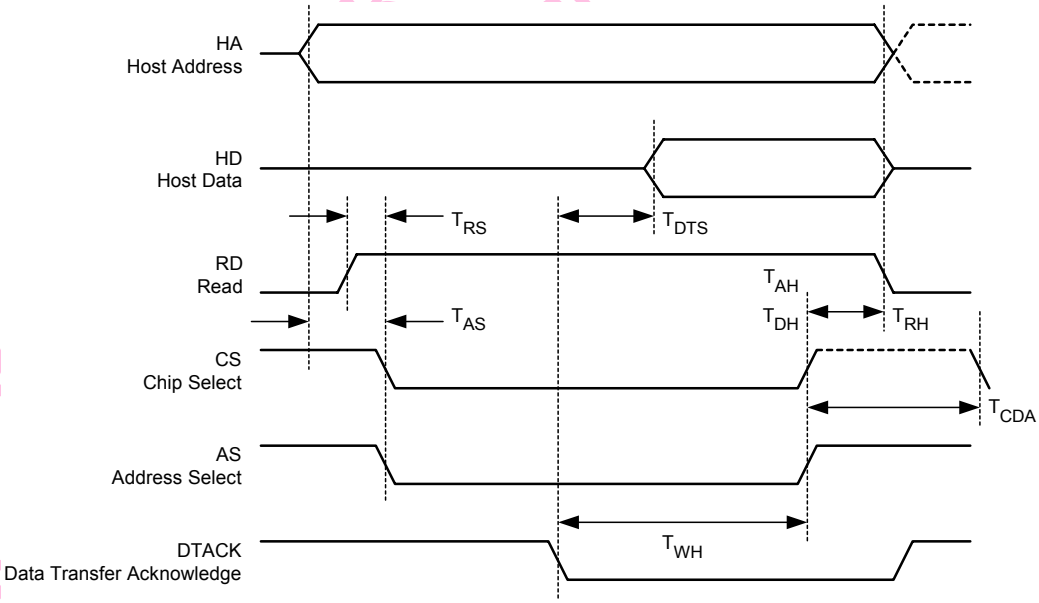


**Figure 34 Host Read Timing, HIU-Motorola Mode**

**Table 20 Host Read Timing Parameters, HIU-Motorola Mode**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AS}$ | Address setup time before Chip Select is asserted | 2 | | | ns |
| $T_{AH}$ | Address hold time after Chip Select is deasserted | 5 | | | ns |
| $T_{RS}$ | Read/write setup time before Chip Select assertion | 2 | | | ns |
| $T_{RH}$ | Read/write hold time after Chip Select is deasserted | 2 | | | ns |
| $T_{DTS}$ | Dtack asserted to data valid | | | 5 | ns |
| $T_{DH}$ | Chip Select deasserted to Data Invalid | 5 | | | ns |
| $T_{CDA}$ | Chip Select deassertion to the next Chip Select assertion | 33 | | | ns |

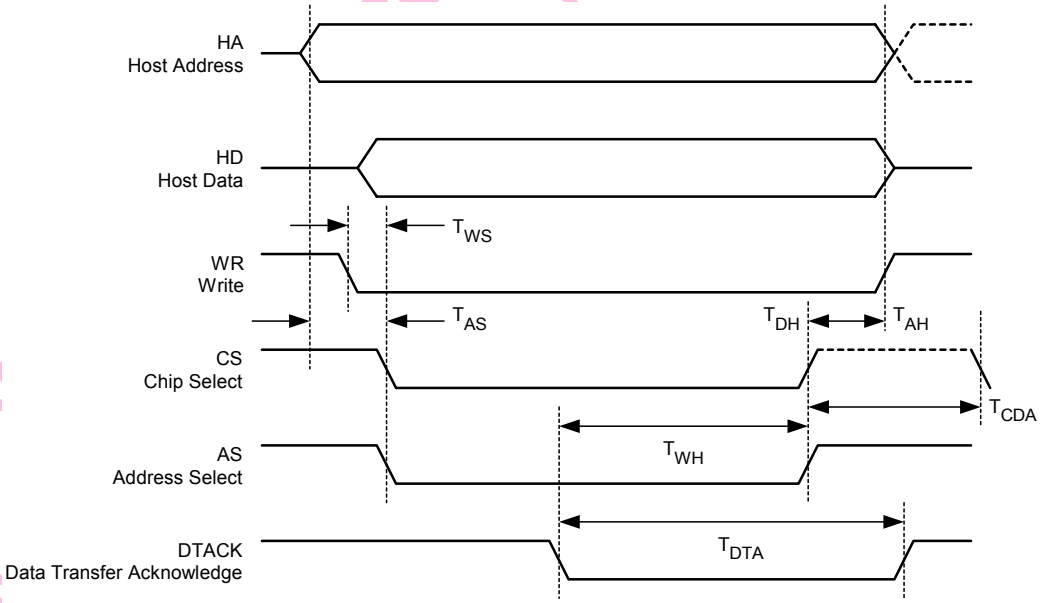


**Figure 35 Host Write Timing, HIU-Motorola Mode**

**Table 21 Host Write Timing Parameters, HIU Motorola-Mode**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AS}$ | Address setup time before Chip Select is asserted | 2 | | | ns |
| $T_{AH}$ | Address hold time after Chip Select is deasserted | 5 | | | ns |
| $T_{CDA}$ | Time between Chip Select deassertion until the next Chip Select assertion | 33 | | | ns |
| $T_{WS}$ | Read/write setup time before Chip Select assertion | 2 | | | ns |
| $T_{WH}$ | Dtack assert hold time before Chip Select is deasserted | 45 | | | ns |
| $T_{DH}$ | Data hold time after Chip Select is deasserted | 1 | | | ns |
| $T_{DTA}$ | Dtack assertion time | 66 | | | ns |

For additional details, see a Motorola specification such as a 68K series manual.

## HIU-Intel Mode

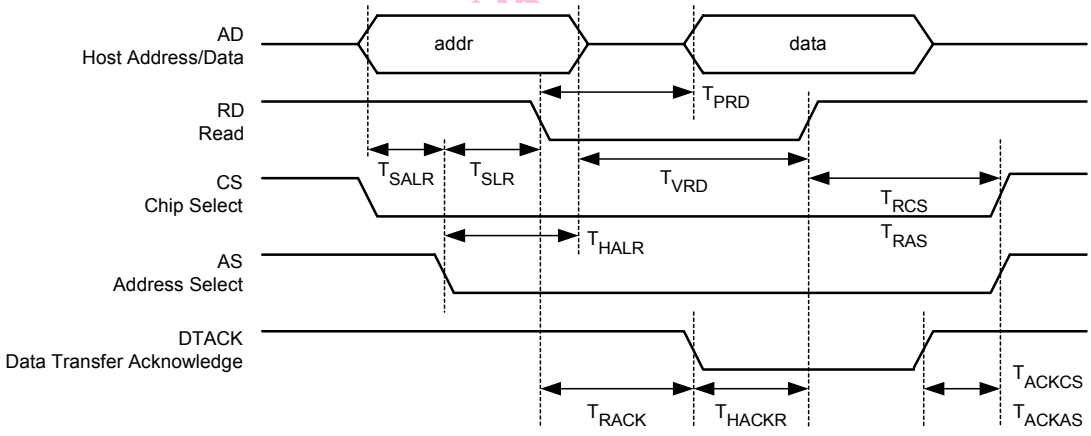


**Figure 36 Host Read Timing, HIU-Intel Mode**

**Table 22 Host Read Timing Parameters, HIU-Intel Mode**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SALR}$ | Address set up time | 20 | | | ns |
| $T_{SLR}$ | Read set up time | 20 | | | ns |
| $T_{HALR}$ | Address hold time | 20 | | | ns |
| $T_{PRD}$ | Data delay time | | 60 | 120 | ns |
| $T_{VRD}$ | Read pulse width | | $T_{PRD}$ + 10 | | ns |
| $T_{RACK}$ | DTACK delay from Read | | 60 | 120 | ns |
| $T_{HACKR}$ | Data hold time | | 10 | | ns |
| $T_{RAS}$ | AS delay from Read | | 20 | | ns |
| $T_{RCS}$ | CS delay from Read | | 20 | | ns |
| $T_{ACKAS}$ | AS delay from DTACK | 5 | | | ns |
| $T_{ACKCS}$ | CS delay from DTACK | 5 | | | ns |

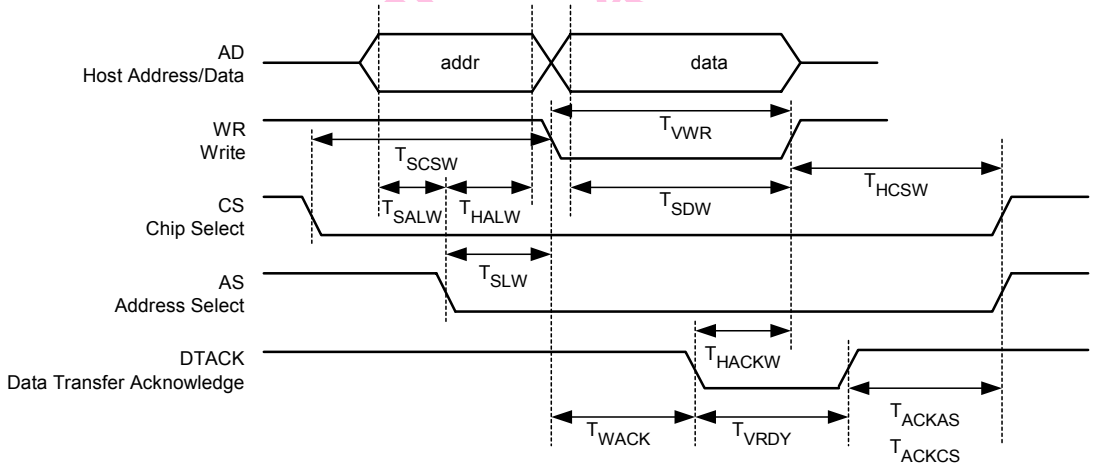


**Figure 37 Host Write Timing, HIU-Intel Mode**

**Table 23 Host Write Timing Parameters, HIU Intel-Mode**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SALW}$ | Address set up time | 20 | | | ns |
| $T_{SLW}$ | Write set up time from AS | 20 | | | ns |
| $T_{HALW}$ | Address hold time | 20 | | | ns |
| $T_{SCSW}$ | Write set up time from CS | 40 | | | ns |
| $T_{HCSW}$ | CS hold time | | 20 | | ns |
| $T_{SDW}$ | Data valid time | | $T_{WACK}$ + 10 | | ns |
| $T_{VWR}$ | Write pulse width | | $T_{WACK}$ + 10 | | ns |
| $T_{VRDY}$ | DTACK duration | | 60 | | ns |
| $T_{WACK}$ | DTACK delay from Write | | 60 | 120 | ns |
| $T_{HACKW}$ | Data hold time | | 10 | | ns |
| $T_{ACKAS}$ | AS delay from DTACK | 5 | | | ns |
| $T_{ACKCS}$ | CS delay from DTACK | 5 | | | ns |

## HIU-PCI Mode

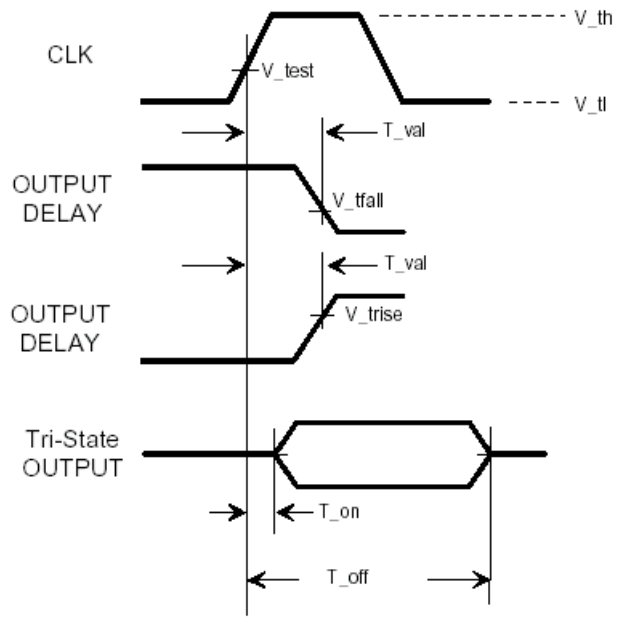


**Figure 38 Host Read Timing, HIU-PCI Mode**

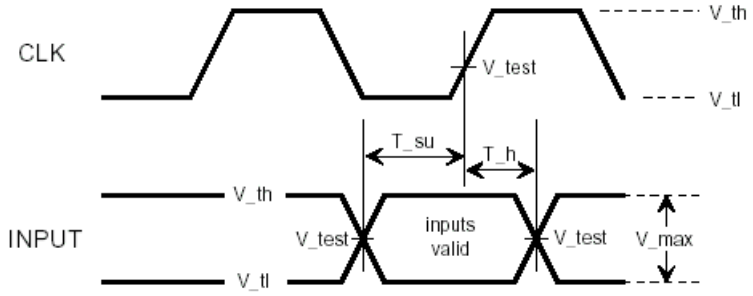


**Figure 39 Host Write Timing, HIU-PCI Mode**

**Table 24 Timing Parameters, HIU-PCI Mode**

| | | 66 MHz | | 33 MHz[7] | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** |
| $T_{val}$ | **CLK** to Signal Valid Delay - bused signals | 2 | 6 | 2 | 11 | ns |
| $T_{val}(ptp)$ | **CLK** to Signal Valid Delay - point to point signals | 2 | 6 | 2 | 12 | ns |
| $T_{on}$ | Float to Active Delay | 2 | | 2 | | ns |
| $T_{off}$ | Active to Float Delay | | 14 | | 28 | ns |
| $T_{su}$ | Input Setup Time to **CLK** - bused signals | 3 | | 7 | | ns |
| $T_{su}(ptp)$ | Input Setup Time to **CLK** - point to point signals | 5 | | 10,12 | | ns |
| $T_h$ | Input Hold Time from **CLK** | 0 | | 0 | | ns |
| $T_{rst}$ | Reset Active Time after power stable | 1 | | 1 | | ms |

***PCI Read Transaction*** For timing diagrams and descriptions, see the PCI Local Bus Specification, version 2.2, from PCISIG.

***PCI Write Transaction*** For timing diagrams and descriptions, see the PCI Local Bus Specification, version 2.2, from PCISIG.

## Video Input

*Note:* Not 100% tested; guaranteed by design characterization

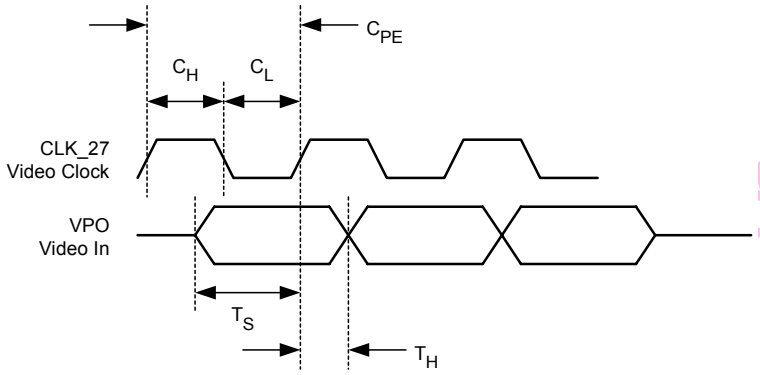


**Figure 40 Video Input Timing**

**Table 25 Video Input Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{PE}$ | 27 MHz clock period | 18.5 | | | ns |
| $C_H$ | High time | 7.0 | | | ns |
| $C_L$ | Low time | 7.0 | | | ns |
| $T_S$ | Video data setup time | 5.0 | | | ns |
| $T_H$ | Video data hold time | 2.0 | | | ns |

For additional details, see the ITU-R.BT.656 specification.

## Video Output

*Note:* Not 100% tested; guaranteed by design characterization

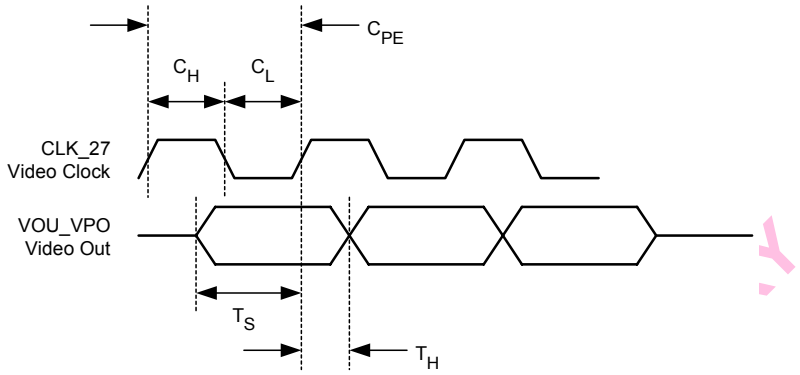


**Figure 41 Video Output Timing**

**Table 26 Video Output Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{PE}$ | 27 MHz clock period | 18.5 | | | ns |
| $C_H$ | High time | 7.0 | | | ns |
| $C_L$ | Low time | 7.0 | | | ns |
| $T_S$ | Video data setup time | 5.0 | | | ns |
| $T_H$ | Video data hold time | 2.0 | | | ns |

For additional details, see the ITU-R.BT.656 specification.

## VBI Input

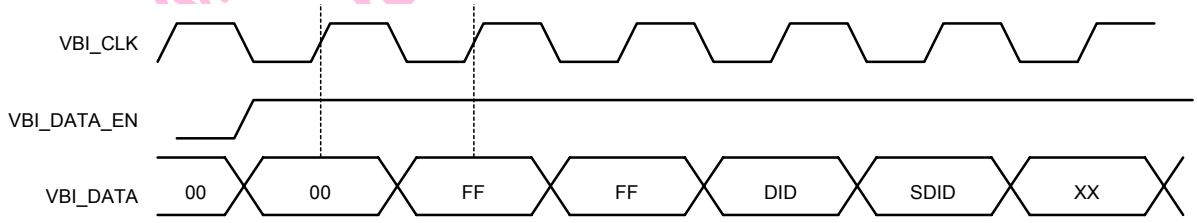


**Figure 42 VBI Input Timing**

**Table 27 VBI Input Timing Parameters**

to be added

For additional details see the data sheet for a device such as the Philips Semiconductors SAA7114H PAL/NTSC/SECAM video decoder.

## Audio Input

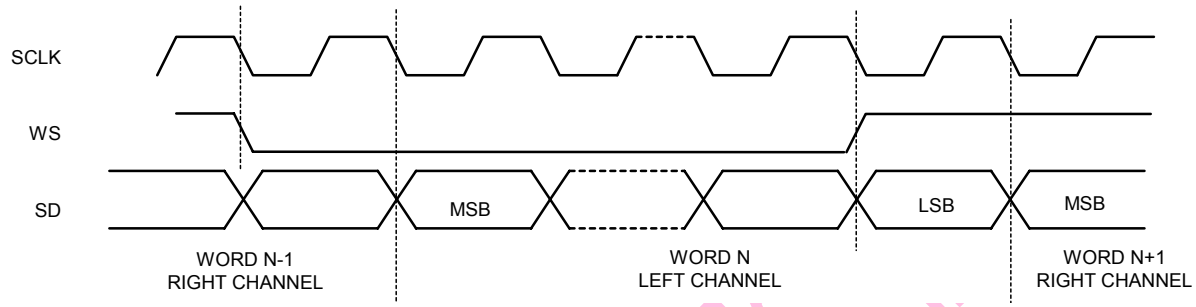


**Figure 43 Basic I²S Bus Timing**

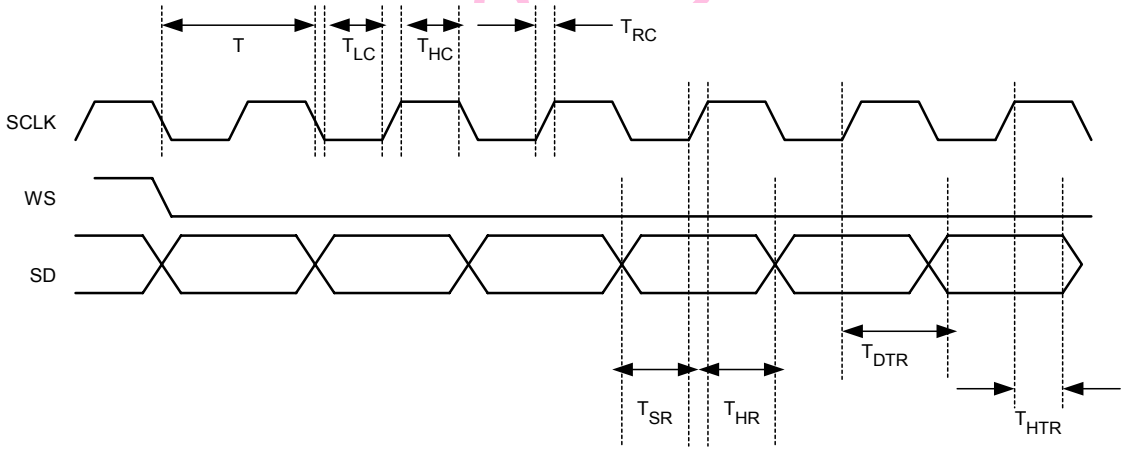


**Figure 44 I²S Transmitter and Receiver Timing**

**Table 28 I²S Timing Parameters**

| Symbol | Parameter | Value |
|---|---|---|
| T | Clock period | |
| $T_{tr}$ | Minimum clock period for transmitter | $T > T_{tr}$ |
| Tr | Minimum clock period for receiver | $T > T_r$ |
| $t_{LC}$ | | |
| $t_{HC}$ | | |
| $t_{RC}$ | | |
| $t_{sr}$ | | |
| $t_{hr}$ | | |
| $t_{htr}$ | | |
| $t_{dtr}$ | | |

For additional details see the Philips I²S bus specification.

## Audio Output

### *I²S Bus Timing*

See "Audio Input" on page 157.

### *S/P-DIF Timing*

to be added -- need info

**Figure 45 S/P-DIF Audio Output Timing**

**Table 29 S/P-DIF Audio Output Timing Parameters**

to be added

## Compressed Data Input (CDI)

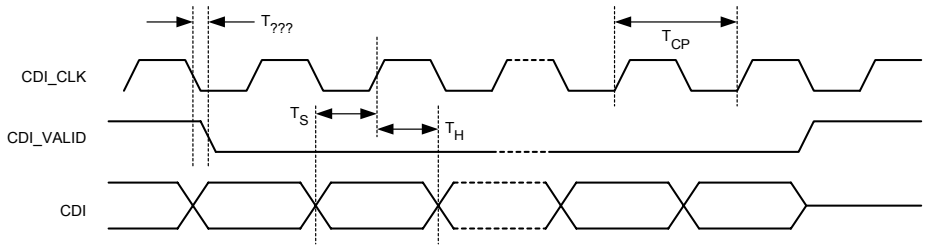


**Figure 46 Compressed Data Input Timing**

*Note:* CDI_VALID is from falling edge of CDI_CLK.

**Table 30 Video Demux / CDI Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{PF}$ | CDIO_CLK period | 18.5 | | | ns |
| $T_S$ | Data setup time | 3 | | | ns |
| $T_H$ | Data hold time | 5 | | | ns |

### *CDI via Host Interface*

The external host can write compressed data (CDI) to the VW2010 using the host interface protocol as follows:

1. The VW2010 asserts CDI_REQ (indicates the VW2010 is ready to receive compressed data).
2. The external host asserts CDI_ACK and drives data on HIU_DATA[15:0] (the external host is ready to write data on the HIU_DATA bus).
3. The VW2010 asserts DTACK when it has read the data on HIU_DATA[15:0].
4. The external host deasserts CDI_ACK and at the same time stops driving the HIU_DATA bus (terminates the write cycle).
5. The VW2010 de-asserts DTACK.
6. The VW2010 de-asserts CDI_REQ.

*Note:* This signal can be kept active until all data transfer cycles are completed.

7. Repeat 1-6 for each data transfer.

## Compressed Data Output (CDO)

### *CDO via CDO Port*

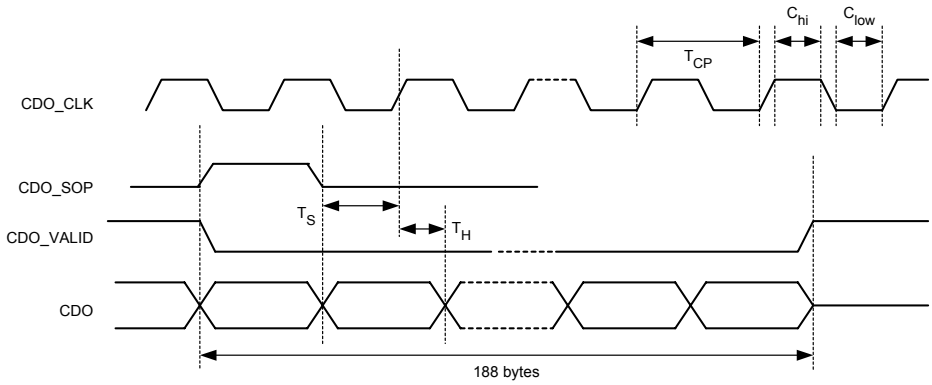


**Figure 47 Video Mux / Compressed Data Output Timing**

*Note:* CDO_VALID is from falling edge of CDO_CLK.

**Table 31 Video Mux / CDO Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{PF}$ | CDO_CLK period | 18.5 | | | ns |
| $T_S$ | Data setup time | 3 | | | ns |
| $T_H$ | Data hold time | 5 | | | ns |

***CDO via Host Interface***

The external host can read compressed data (CDO) from the VW2010 using the host interface protocol as follows:

1. The VW2010 asserts CDO_REQ (indicates the VW2010 is ready to send compressed data).
2. The external host asserts CDO_ACK (the external host is ready to read data on the HIU_DATA bus).
3. The VW2010 asserts DTACK and writes data on HIU_DATA[15:0].
4. The external host deasserts CDO_ACK (terminates the read cycle).
5. The VW2010 de-asserts DTACK.
6. The VW2010 de-asserts CDO_REQ.

*Note:* This signal can be kept active until all data transfer cycles are completed.

7. Repeat 1-6 for each data transfer.

## Host DMA In

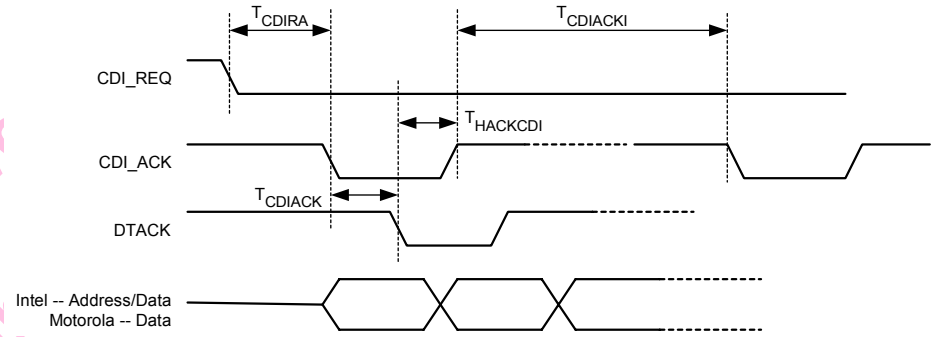


**Figure 48 DMA-In Timing**

1. The VW2010 asserts CDI_REQ (indicates the VW2010 is ready to receive data).
2. The external host asserts CDI_ACK and drives data on HIU_DATA[15:0] (the external host is ready to write data on the HIU_DATA bus).
3. The VW2010 asserts DTACK when it has read the data on HIU_DATA[15:0].
4. The external host deasserts CDI_ACK and at the same time stops driving the

HIU_DATA bus (terminates the write cycle).

5. The VW2010 de-asserts DTACK.
6. The VW2010 de-asserts CDI_REQ.

*Note:* This signal can be kept active until all data transfer cycles are completed.

7. Repeat 1-6 for each data transfer.

**Table 32 DMA-In Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CDIRA}$ | ACK delay from REQ | 10 | | | ns |
| $T_{CDIACKI}$ | Idle time between successive ACK | 70 | | | ns |
| $T_{HACKCDI}$ | ACK hold time | 10 | | | ns |
| $T_{CDIACK}$ | DTACK delay from ACK | | 60 | 120 | ns |

## Host DMA Out

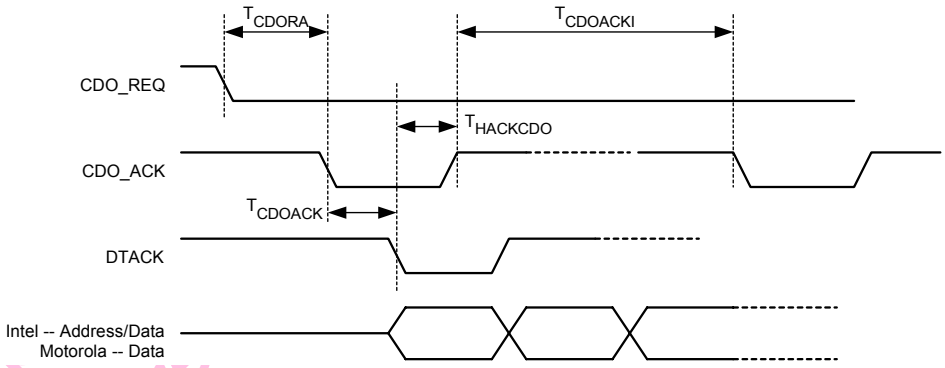


**Figure 49 DMA-Out Timing**

1. The VW2010 asserts CDO_REQ (indicates the VW2010 is ready to send data).
2. The external host asserts CDO_ACK (the external host is ready to read data on the HIU_DATA bus).
3. The VW2010 asserts DTACK and writes data on HIU_DATA[15:0].
4. The external host deasserts CDO_ACK (terminates the read cycle).
5. The VW2010 de-asserts DTACK.
6. The VW2010 de-asserts CDO_REQ.

*Note:* This signal can be kept active until all data transfer cycles are completed.

7. Repeat 1-6 for each data transfer.

**Table 33 DMA-Out Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CDORA}$ | ACK delay from REQ | 10 | | | ns |
| $T_{CDOACKI}$ | Idle time between successive ACK | 70 | | | ns |
| $T_{HACKCDO}$ | ACK hold time | 10 | | | ns |
| $T_{CDOACK}$ | DTACK delay from ACK | | 60 | 120 | ns |

## PCI DMA

PCI DMA In and PCI DMA Out are performed in accordnce with the PCI SPecifications.

## Encoder SDRAM Interface (2M32)

*Note:* In most applications, the same SDRAM is also used for the decoder.

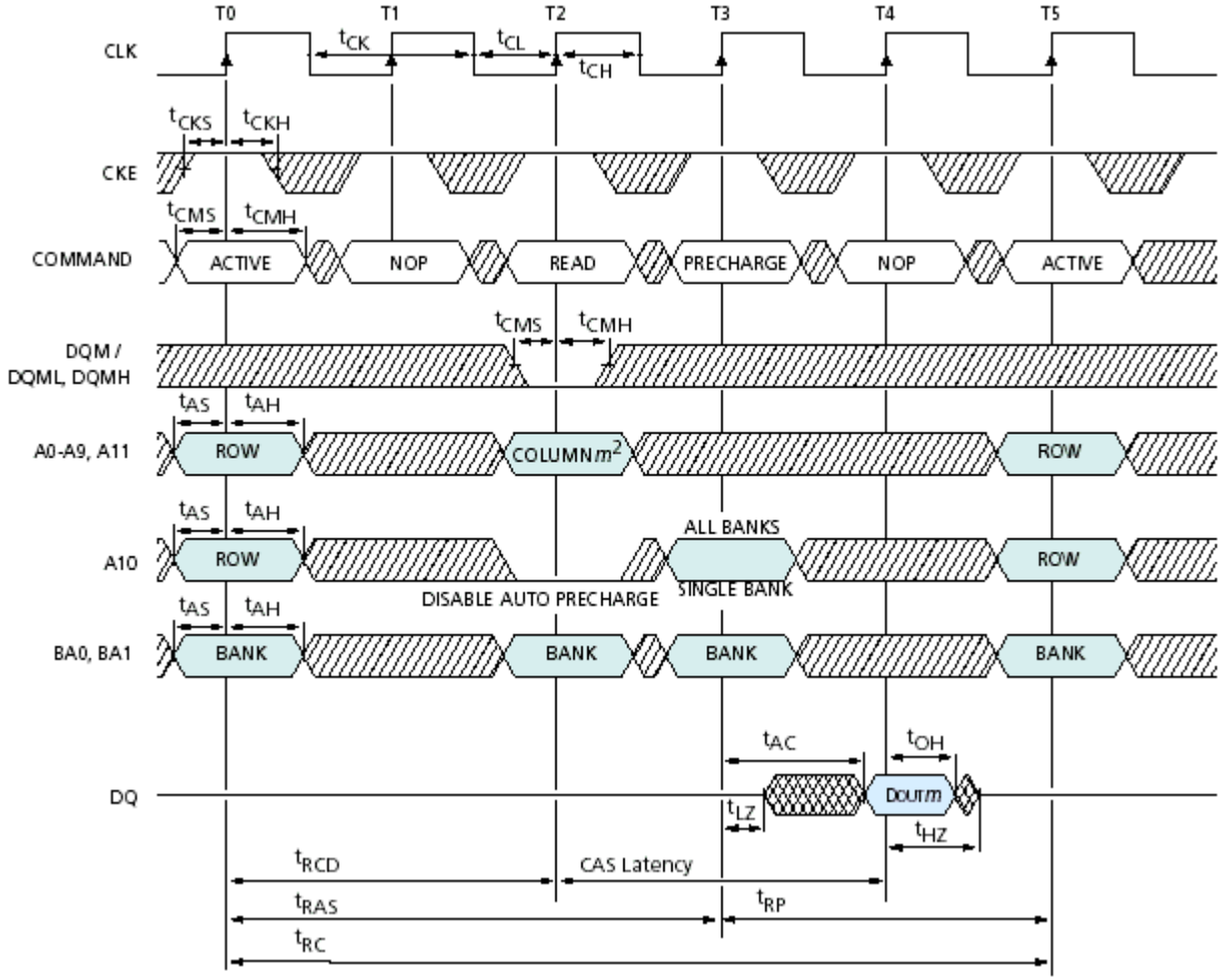


**Figure 50 SDRAM Read Cycle Timing (2M32)**

**Table 34 SDRAM Read Cycle Parameters**

| SYMBOL* | -5 MIN | -5 MAX |
|---|---|---|
| $^tAC(3)$ | | 4.5 |
| $^tAC(2)$ | | |
| $^tAC(1)$ | | |
| $^tAH$ | 1 | |
| $^tAS$ | 1.5 | |
| $^tCH$ | 2 | |
| $^tCL$ | 2 | |
| $^tCK(3)$ | 5 | |
| $^tCK(2)$ | | |
| $^tCK(1)$ | | |
| $^tCKH$ | 1 | |
| $^tCKS$ | 1.5 | |

| SYMBOL* | -5 MIN | -5 MAX |
|---|---|---|
| $^tCMH$ | 1 | |
| $^tCMS$ | 1.5 | |
| $^tHZ(3)$ | 4.5 | |
| $^tHZ(2)$ | | |
| $^tHZ(1)$ | | |
| $^tLZ$ | 1 | |
| $^tOH$ | 1.5 | |
| $^tRAS$ | 38.7 | 120,000 |
| $^tRC$ | 55 | |
| $^tRCD$ | 15 | |
| $^tRP$ | 15 | |

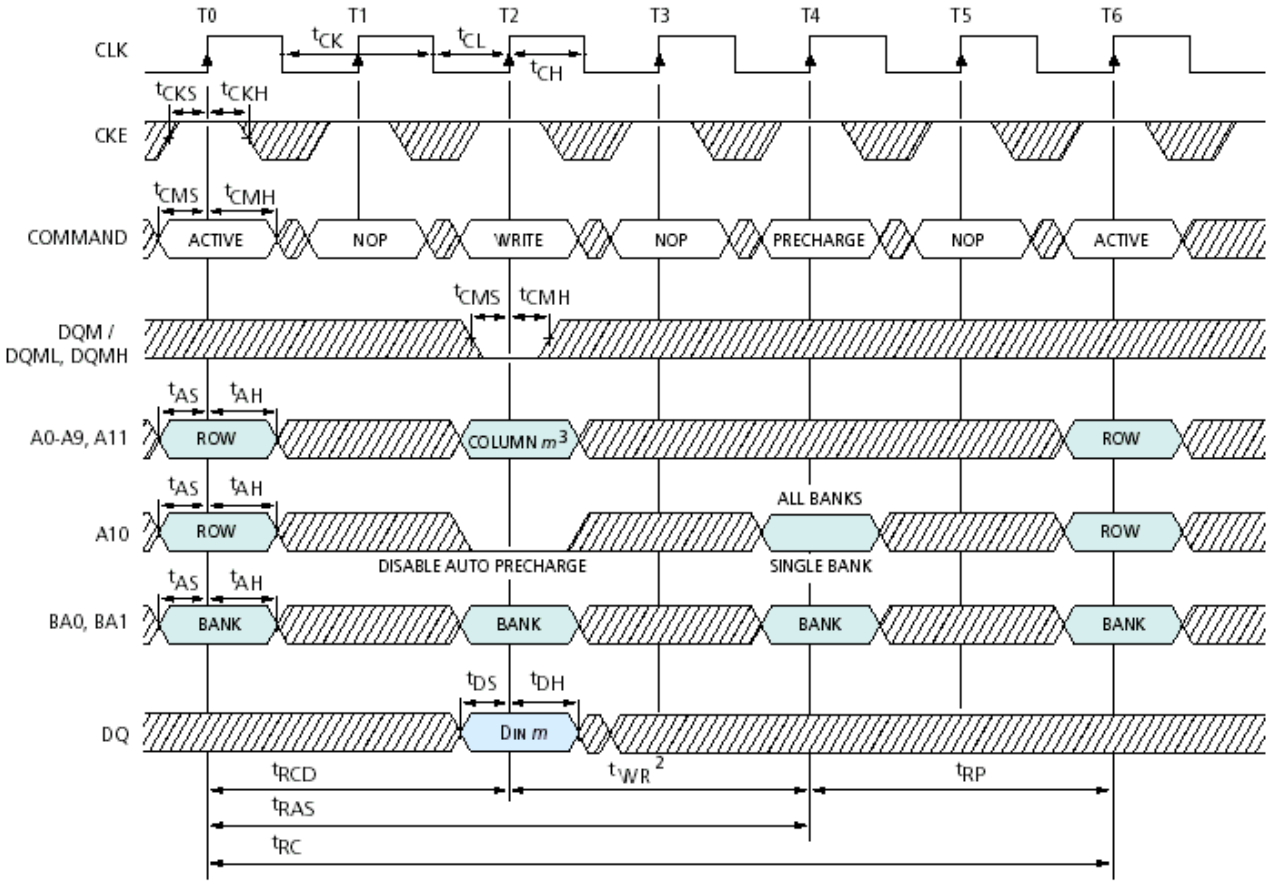


**Figure 51 SDRAM Write Cycle Timing (2M32)**

**Table 35 SDRAM Write Cycle Parameters**

| | -5 | |
|---|---|---|
| SYMBOL* | MIN | MAX |
| $t_{AH}$ | 1 | |
| $t_{AS}$ | 1.5 | |
| $t_{CH}$ | 2 | |
| $t_{CL}$ | 2 | |
| $t_{CK}$ (3) | 5 | |
| $t_{CK}$ (2) | | |
| $t_{CK}$ (1) | | |
| $t_{CKH}$ | 1 | |
| $t_{CKS}$ | 1.5 | |

| SYMBOL* | -5 MIN | -5 MAX |
|---|---|---|
| tCMH | 1 | |
| tCMS | 1.5 | |
| tDH | 1 | |
| tDS | 1.5 | |
| tRAS | 38.7 | 120,000 |
| tRC | 55 | |
| tRCD | 15 | |
| tRP | 15 | |
| tWR | 2 tCK | |

For additional details, see the Micron MT48LC2M32B2 data sheet.

## Decoder SDRAM Interface (1M16)

*Note:* In some applications, a smaller-capacity SDRAM may be sufficient to support the decoder.

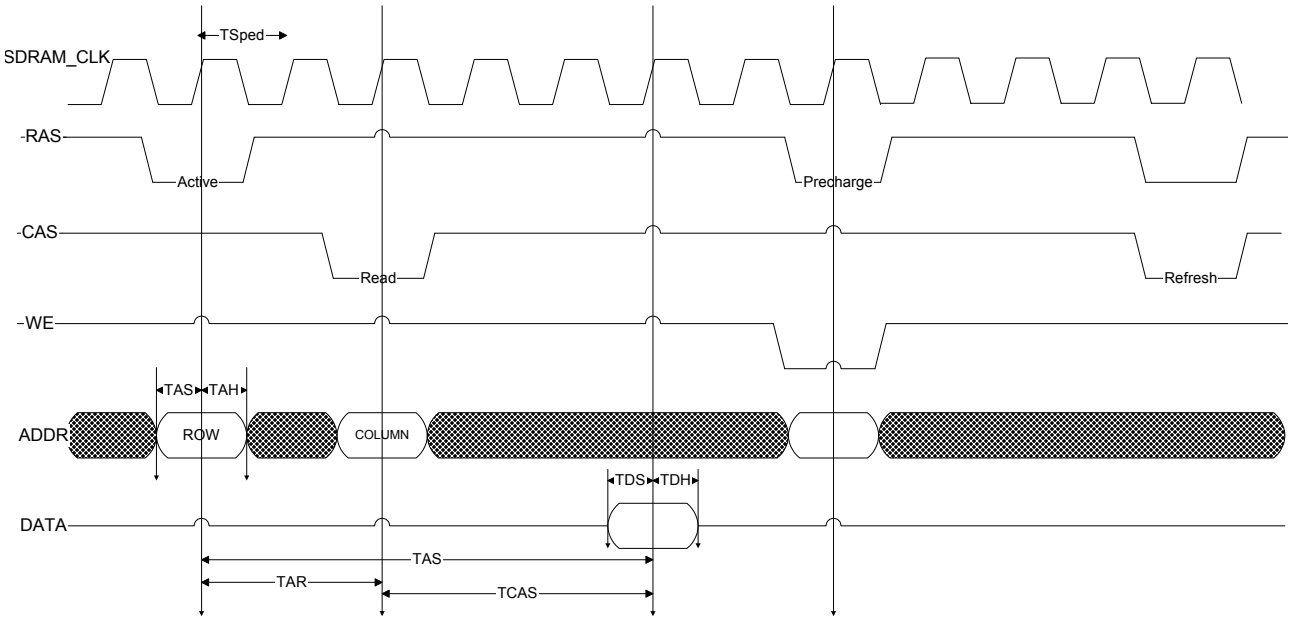


**Figure 52 SDRAM Read Cycle Timing (1M16)**

**Table 36 SDRAM Read Cycle Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AS}$ | Address setup time | 2 | | - | ns |
| $T_{AH}$ | Address hold time | 1.5 | | - | ns |
| $T_{DS}$ | Data setup time | 2 | | - | ns |
| $T_{DH}$ | Data hold time | 2 | | - | ns |
| $T_{CAS}$ | CAS latency (3 cycles) | 3 | | 3 | Clock |
| $T_{AR}$ | Active to read time | 3 | | 3 | Clock |

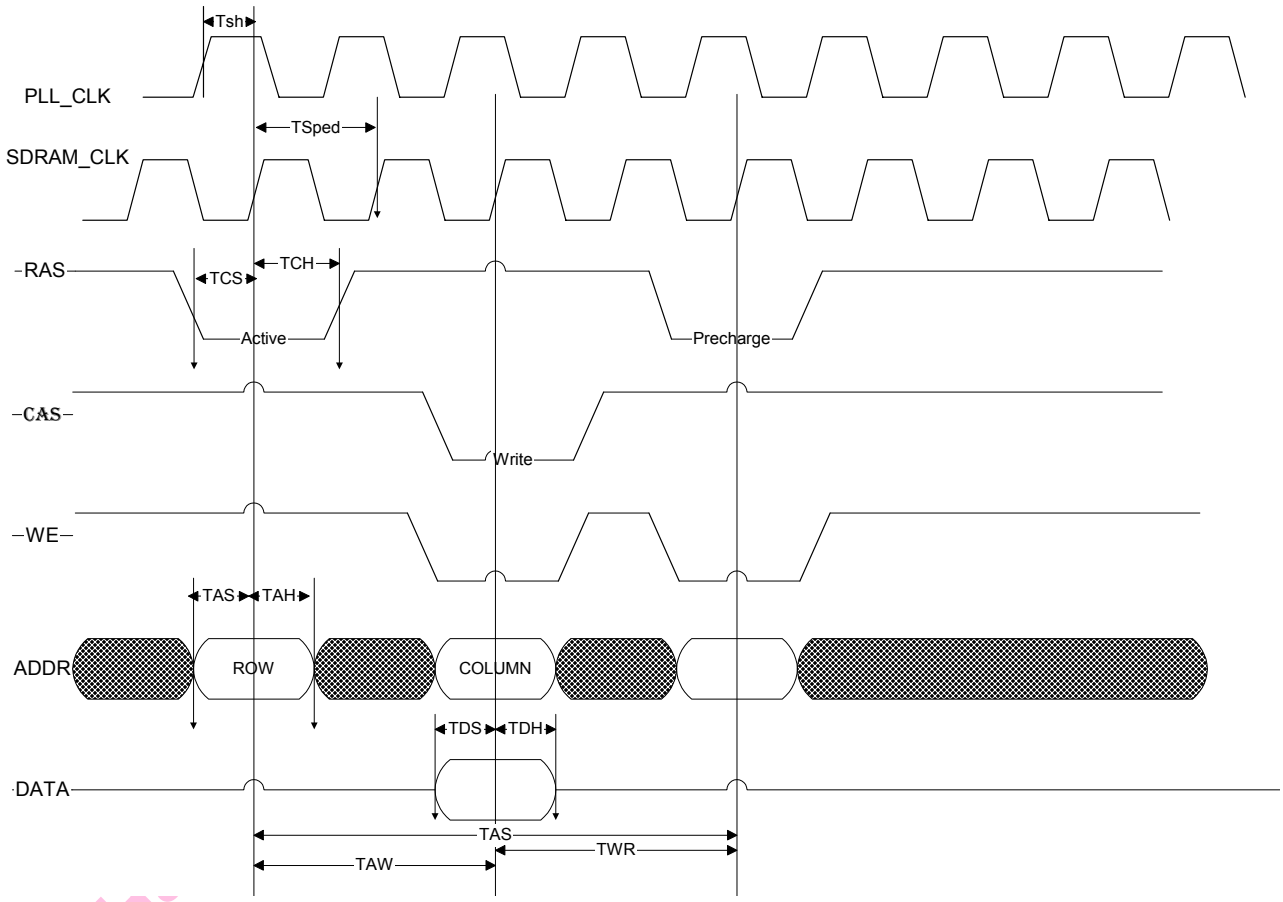


**Figure 53 SDRAM Write Cycle Timing (1M16)**

**Table 37 SDRAM Write Cycle Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{Sped}$ | SDRAM clock cycle time | 9 | | | ns |
| $T_{SH}$ | SDRAM_CLK delay from PLL_CLK | 7 | | | ns |
| $T_{AS}$ | Address setup time | 4 | | | ns |
| $T_{AH}$ | Address hold time | 2 | | | ns |
| $T_{CS}$ | RAS setup time | 4 | | | ns |
| $T_{CH}$ | RAS hold time | 2 | | | ns |
| $T_{DS}$ | Data setup time | 4 | | | ns |
| $T_{DH}$ | Data hold time | 2 | | | ns |
| $T_{AW}$ | Active to write time | 3 | | 3 | Clock |
| $T_{WR}$ | Write to precharge time | 2 | | 2 | Clock |

For additional details, see the Micron MT48LC1M16A1 data sheet.

## ROM Interface

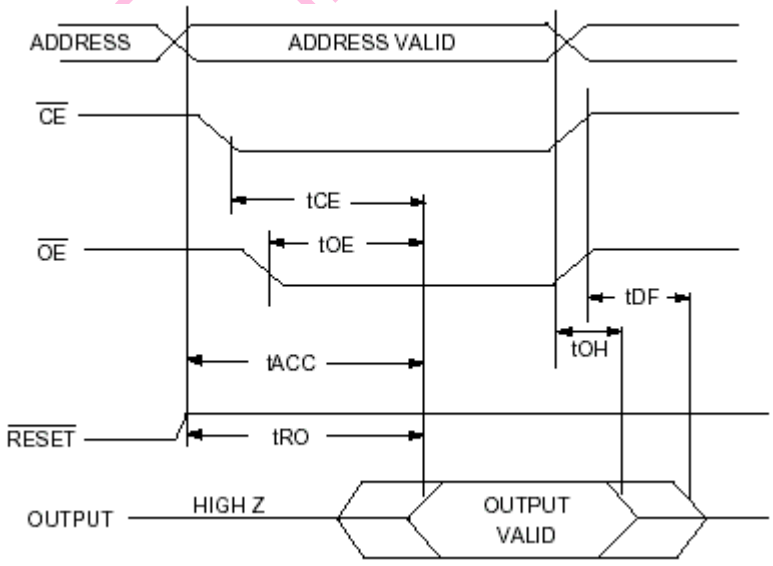


**Figure 54 ROM Interface Read Timing**

**Table 38 ROM Read Timing Parameters**

| Symbol | Parameter | AT49BV16X4(T)-90 | | AT49BV16X4(T)-12 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | 90 | | 120 | ns |
| $t_{CE}$[1] | $\overline{CE}$ to Output Delay | | 90 | | 120 | ns |
| $t_{OE}$[2] | $\overline{OE}$ to Output Delay | 0 | 40 | 0 | 50 | ns |
| $t_{DF}$[3][4] | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 25 | 0 | 30 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first | 0 | | 0 | | ns |
| $t_{RO}$ | $\overline{RESET}$ to Output Delay | | 800 | | 800 | ns |

For additional details, see the Digi Key AT49BV1614 data sheet.

## ICI Interface

Table 39 on page 170 shows the ICI interface timing parameters and Figure 55 shows the data transfers on the ICI bus.

During write operations, data transfers are relative to the SCL output. During read operations, data transfers are relative to the SCL input.

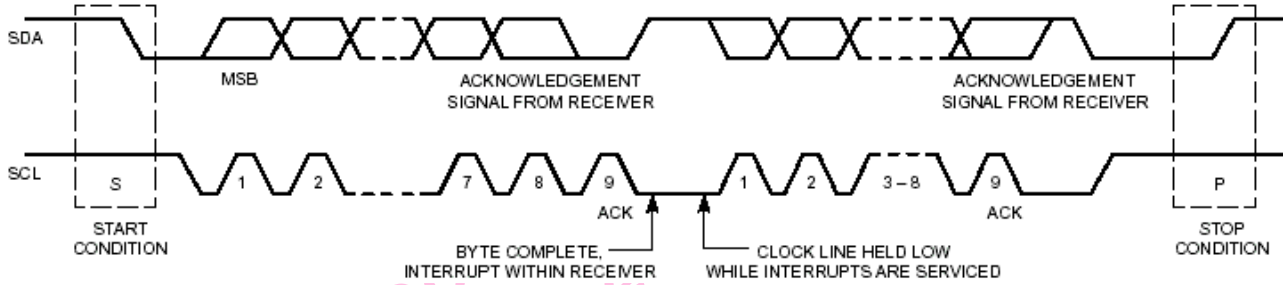


**Figure 55 Data Transfer on the ICI Bus**

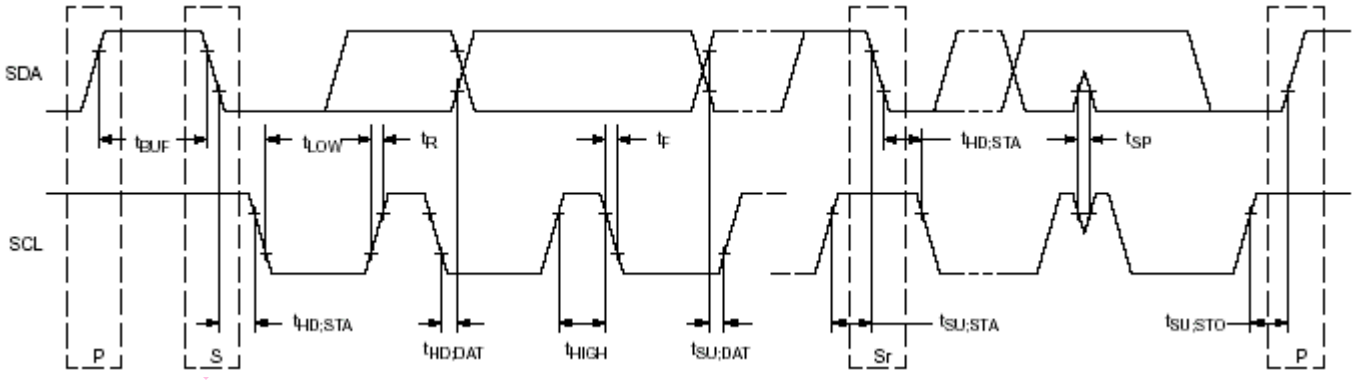


**Figure 56 ICI Timing**

**Table 39 ICI Timing Parameters**

| PARAMETER | SYMBOL | STANDARD-MODE I²C-BUS | | FAST-MODE I²C-BUS | | UNIT |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| SCL clock frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 4.7 | – | 1.3 | – | µs |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | 4.0 | – | 0.6 | – | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | – | 1.3 | – | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4.0 | – | 0.6 | – | µs |
| Set–up time for a repeated START condition | $t_{SU;STA}$ | 4.7 | – | 0.6 | – | µs |
| Data hold time: | $t_{HD;DAT}$ | | | | | |
| for CBUS compatible masters (see NOTE, Section 9.1.3) | | 5.0 | – | – | – | µs |
| for I²C–bus devices | | 0[1] | – | 0[1] | 0.9[2] | µs |
| Data set–up time | $t_{SU;DAT}$ | 250 | – | 100[3] | – | ns |
| Rise time of both SDA and SCL signals | $t_r$ | – | 1000 | $20 + 0.1C_b$[4] | 300 | ns |
| Fall time of both SDA and SCL signals | $t_f$ | – | 300 | $20 + 0.1C_b$[4] | 300 | ns |
| Set–up time for STOP condition | $t_{SU;STO}$ | 4.0 | – | 0.6 | – | µs |
| Capacitive load for each bus line | $C_b$ | – | 400 | – | 400 | pF |

All values referred to $V_{IHmin}$ and $V_{ILmax}$ levels (see Table 3).

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal.
3. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.
4. $C_b$ = total capacitance of one bus line in pF.

For additional details, see the Philips Semiconductor I²C specification.

## PLL Interface

For details, see the ICS511 and the MK2745-21data sheets from Integrated Circuit Systems.

## JTAG / EJTAG Interface

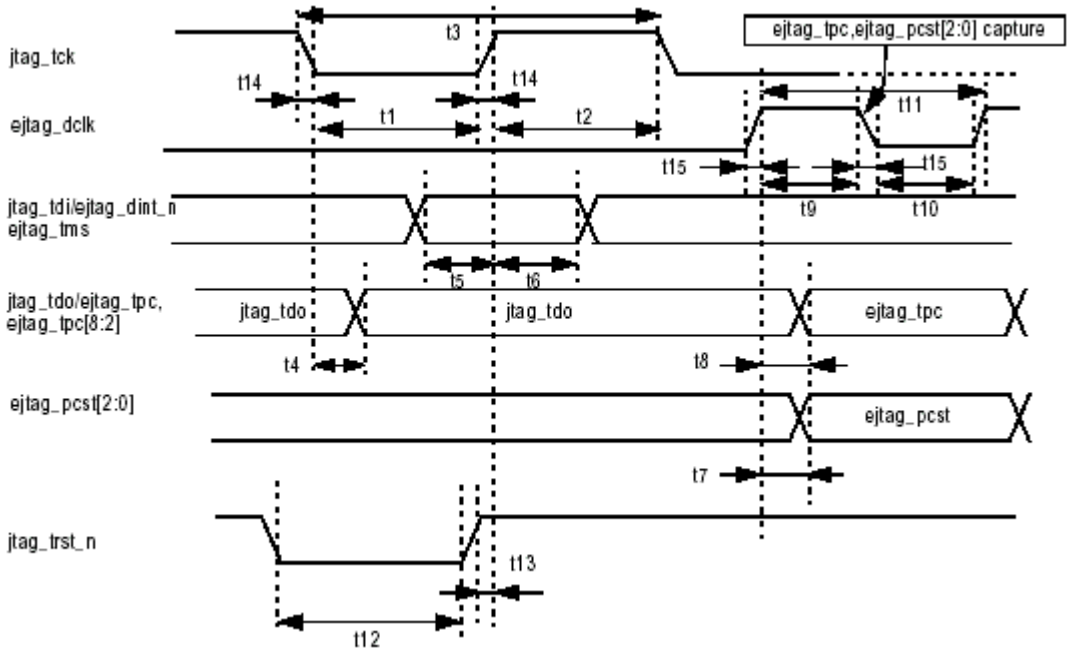


**Figure 57 JTAG / EJTAG Timing**

t1 = $t_{TCKlow}$
t2 = $t_{TCKHIGH}$
t3 = $t_{TCK}$
t4 = $t_{TDODO}$
t5 = $t_{TDIS}$
t6 = $t_{TDIH}$
t7 = $t_{PCSTDO}$
t8 = $t_{TPCDO}$
t9 = $t_{DCKHIGH}$
t10 = $t_{DCKLOW}$
t11 = $t_{DCK}$
t12 = $t_{TRSTDO}$
t13 = $t_{TRSTR}$
t14 = $t_{TCK\ RISE,\ ITCK\ FALL}$
t15 = $t_{DCK\ RISE,\ tDCK\ FALL}$

**Table 40 JTAG / EJTAG Timing Parameters**

to be added

For additional details, see the JTAG standard IEEE 1149-1 and an EJTAG data sheet from EPI, for example.

# Index

## Numerics



## A



## B



## C

## D



## E

## O



## P



## R



## S



## T

## U



## V