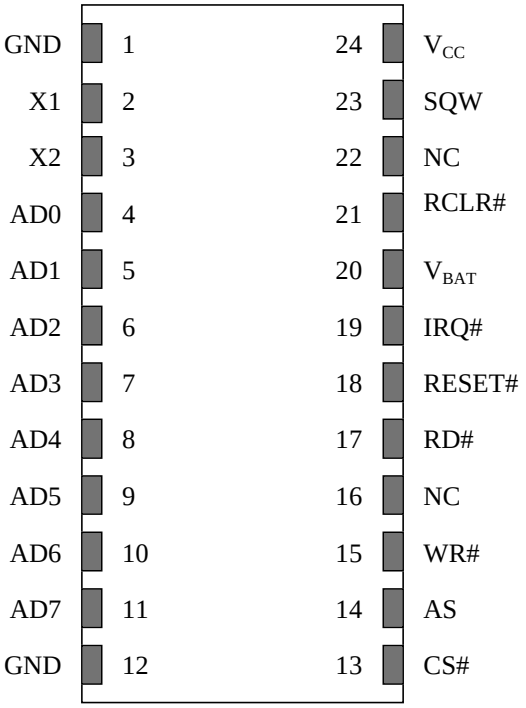
FEATURES

- Drop-in replacement for IBM AT computer clock/calendar.
- Pin configuration closely matches the DS12887, DS12885and DS12885Q
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ#)
- Three interrpts are separately software-maskable and testable
  - Times-of-day alarm once/second to once/day
  - Periodic rates from 122 μs to 500 ms
  - End of clock update cycle
- Optional 28-pin PLCC surface mount package

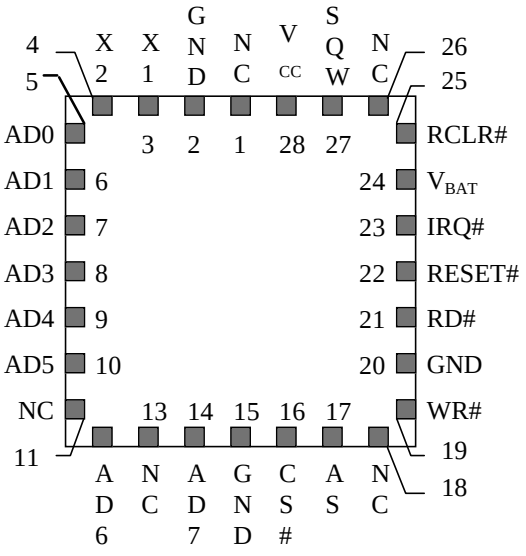
DESCRIPTION

The VT82885 Real Time Clock is designed to be a direct replacement for the DS12885. The VT82885 is identical in form, fit and function to the DS12885. It has 114 bytes of general purpose RAM. Access to this RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. A complete description of operating conditions, electrical characteristics, bus timing and pin descriptions follows.

PIN ASSIGNMENT



VT82885 24 PIN DIP



VT82885 28-PIN PLCC

PIN DESCRIPTION

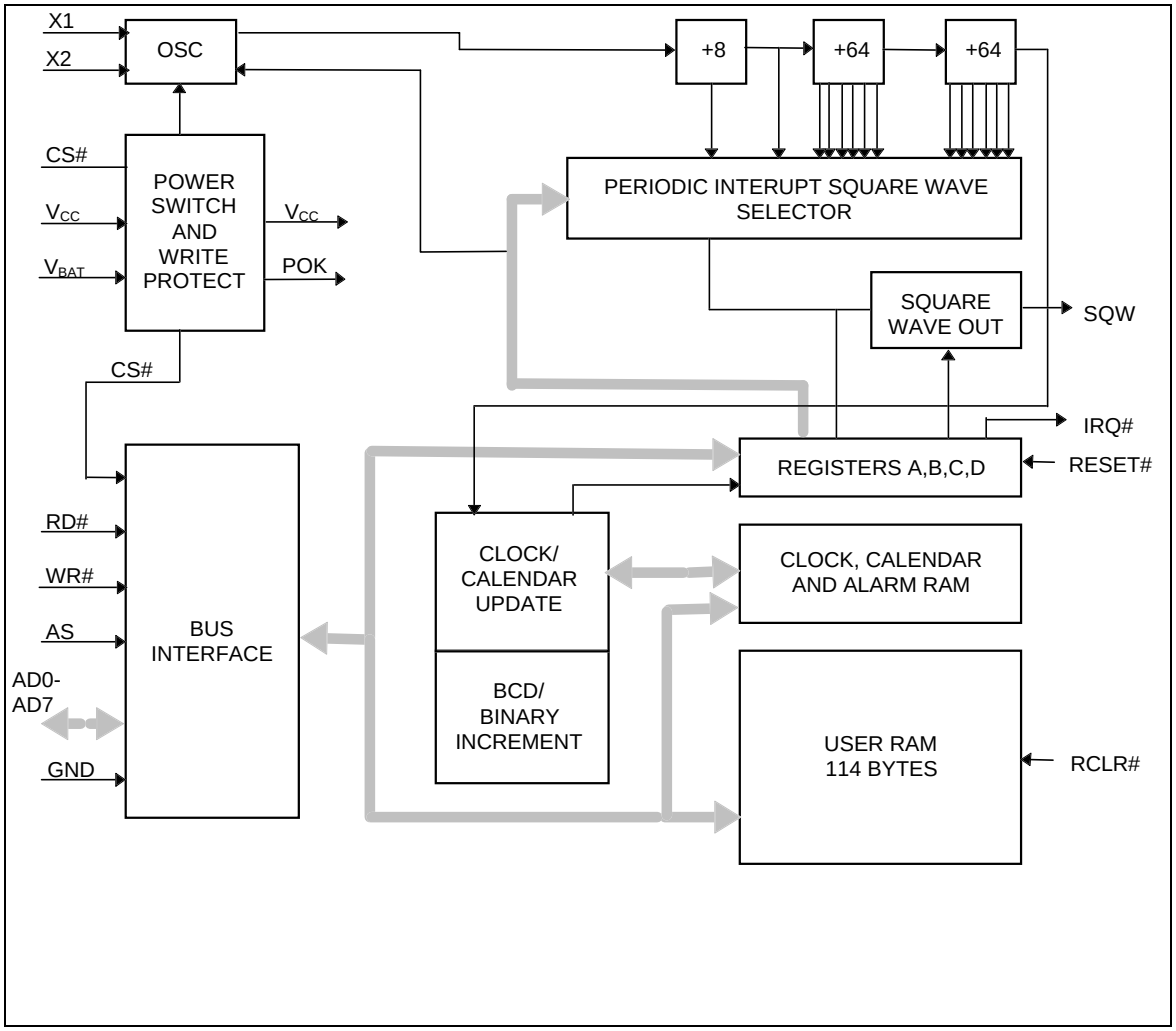
AD0-AD7	- Multiplexed Address/Data Bus
NC	- No Connection
CS#	- Chip Select
AS	- Address Strobe

WR#	- Write Strobe
RD#	- Read Strobe
RESET#	- Reset Input
IRQ#	- Interrupt Request Output
SQW	- Square Wave Output
V_{CC}	- +5 Volt Supply
GND	- Ground
X1, X2	- 32.768 kHz Crystal Connections
V_{BAT}#	- +3 Volt Battery Input
RCLR#	- RAM Clear

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the VT82885. The following paragraphs describe the function of each pin.

FIQURE 1: BLOCK DIAGRAM VT82885



POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the VT82885 and reaches a level of greater than 4.25 volts, the device becomes ac-cessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after

power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inac-tive level regardless of the value of CS# at the input pin. The VT82885 is, therefore, write-protected. When V_{CC} falls below the level of V_{BAT}, the external V_{CC} supply is switched off and the external V_{BAT} lithium energy source supplies power to the Real Time Clock and the RAM memory.

SIGNAL DESCRIPTIONS

V_{CC} – DC power is provided to the device on thIs pin. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When VCC is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function contin-ues unaffected by the lower input voltage. As VCC falls below V_{BAT}, the RAM and timekeeper are switched over to the exter-nal lithium energy source. The timekeeping function maintains an accuracy of ± 1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

V_{BAT} – Battery input for any standard 3 volt lithium cell or energy source. Battery vol-tage must be held between 2.5 and 3.4 volts for proper operation. A maximum load of .5 µA at 25°C in the absence of V_{CC} power should be used to size the external energy source.

SQW (Square Wave Output) – The SQW pin can output a signal from one of 13 taps provided by the internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

TABLE 1: PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

X1, X2 – These pins connect to a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Each of the pins (X1 and X2) require the installation of an external 10 pF capacitor.

RCLR# – The RCLR# pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR# must be forced to an input logic of 0 (-0.3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The RCLR# function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) – Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and cycle paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the VT82885 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS, at which time the VT82885 latches the address from AD0 to AD6. Valid data must be present and held stable during the latter portion of the RD# or WR# pulses. In a read cycle the VT82885 outputs 8 bits of data during the latter portion of the RD# or RD# pulses. The read cycle is terminated and the bus returns to a high impedence state as RD# transistions high as in Intel timing.

AS (Adress Strobe Input) – A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS causes the address to be latched within the VT82885.

RD# (Read Strobe) – The RD# pin identifies the time period when the VT82885 drives the bus with read data. The RD# signal is the same definition as the Output Enable (OE#) signal on a typical memory.

WR# (Write Strobe) – The WR# pin is used to indicate a write cycle.

CS# (Chip Select Input) – The Chip Select signal must be asserted low for a bus cycle in the VT82885 to be accessed. CS# must be kept in the active state during RD# and WR#. Bus cycles which take place without asserting CS# will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the VT82885 internally inhibits access cycles by internally disabling the CS# input. This action protects both the real time clock data and RAM data during power outages.

IRQ# (Interrupt Request Output) – The IRQ# pin is an active low output of the VT82885 that can be used as an interrupt input to a processor. The IRQ# output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ# pin the processor program normally reads the C register. The RESET# pin also clears pending interrupts.

When no interrupt condition is present, the IRQ# level is in the high impedence state. Multiple interrupting devices can be connected to an IRQ# bus. The IRQ# bus is an open drain output and requires an external pull-up resistor.

RESET# (Reset Input) – The RESET# pin has no effect on the clock, calendar, or RAM. On power-up the RESET# pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that RESET# is held low is dependent on the application. However, if RESET# is used on power-up, the time RESET# is low should exceed 200 ms to make sure that the internal timer that controls the VT82885 on power-up has timed out. When RESET# is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.

B. Alarm Interrupt Flag (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until RESET# is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. IRQ# pin is in the high impedence state.

I. Square Wave Output Enable (SQWE) bit is cleared to zero.

J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application RESET# can be connected to V_{CC}. This connection will allow the VT82885 to go in and out of power fail without affecting any of the control registers.

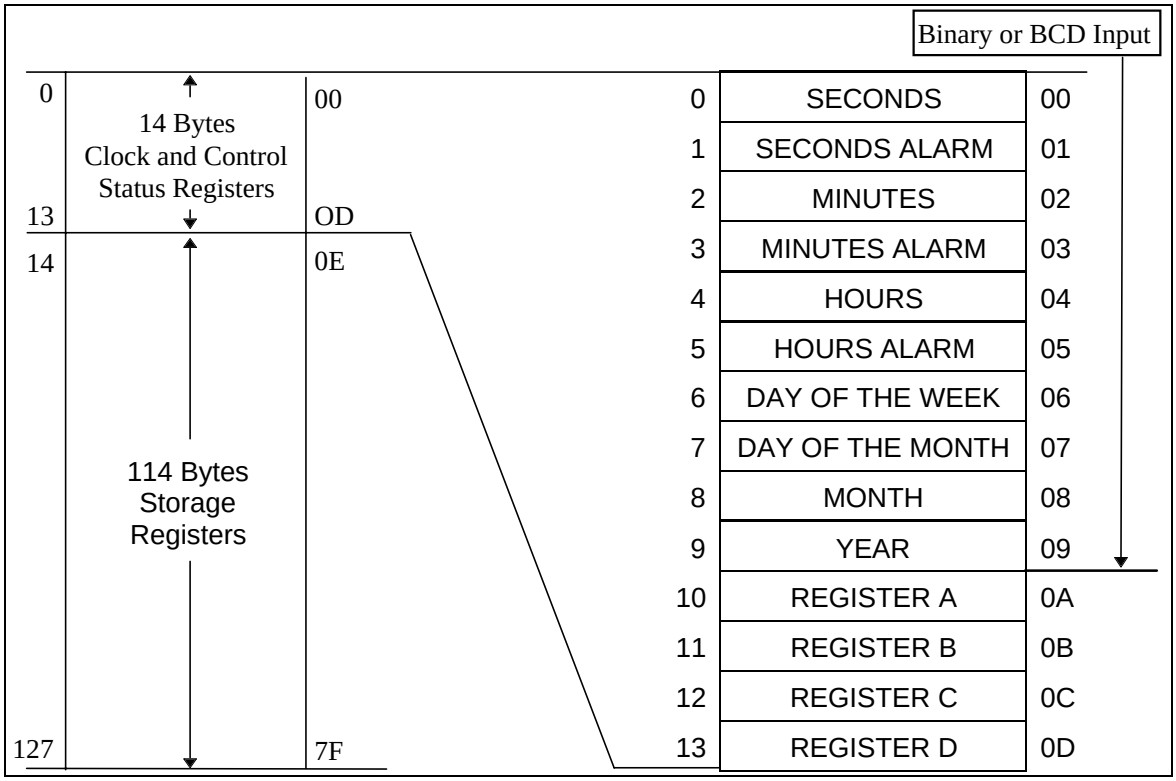
ADDRESS MAP

The address map of the VT82885 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar and alarm data, and four bytes which are used for control and status. All 128 bytes can be directly written or read except the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A, B, C and D) are described in the “Register” section.

FIGURE 2: ADDRESS MAP VT82885



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar and alarm registers, the SET bit in Register B

should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode can-not be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour loca-tions. When the 12-hour format is selected, the high order bit of the hours byte repre-sents PM when it is a logic one. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data oc-curs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading in-correct time and calendar data is low. Sev-eral methods of avoiding any possible incor-rect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a “don’t care” state in one or more of the three alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm will be generated each hour when the “don’t care” bits are set in the hours byte. Similarily, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three alarm bytes create an interrupt every second.

TABLE 2: TIME. CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1.12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

NONVOLATILE RAM

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the VT82885. They can be used by the processor program as nonvolatile memory and are fully available during the update cycles.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The peridoic interrupt can be selected for rates from 500 ms to 122 μs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initi-ated when the event occurs. A zero in an interrupt-enable bit prohibits the IRQ# pin from being asserted from the interrupt condition. If an interrupt flag is already set when the interrupt is enabled, IRQ# is im-mediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first ena-bling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When the flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read.; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the IRQ# pin is asserted low. IRQ# is asserted as long as at least one of three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the IRQ# pin is being driven low. Determination that the RTC initiated an interrupt is accom-plished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the VT82885. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

The VT82885's internal oscillator can be turned on and off as required. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The PS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE)

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ# pin to go to an active state from once every 500 ms to once every 122 μs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is se-

lected using the same Register A bits which selected the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

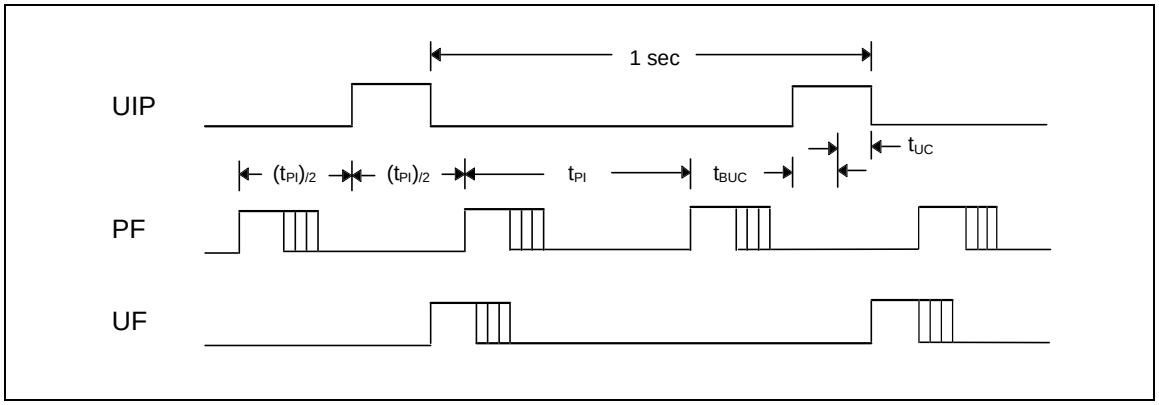
The VT82885 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar and alarm buf-fers and also guarantees that time and cal-endar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µsbefore the time/calendar data will be changed. There-fore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{P1/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

FIGURE 3: UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



REGISTERS

The VT82885 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one, the update transfer will soon oc-cur. When UIP is a zero, the update transfer will not occur for at least 244 μs. The time, calendar and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RESET#. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2 RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate;
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS# bits. These four read/write bits are not affected by RESET#.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit that is not modified by RESET# or internal functions of the VT82885.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the IRQ# pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ# pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the IRQ# output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal VT82885 functions, but is cleared to zero on RESET#.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to one, permits the Alarm Flag (AF) bit in Register C to assert IRQ#. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a “don’t care” alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not iniate the IRQ# signal. The RE-SET# pin clears AIE to zero. The internal functions of the VT82885 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert IRQ#. The RESET# pin going low or the SET bit going high clears to UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared

by the RESET# pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET#. A one in DM signifies binary data while a zero in DM specifies Bnary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of RESET#.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET#.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is one, the IRQ# pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET# pin is low.

ABSOLUTE MAXIMUM RATINGS*

PF

The Periodic Interrupt Flag (PF) is a read-only bit whcih is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the IRQ# signal is active and will set the IRQF bit. The PF bit is cleared by a RESET# or a software read of Register C.

AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ# pin will go low and a one will appear in the IRQF pin. UF is cleared by reading Register C or a RESET#.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ# pin. UF is cleared by reading Register C or a RESET#.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

This bit is not writeable and should always be one when read. If a zero is ever present, an exhausted external lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by RESET#.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

VOLTAGE ON ANY PIN RELATIVE TO GROUND -0.3V TO +7.0V
OPERATING TEMPERATURE 0°C TO 70°C
STORAGE TEMPERATURE -40°C TO +70°C
SOLDERING TEMPERATURE 260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		5	10	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5V TO 5.5V)

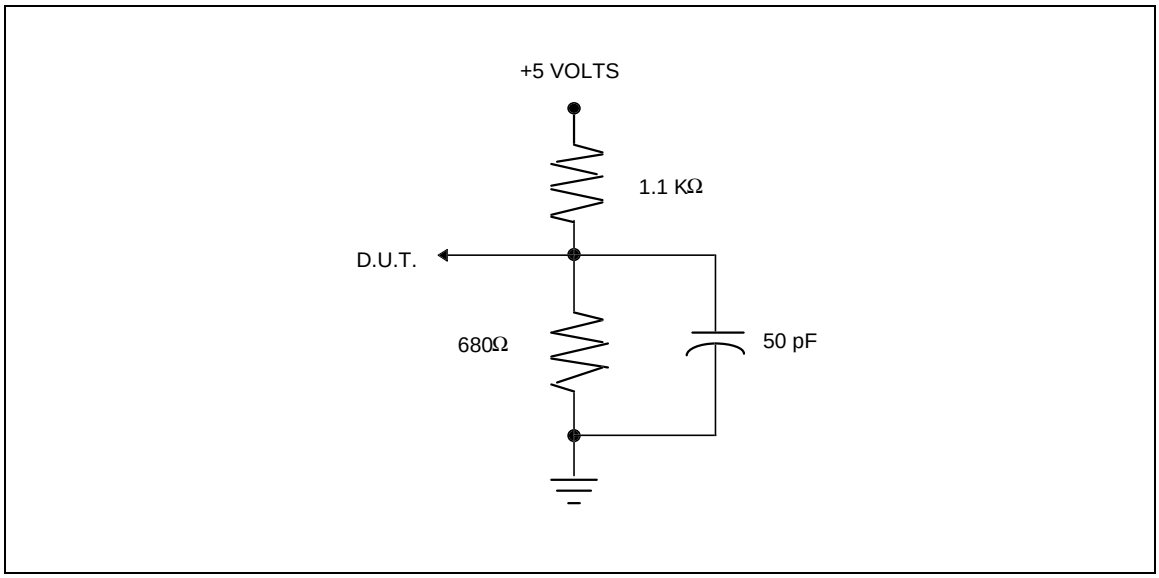
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/WR# High	PW_{EL}	150			ns	

Pulse Width, DS/E High or RD/WR# Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/W# Hold Time	t_{RWH}	10			ns	
R/W# Setup Time before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time before DS, WR#, or RD#	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0				
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/alE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time from DS/E or RD#	t_{DDR}	20		120	ns	
DataSetup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
IRQ# Release from DS	t_{IRDS}			2	µs	
IRQ# Release from RESET#	t_{IRR}			2	µs	
Delay Time before Update Cycle	t_{BUC}		244		µs	
Periodic Interrupt Time Interval	t_{PI}					See Table 1
Time of Update Cycle	t_{UC}		1708		µs	

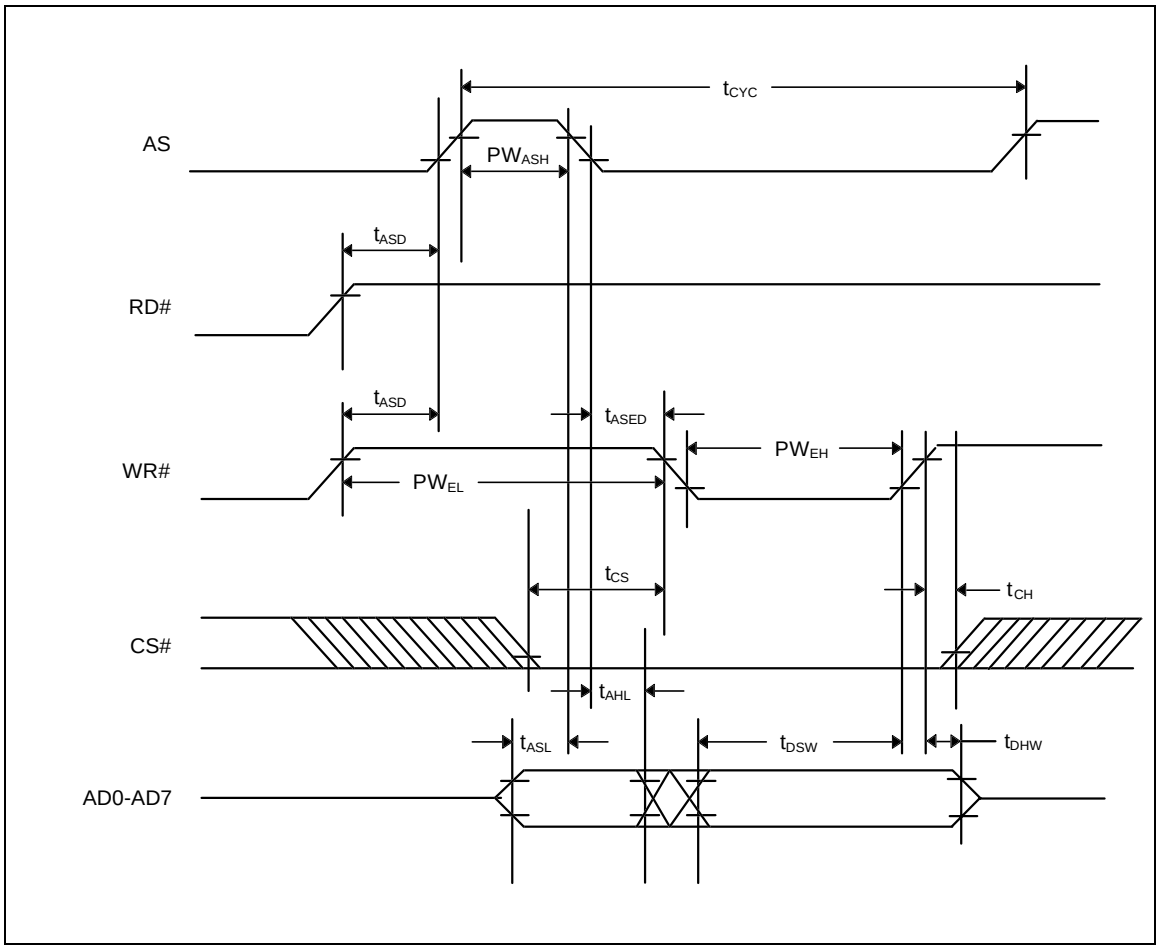
NOTES

1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, the IRQ# pin and the SQW pin when each is in the high impedence state.
4. The IRQ# pin is open drain.
5. Measured with a load as shown in Figure 4.

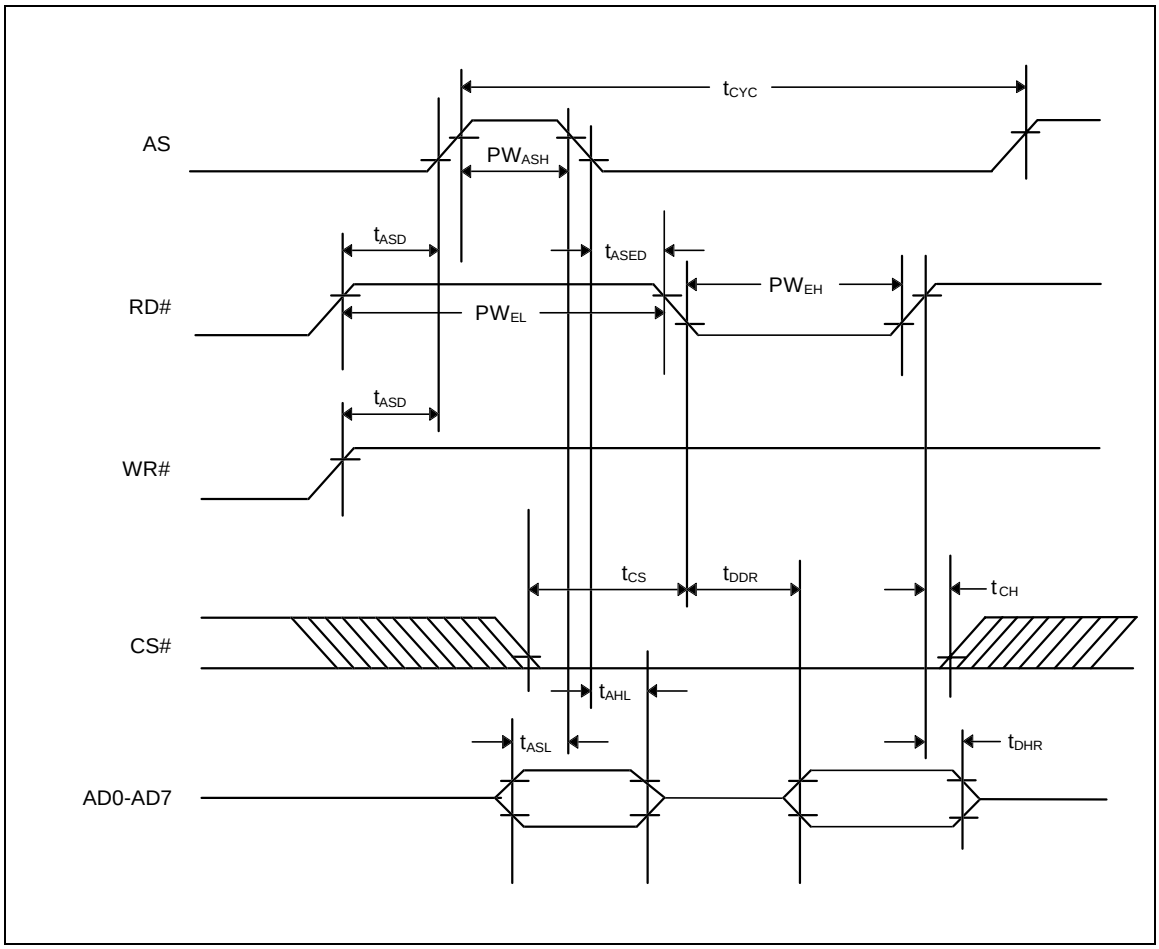
FIGURE 4: OUTPUT LOAD



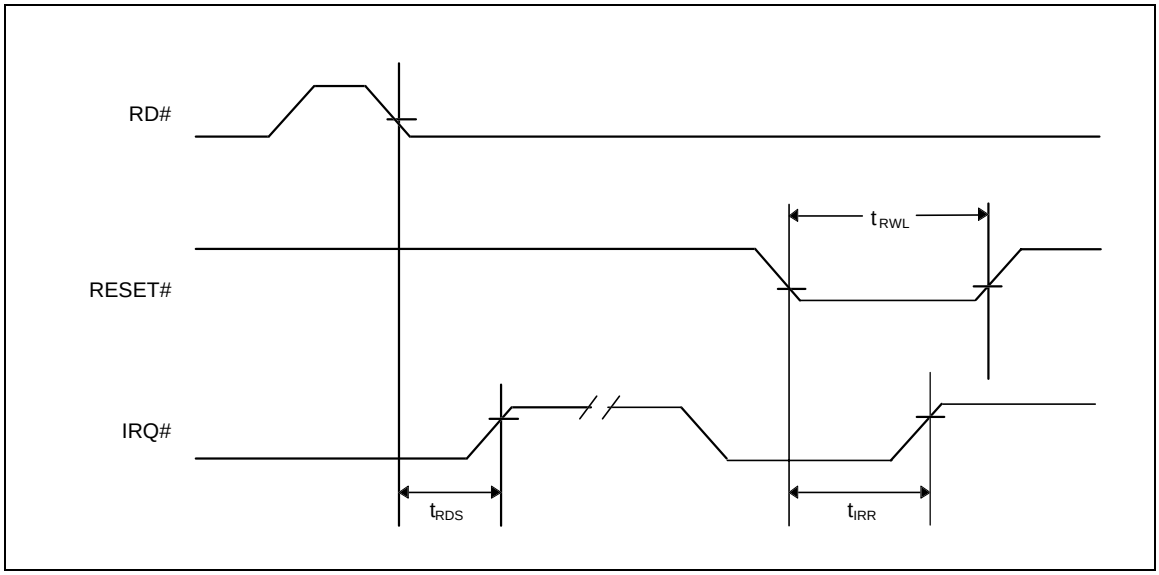
VT82885 BUS TIMING FOR WRITE CYCLE



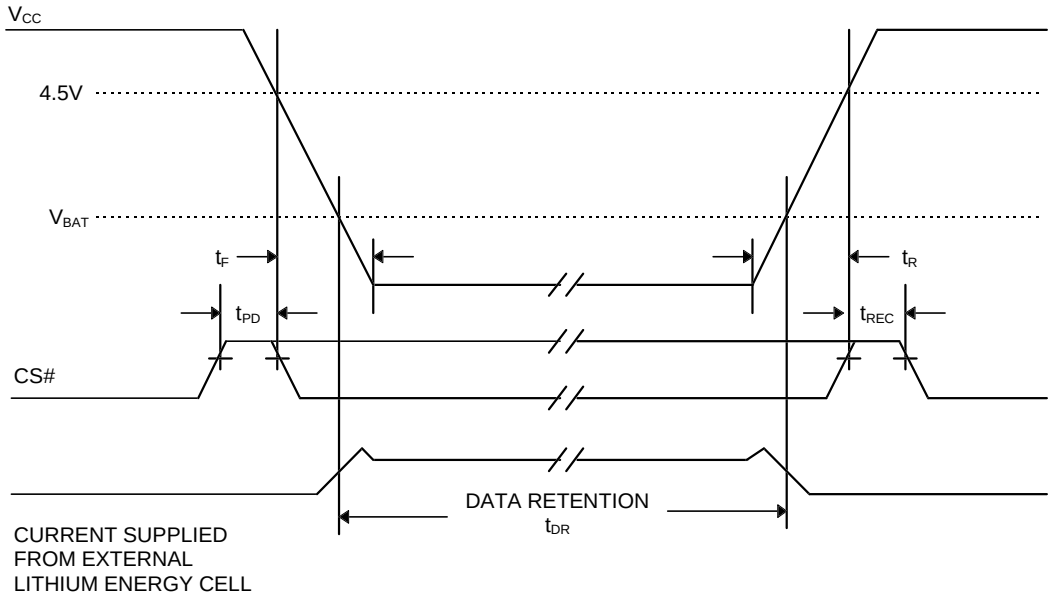
VT82885 BUS TIMING FOR READ CYCLE



VT82885 IRQ RELEASE DELAY TIMING



POWER DOWN/POWER UP TIMING



POWER DOWN/POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CS# at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V (CS# at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V (CS# at V_{IH})	t_R	100			µs	
CS# at V_{IH} after Power-Up	t_{REC}	20		200	ms	

(tA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTE

The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

WARNING

Under no circumstances are negative undershots, of any amplitude, allowed when device is in battery backup mode.