

## 16Mb SDRAM

- 3.3 volt 1Mx16
- 100/143 MHz SDRAM
- 2 banks, 4K refresh

## GENERAL DESCRIPTION

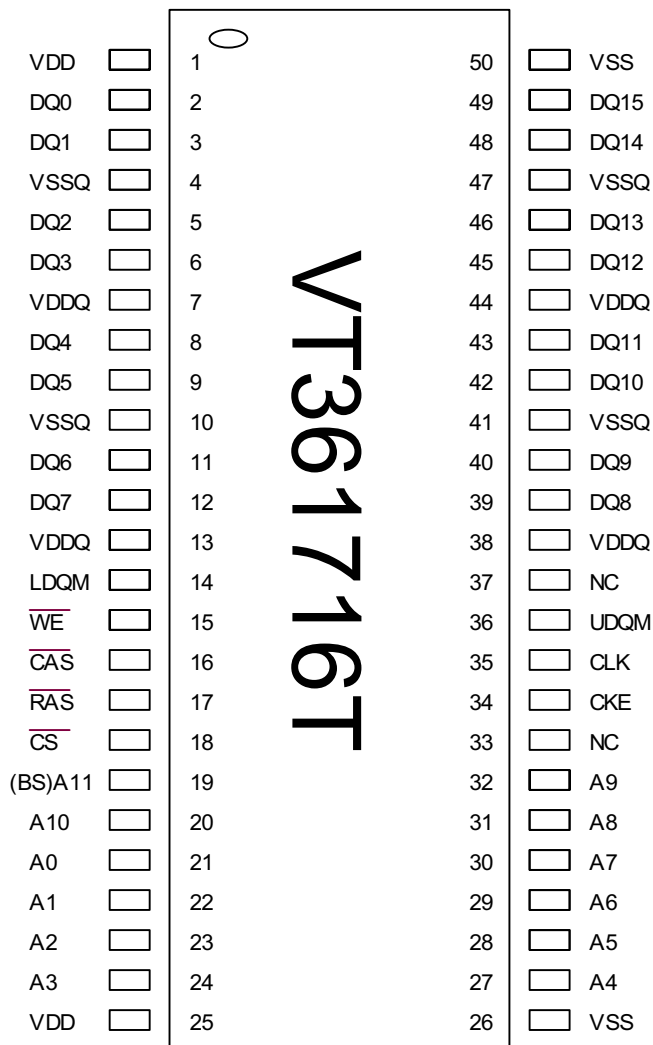
The VT361716T is a high-speed synchronous dynamic random access memory (SDRAM), organized as 512K words x 2 banks x 16 bits. Using pipelined architecture technology. Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1,2,4,8 or full page when a bank and row is selected by an ACTIVE command. By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance.

## FEATURES

- 3.3V  $\pm$  0.3V power supply
- 524,288 words x 2 banks x 16 bits organization
- Two banks operation
- Power-down Mode
- Sequential and interleave burst
- Burst Length: 1,2,4,8 and full page
- CAS latency: 2 and 3
- 4K refresh cycles/64 ms
- Auto & self refresh
- DQM for masking
- Burst read single-bit write operation
- LVTTL compatible with multiplexed address
- All inputs are sample at the positive going edge of the system clock

## PIN CONFIGURATION (Top view)

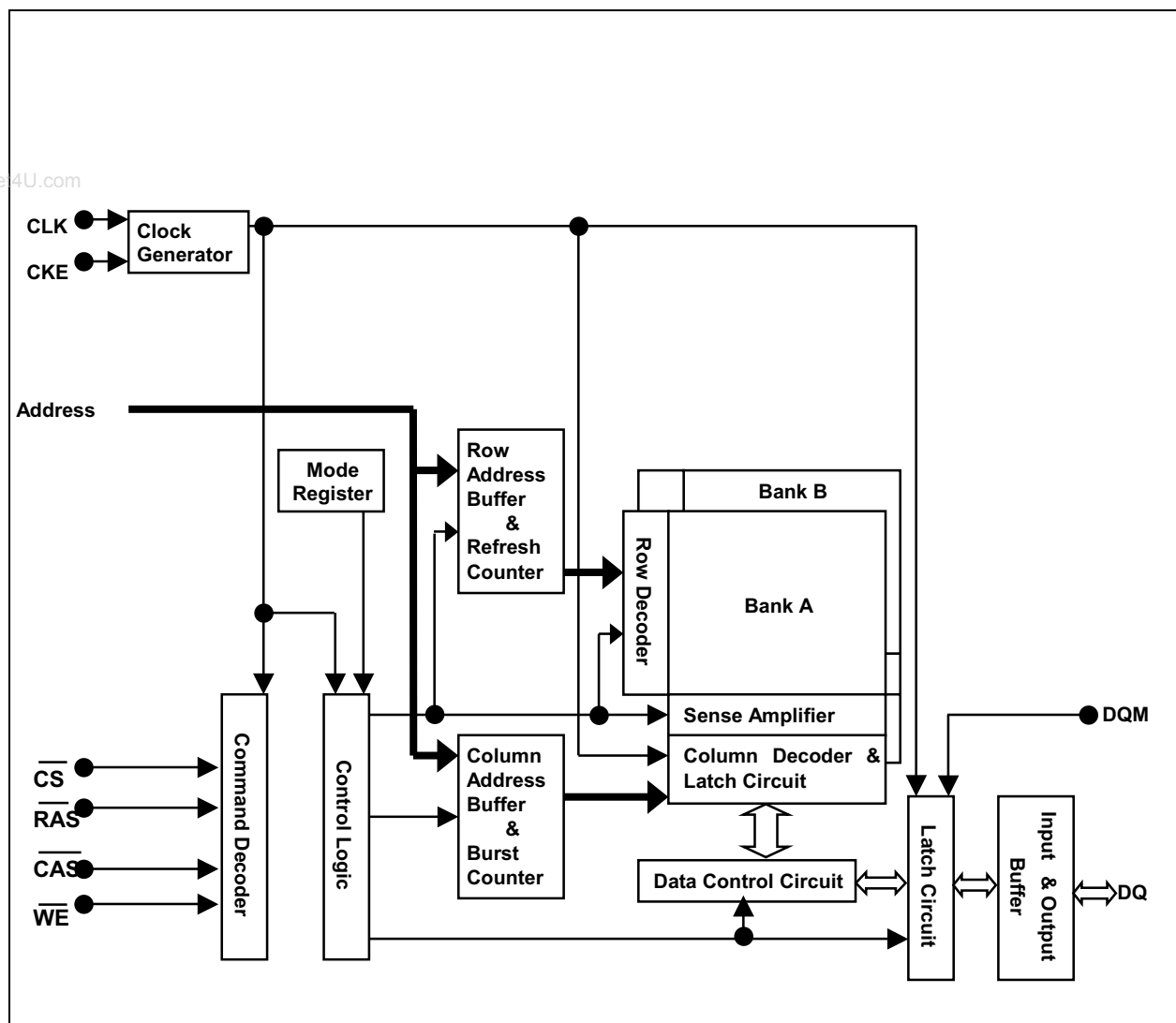
## 50-Pin Plastic TSOP ( II ) ( 400mil )



## PIN DESCRIPTION

| PIN NAME                           | FUNCTION                     | DESCRIPTION                                                                                                                                  |
|------------------------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| A <sub>0</sub> - A <sub>10</sub>   | Address                      | Multiplexed pins for row and column address. Row address: A <sub>0</sub> -A <sub>10</sub> . Column address: A <sub>0</sub> -A <sub>7</sub> . |
| A <sub>11</sub> (BS)               | Bank Select                  | Select bank to activate during row address latch time, or bank to read/write during address latch time.                                      |
| DQ <sub>0</sub> - DQ <sub>15</sub> | Data Input / Output          | Multiplexed pins for data output and input.                                                                                                  |
| /CS                                | Chip Select                  | Disable or enable the command decoder.                                                                                                       |
| /RAS                               | Row Address Strobe           | Latches row addresses on the positive going edge of the CLK with /RAS low.                                                                   |
| /CAS                               | Column Address Strobe        | Latches column addresses on the positive going edge of the CLK with /CAS low.                                                                |
| /WE                                | Write Enable                 | Enables write operation and row precharge.                                                                                                   |
| DQM                                | Input/output mask            | Makes data output Hi-z. Blocks data input when DQM active.                                                                                   |
| CLK                                | Clock Inputs                 | System clock used to sample inputs on the rising edge of clock.                                                                              |
| CKE                                | Clock Enable                 | CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode or Self Refresh mode is entered.          |
| V <sub>DD</sub>                    | Power (+3.3V)                | Power for input buffers and logic circuit inside DRAM.                                                                                       |
| V <sub>SS</sub>                    | Ground                       | Ground for input buffers and logic circuit inside DRAM.                                                                                      |
| V <sub>DDQ</sub>                   | Power (+3.3V) for I/O buffer | Separated power from V <sub>DD</sub> , to improve DQ noise immunity.                                                                         |
| V <sub>SSQ</sub>                   | Ground for I/O buffer        | Separated power from V <sub>SS</sub> , to improve DQ noise immunity.                                                                         |
| NC                                 | No Connection                | No Connection                                                                                                                                |

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER                               | SYMBOL            | VALUE        | UNIT |
|-----------------------------------------|-------------------|--------------|------|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}, V_{OUT}$ | -0.3 to +3.6 | V    |
| Supply voltage relative to $V_{SS}$     | $V_{DD}, V_{DDQ}$ | -0.3 to +3.6 | V    |
| Short circuit current                   | $I_{OS}$          | 50           | mA   |
| Power dissipation                       | PD                | 1.0          | W    |
| Operating temperature                   | $T_{OPT}$         | 0 to +60     | °C   |
| Storage temperature                     | $T_{STG}$         | -55 to +125  | °C   |

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**DC OPERATING CONDITIONS AND CHARACTERISTICS**Recommended DC operating conditions (Voltage referenced to  $V_{SS} = 0V$ ,  $T_A = 0$  to  $70^{\circ}C$ )

| PARAMETER          | SYMBOL   | MIN  | TYP | MAX          | UNIT | NOTE |
|--------------------|----------|------|-----|--------------|------|------|
| Supply voltage     | $V_{DD}$ | 3.0  | 3.3 | 3.6          | V    |      |
| Input high voltage | $V_{IH}$ | 2.0  |     | $V_{DD}+0.3$ | V    |      |
| Input low voltage  | $V_{IL}$ | -0.3 |     | 0.8          | V    |      |

**CAPACITANCE** ( $V_{DD}=3.3V$ ,  $T_A=25^{\circ}C$ ,  $f=1MHz$ ,  $V_{REF}=1.4V+200mV$ )

| PARAMETER                                          | SYMBOL    | TYP | MAX | UNIT |
|----------------------------------------------------|-----------|-----|-----|------|
| Input capacitance ( $A_0 - A_{10}, BS$ )           | $C_{IN1}$ | 2.5 | 5   | Pf   |
| Input capacitance ( $/RAS, /CAS, /WE$ )            | $C_{IN2}$ | 2.5 | 5   | Pf   |
| Input capacitance (CKE)                            | $C_{IN3}$ | 2.5 | 5   | Pf   |
| Input capacitance (CLK)                            | $C_{IN4}$ | 2.5 | 5   | Pf   |
| Input capacitance ( $/CS$ )                        | $C_{IN5}$ | 2.5 | 5   | Pf   |
| Input capacitance (DQM)                            | $C_{IN6}$ | 2.5 | 5   | Pf   |
| Data input/output capacitance ( $DQ_0 - DQ_{15}$ ) | $C_{I/O}$ | 4.0 | 6.5 | Pf   |

## TABLE OF OPERATING MODES

## COMMAND TRUTH TABLE

| FUNCTION                  | SYMBOL | CKE |   | /CS | /RAS | /CAS | /WE | BA | A10 | A9 - A0 |
|---------------------------|--------|-----|---|-----|------|------|-----|----|-----|---------|
|                           |        | n-1 | N |     |      |      |     |    |     |         |
| Device deselect           | DESL   | H   | X | H   | X    | X    | X   | X  | X   | X       |
| No operation              | NOP    | H   | X | L   | H    | H    | H   | X  | X   | X       |
| Mode register set         | MRS    | H   | X | L   | L    | L    | L   | L  | L   | V       |
| Bank activate             | ACT    | H   | X | L   | L    | H    | H   | V  | V   | V       |
| Read                      | READ   | H   | X | L   | H    | L    | H   | V  | L   | V       |
| Read with auto precharge  | READA  | H   | X | L   | H    | L    | H   | V  | H   | V       |
| Write                     | WRIT   | H   | X | L   | H    | L    | L   | V  | L   | V       |
| Write with auto precharge | WRITA  | H   | X | L   | H    | L    | L   | V  | H   | V       |
| Precharge select bank     | PRE    | H   | X | L   | L    | H    | L   | V  | L   | X       |
| Precharge all banks       | PALL   | H   | X | L   | L    | H    | L   | X  | H   | X       |
| Burst stop                | BST    | H   | X | L   | H    | H    | L   | X  | X   | X       |
| CBR (Auto) refresh        | REF    | H   | H | L   | L    | L    | H   | X  | X   | X       |
| Self refresh              | SELF   | H   | L | L   | L    | L    | H   | X  | X   | X       |
| Data mask/output disable  | MASK   | H   | X | X   | X    | X    | X   | X  | X   | X       |
| Clock suspend mode entry  |        | H   | L | X   | X    | X    | X   | X  | X   | X       |
| Clock suspend             |        | L   | L | X   | X    | X    | X   | X  | X   | X       |
| Clock suspend mode exit   |        | L   | H | X   | X    | X    | X   | X  | X   | X       |
| Power down entry          |        | H   | L | X   | X    | X    | X   | X  | X   | X       |
| Power down exit           |        | L   | H | X   | X    | X    | X   | X  | X   | X       |

H:High level, L:Low level

X:High or Low level (Don't care), V: Valid Data input

**AC CHARACTERISTICS AND OPERATING CONDITION**(V<sub>CC</sub>=3.3V±0.3V, Ta=0° to 70°C Notes : 5,6,7)

| SYMBOL           | PARAMETER                               | -6<br>(143MHz)                    |      | -7<br>(100MHz)                    |      | UNITS |
|------------------|-----------------------------------------|-----------------------------------|------|-----------------------------------|------|-------|
|                  |                                         | MIN                               | MAX  | MIN                               | MAX  |       |
| t <sub>RC</sub>  | Ref/Active to Ref/Active Command Period | 63                                |      | 72                                |      | ns    |
| t <sub>RAS</sub> | Active to precharge Command Period      | 42                                | 100K | 50                                | 100K |       |
| t <sub>RCD</sub> | Active to Read/Write Command Delay Time | 20                                |      | 20                                |      |       |
| t <sub>CCD</sub> | Read/Write(a) to Read/Write(b) Command  | 1                                 |      | 1                                 |      | cycle |
| t <sub>RP</sub>  | Precharge to Active(b) Command Period   | 20                                |      | 20                                |      | ns    |
| t <sub>RRD</sub> | Active(a) to Active(b) Command Period   | 14                                |      | 20                                |      |       |
| t <sub>CK</sub>  | CLK Cycle Time                          | 7                                 |      | 10                                |      |       |
| t <sub>CH</sub>  | CLK High Level                          | 2.5                               |      | 3                                 |      |       |
| t <sub>CL</sub>  | CLK Low Level                           | 2.5                               |      | 3                                 |      |       |
| t <sub>AC</sub>  | Access Time from CLK                    |                                   | 6    |                                   | 7    |       |
| t <sub>OH</sub>  | Output Data Hold Time                   | 2.5                               |      | 3                                 |      |       |
| t <sub>HZ</sub>  | Output Data High Impedance Time         |                                   | 5    |                                   | 5    |       |
| t <sub>LZ</sub>  | Output Data Low Impedance Time          | 1                                 |      | 0                                 |      |       |
| t <sub>SB</sub>  | Power Down Mode Entry Time              | 5                                 |      |                                   |      |       |
| t <sub>T</sub>   | Transition Time of CLK(Rise and Fall)   | 0.5                               | 10   | 1                                 | 10   |       |
| t <sub>DS</sub>  | Data-in-Set-up Time                     | 2                                 |      | 2                                 |      |       |
| t <sub>DH</sub>  | Data-in Hold Time                       | 1                                 |      | 1                                 |      |       |
| t <sub>AS</sub>  | Address Set-up Time                     | 2                                 |      | 2                                 |      |       |
| t <sub>AH</sub>  | Address Hold Time                       | 1                                 |      | 1                                 |      |       |
| t <sub>CKS</sub> | CKE Set-up Time                         | 2                                 |      | 2                                 |      |       |
| t <sub>CKH</sub> | CKE Hold Time                           | 1                                 |      | 1                                 |      |       |
| t <sub>CMS</sub> | Command Set-up Time                     | 2                                 |      | 2                                 |      |       |
| t <sub>CMH</sub> | Command Hold Time                       | 1                                 |      | 1                                 |      |       |
| t <sub>REF</sub> | Refresh Time                            |                                   | 64   |                                   | 64   | ms    |
| t <sub>RSC</sub> | Mode Register Set Cycle Time            | 2                                 |      | 2                                 |      | CLK   |
| t <sub>DPL</sub> | Data in to Precharge                    | 1                                 |      | 1                                 |      |       |
| t <sub>BDL</sub> | Last Data in to Burst Stop              | 1                                 |      | 1                                 |      |       |
| t <sub>DAL</sub> | Data in to Active Command               | t <sub>DPL</sub> +t <sub>RP</sub> |      | t <sub>DPL</sub> +t <sub>RP</sub> |      |       |

(CL=CAS Latency)

## MODE REGISTER (ADDRESS INPUT FOR MODE SET)

|    |    |   |   |   |          |   |   |   |   |   |   |
|----|----|---|---|---|----------|---|---|---|---|---|---|
| 11 | 10 | 9 | 8 | 7 | 6        | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0 | 0 | 1 | Reserved |   |   |   |   |   |   |

JEDEC Standard test Set

| 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4  | 3  | 2 | 1 | 0 |
|----|----|---|---|---|--------|---|----|----|---|---|---|
| x  | x  | 1 | 0 | 0 | LTMODE |   | WT | BL |   |   |   |

Burst Read and Single Write (for Write Through Cache)

|    |    |   |   |   |        |   |    |    |   |   |   |
|----|----|---|---|---|--------|---|----|----|---|---|---|
| 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4  | 3  | 2 | 1 | 0 |
| x  | x  | 0 | 0 | 0 | LTMODE |   | WT | BL |   |   |   |

Burst Read and Burst Write

X=Don't care

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| Burst length | Bits2-0 | WT=0      | WT=1 |
|--------------|---------|-----------|------|
|              | 000     | 1         | 1    |
|              | 001     | 2         | 2    |
|              | 010     | 4         | 4    |
|              | 011     | 8         | 8    |
|              | 100     | R         | R    |
|              | 101     | R         | R    |
|              | 110     | R         | R    |
|              | 111     | Full page | R    |

| Wrap type | 0 | Sequential |
|-----------|---|------------|
|           | 1 | Interleave |

| Latency mode | Bits6-4 | /CAS latency |
|--------------|---------|--------------|
|              | 000     | R            |
|              | 001     | R            |
|              | 010     | 2            |
|              | 011     | 3            |
|              | 100     | R            |
|              | 101     | R            |
|              | 110     | R            |
|              | 111     | R            |

Remark R: Reserved

## DC CHARACTERISTICS

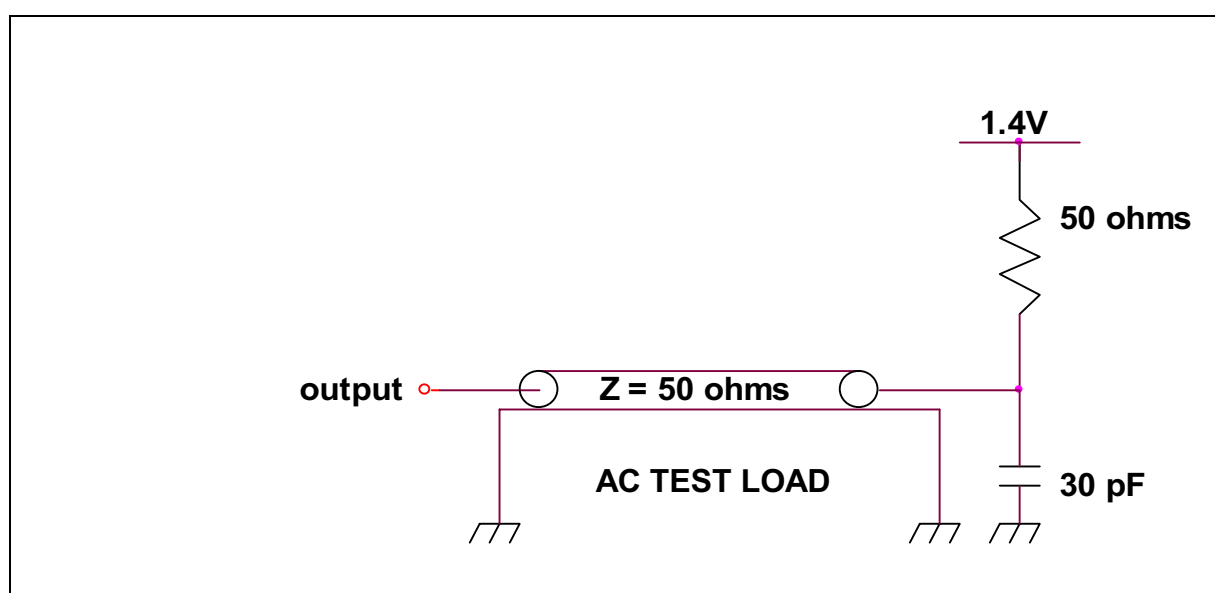
Recommended D.C. Operating condition ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^\circ C$ )

| DESCRIPTION/TEST CONDITION                                                                                                                                                    | SYMBOL      | -6   |      | -7   |      | UNIT |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|------|------|------|------|
|                                                                                                                                                                               |             | Min. | Max. | Min. | Max. |      |
| Operating Current<br>$t_{RC} \geq t_{RC(min)}$ , Outputs Open<br>Address changed once during $t_{CK(min)}$ .<br>Burst Length = 1 (One Bank Active)                            | $I_{DD1}$   |      | 110  |      | 120  | mA   |
| Precharge Standby Current in non power-down mode<br>$t_{CK} = t_{CK(min)}$ , $/CS \geq V_{IH(min)}$ , $CKE \geq V_{IH(min)}$ ,<br>Input signals are changed once during 30ns. | $I_{DD2N}$  |      | 40   |      | 50   |      |
| Precharge Standby Current in non power-down mode<br>$t_{CK} = \infty$ , $CKE \geq V_{IH(min)}$ , $CLK \leq V_{IL(max)}$ ,<br>Input signals are stable                         | $I_{DD2NS}$ |      | 20   |      | 30   |      |
| Precharge Standby Current in power-down mode<br>$t_{CK} = t_{CK(min)}$ , $CKE \leq V_{IL(max)}$                                                                               | $I_{DD2P}$  |      | 2    |      | 3    |      |
| Precharge Standby Current in power-down mode<br>$t_{CK} = \infty$ , $CKE \leq V_{IL(max)}$ , $CLK \leq V_{IL(max)}$                                                           | $I_{DD2PS}$ |      | 2    |      | 2.8  |      |
| Active Standby Current in non power-down mode<br>$CKE \geq V_{IH(min)}$ , $t_{CK} = t_{CK(min)}$ (Both Bank Active)                                                           | $I_{DD3N}$  |      | 60   |      | 70   |      |
| Active Standby Current in power-down mode<br>$CKE \leq V_{IL(max)}$ , $t_{CK} = t_{CK(min)}$ , $/CS \geq V_{IH(min)}$ (Both Bank Active)                                      | $I_{DD3P}$  |      | 5    |      | 5    |      |
| Operating Current(Page Burst, and All Bank activated)<br>$t_{CCD} = t_{CCD(min)}$ , Outputs Open, Multi-bank interleave, gapless data                                         | $I_{DD4}$   |      | 120  |      | 130  |      |
| Refresh Current<br>$t_{RC} \geq t_{RC(min)}$ , ( $t_{REF} = 32ms$ )                                                                                                           | $I_{DD5}$   |      | 120  |      | 130  |      |
| Self Refresh Current<br>$CKE \leq 0.2V$                                                                                                                                       | $I_{DD6}$   |      | 2    |      | 2.5  |      |

| PARAMETER | DESCRIPTION                                                                                 | MIN. | MAX. | UNIT    |
|-----------|---------------------------------------------------------------------------------------------|------|------|---------|
| $I_{IL}$  | Input Leakage Current<br>( $0V \leq V_{IN} \leq V_{DD}$ All other pins not under test = 0V) | -5   | 5    | $\mu A$ |
| $I_{OL}$  | Output Leakage Current<br>Output disable, ( $0V \leq V_{OUT} \leq V_{DDQ}$ )                | -5   | 5    | $\mu A$ |
| $V_{OH}$  | LVTTL Output "H" Level Voltage<br>( $I_{OUT} = -2mA$ )                                      | 2.4  | -    | V       |
| $V_{OL}$  | LVTTL Output "L" Level Voltage<br>( $I_{OUT} = 2mA$ )                                       | -    | 0.4  | V       |

| PARAMETER                                        | CONDITIONS                             |
|--------------------------------------------------|----------------------------------------|
| Reference Level of Output Signals                | 1.4V/1.4V                              |
| Output board                                     | Reference to the Under Output Load (B) |
| Input Signal Levels                              | 3.0V / 0.0V                            |
| Transition Time (Rise and Fall) of Input Signals | 1nS                                    |
| Reference Level of Input Signals                 | 1.4V                                   |

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