Vendor PN:VT1165MFQX

VOLTERRA

REVISION - December 8, 2005

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Smart Slave™	Current Rating	Input Voltage	Output Voltage	VID
VT1105S*	25A per Phase	10.8V to 13.2V	0.800V to 1.850V or 0.450V to 2.0375V	VRMs 9, 10.X, and Opteron™ or Serial VID (SVID) Mode
VT1125S				
VT1115S	30A per Phase			
VT1135S				

GENERAL DESCRIPTION

The VT1165M chipset, Volterra's fourth-generation chipset, is a complete, integrated, scalable architecture for the highest density multi-phase synchronous buck regulators. This ultra high density solution minimizes external components and offers enhanced regulator performance, comprehensive control and reporting features, ease of design and the smallest footprint available for demanding multi-phase synchronous buck converters. The chipset is targeted for applications such as servers and networking systems.

The VT1165M system architecture consists of a master controller (VT1165M), multiple Smart Slave™ integrated output devices, input capacitors, output capacitors and output inductors. The actual number of Smart Slaves™ can be set by the designer and application requirements. The desired slave and load operating conditions are controlled and monitored via an interconnecting digital bus as shown in Figure 1.

With this chipset, Volterra implements enhancements to the digital SMBus interface for monitoring and controlling of the voltage regulator. Regulator parameters can be set and monitored via the two-way SMBus for control, protection and shutdown of the regulator. The SMBus can provide a reading of faults such as VX short-circuit or slave over-temperature, so that the regulator can be controlled and protected during all operating conditions. The SMBus can also provide temperature readings of individual slaves.

A key benefit of the VT1165M is that it provides excellent scalability. This flexibility allows the designer to trade-off cost and performance for a given application using one VT1165M controller and different slave configurations with no redesign or re-layout. The number of phases can be determined by the designer and easily populated or de-populated to meet different load and performance targets.

***NOTE: The VT1165M, VT1115S, VT1125S & VT1135S have a status of PRELIMINARY. The VT1105S has a status of NEW PRODUCT. See the back page of this datasheet for details on these statuses.**

KEY FEATURES

- **Smallest Footprint: Typical Solution Occupies Less than 1600mm^2 in a 150A VRM Application**
- **Lowest Profile: 5mm Maximum Height**
- **Highest Accuracy Current Sharing**
- **Differential Voltage Sense at Point of Load**
- **1A/ns Step Load Transient Response**
- **Scalable Output Current: Up to 8 Slaves**
- **Slave Temperature Reporting**
- **Compatible with Coupled Inductors**
- **Programmable Switching Frequency: 500kHz-1.5MHz**
- **6-Bit VID Input, with 12.5mV Steps and Setpoint Trim for Programmable V_{OUT}**
  - **Intel® VRM 9: 1.100V-1.850V**
  - **Intel® VRM 10.X: 0.8375V-1.6000V**
  - **AMD® Opteron™: 0.800V-1.550V**
  - **Serial VID (SVID) Mode: 0.450V-2.0375V**
- **Dynamic VID**
- **Programmable VID via SMBUS**
- **Programmable Setpoint and Droop**
- **Programmable OVP, OVLO and UVLO**
- **Cycle-by-Cycle Current Limiting**
- **Power Good Flag, Fault Flag and Output Enable**

SYSTEMS

- **Servers and Workstations**
- **Enterprise Storage**
- **Broadband Communication & Networking**
- **Small Form Factor Desktops**

APPLICATIONS

Voltage Regulator Modules (VRMs) and On-Board Regulators (VR Down)

- **Microprocessors (μP): 32 and 64 Bit I/A and RISC Architectures**
- **Memory**
- **Graphics Processors**
- **Network, Chipset ICs**

BASIC APPLICATION CIRCUIT

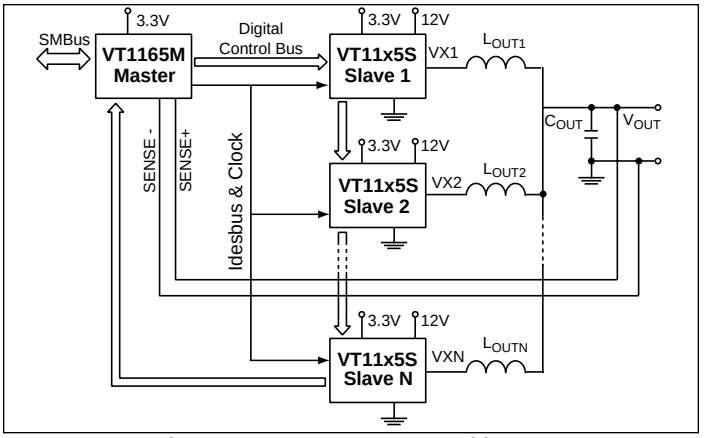


Figure 1. VT1165M System Architecture

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ORDERING INFORMATION

Part Number	IC	Package Style	Drawing Number	Shipment Method	Package Marking
VT1165MQ	Master	QFN-40	ES AP-0906	Trays	VT1165M
VT1165MQX				2.5ku Tape & Reel	
VT1105SCR	25A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105S
VT1105SCX				2.5ku Tape & Reel	
VT1115SCR	30A Smart Slave™	CSP-53	ES AP-1088	250u Tape & Reel	VT1115S
VT1115SCX				2.5ku Tape & Reel	
VT1125SCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125S
VT1125SCX				2.5ku Tape & Reel	
VT1135SCR	30A Smart Slave™	CSP-41	ES AP-0804	250u Tape & Reel	VT1135S
VT1135SCX				2.5ku Tape & Reel	
Lead-Free Options (RoHS Compliant)					
VT1165MFQ	Master	QFN-40	ES AP-0906	Trays	VT1165MF
VT1165MFQX				2.5ku Tape & Reel	
VT1105SFCR	25A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105SF
VT1105SFCX				2.5ku Tape & Reel	
VT1115SFCR	30A Smart Slave™	CSP-53	ES AP-1088	250u Tape & Reel	VT1115SF
VT1115SFCX				2.5ku Tape & Reel	
VT1125SFCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125SF
VT1125SFCX				2.5ku Tape & Reel	
VT1135SFCR	30A Smart Slave™	CSP-41	ES AP-0804	250u Tape & Reel	VT1135SF
VT1135SFCX				2.5ku Tape & Reel	

ABSOLUTE MAXIMUM RATINGS (SEE NOTE 1)

Supply Voltage (12V) ..... -0.3V to 16V
Supply & Input Pin Voltages (3.3V) ..... -0.3V to 4V
VT1165M SC and SD Pin Voltages ..... -0.3V to 7V
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... -65° to 150°C
Peak Reflow Temperature Eutectic ..... 245°C
Peak Reflow Temperature Lead-Free ..... 260°C

THERMAL RATINGS

Θ_{JC} Max (QFN-40) ..... 14.8°C/W
Θ_{JC} Max (CSP-41) ..... 0.6°C/W
Θ_{JC} Max (CSP-52) ..... 0.5°C/W
Θ_{JC} Max (CSP-53) ..... 0.5°C/W
Θ_{JC} Max (CSP-69) ..... 0.3°C/W
Θ_{JA}[2] Typ (CSP-41) ..... 21°C/W
Θ_{JA}[2] Typ (CSP-52) ..... 19°C/W
Θ_{JA}[2] Typ (CSP-53) ..... 19°C/W
Θ_{JA}[2] Typ (CSP-69) ..... 17°C/W

OPERATING RATINGS

Input 3.3V Voltages (Master &Slave) ..... 2.97V to 3.63V
Slave 12V Supply ..... 10.8V to 13.2V
Junction Temperature (T_J) Master & Slave ..... 0° to 125°C
Frequency (Fsw) ..... 500kHz to 1.5MHz
Design Guideline for Maximum Slave DC Output Current (VT1105S, VT1125S) 25A
Design Guideline for Maximum Slave DC Output Current (VT1115S, VT1135S) 30A
Electrical DC Current Limit Per Slave Assuming No Thermal Limitations (VT1105S, VT1125S) 30A
Electrical DC Current Limit Per Slave Assuming No Thermal Limitations (VT1115S, VT1135S) 36A
Peak Instantaneous Slave Current (VT1105S, VT1125S) 56A
Peak Instantaneous Slave Current (VT1115S, VT1135S) 63A

NOTE 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2: Data taken with Volterra's evaluation kit.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS

V_{DD-M} = V_{DD-S} = V_{CC-S} = 3.3V ±10%, V_{DD-H} = 10.8V to 13.2V unless otherwise specified. The ✻ symbol denotes specifications which apply over the following operating junction temperature ranges ($T_{J-SLAVE}$ = 0 to 125°C and $T_{J-MASTER}$ = 0 to 100°C), otherwise specifications are for T_J = 25°C. The # denotes parameters that are programmable.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Supply Voltages, V_{DD} and V_{CC}								
V_{DD-M}	Supply Voltage Range (Master)			✻	2.97	3.3	3.63	V
V_{DD-S}, V_{CC-S}	Supply Voltage Range (Slave 3.3V)			✻	2.97	3.3	3.63	V
V_{DDH}	Supply Voltage Range (Slave 12V)			✻	10.8	12.0	13.2	V
I_{DD-M}	Supply Current (Master)	PWM				13		mA
		Shutdown, OE = 0				10		mA
I_{DD-S}, I_{CC-S}	Supply Current (Slave 3.3V)	VT1105S	PWM			45		mA
			Shutdown			20		mA
		VT1115S	PWM			25		mA
			Shutdown			20		mA
		VT1125S	PWM			55		mA
			Shutdown			20		mA
		VT1135S	PWM			25		mA
			Shutdown			20		mA
I_{DDH}	Quiescent Supply Current (Slave 12V)	VT1105S				1		mA
		VT1115S				2		mA
		VT1125S				1		mA
		VT1135S				2		mA
Output Voltage and DC Accuracy								
V_{OUT}	Output Voltage Range	VRM 9 VID Code		✻	1.100		1.850	V
		VRM 10.X VID Code		✻	0.8375		1.6000	V
		Opteron™ VID Code		✻	0.800		1.550	V
$ERROR_{MASTER-REF}$	DC Setpoint Accuracy (including voltage reference and master amplifier)	Full VID Range: The Greater of		✻	-6 or -0.8		+9 or 0.8	mV %
Regulation and System Specifications (Specified by design, tested using circuits in Figures 5 & 6)								
ΔV_{OUT}	Line Regulation	$V_{DDH-S12V}$ = 12V ±10%				5		mV
	Output Ripple					10		mV
SR_{OUT}	Output Slew Rate					1000		A/µs
$T_{TURN-ON}$	Turn-On Response Time. Time to V_{OUT} > 95% of Final Value.	From V_{DD-M} > UVLO (8 slaves, I_{MAX} = 28A, 800kHz, 300µF/slave, C_{NOM} = 6.8nF). Includes configuration time.			4.6		5.4	ms
		From OE Positive Edge (8 slaves, I_{MAX} = 28A, 800kHz, 300µF/slave, C_{NOM} = 6.8nF)			0	100	200	µs
$V_{OVERSHOOT}$	Turn-On Overshoot	Built in Soft Start					0	%
$V_{UNDERSHOOT}$	Turn-Off Undershoot	30Ω Load				0		mV
$CMRR_{SENSE}$	Common-Mode Rejection Ratio of Differential Sense					40		dB
I_{SENSE}	SENSE Pin Currents	SENSE+ Sinking, SENSE- Sourcing				60	100	µA

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Regulation and System Specifications (Specified by design, tested using circuits in Figures 5 & 6) (CONTINUED)								
Eff	Efficiency (Measured at Inductor), 6 Phases	VT1105S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			80		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			83		%
	Efficiency (Measured at Inductor), 6 Phases	VT1115S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			83		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			85		%
	Efficiency (Measured at Inductor), 6 Phases	VT1125S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			83		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			85		%
	Efficiency (Measured at Inductor), 6 Phases	VT1135S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			80		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			83		%
Slave Scalability and Peak Current Limit								
N_{SLAVE}	Maximum total number of slaves						8	
I_{LIM-SL}	Peak Current Limit Per Slave	VT1105S, VT1125S					56	A
		VT1115S, VT1135S					63	A
$I_{MAX-SL(DC)}$	DC Maximum Output Current Per Slave	VT1105S, VT1125S		#			25	A
		VT1115S, VT1135S		#			30	A
-	Slave DC Current Accuracy	VT1105S, VT1115S, VT1125S, VT1135S		*		5	7	%
MASTER DIGITAL CONTROL AND STATUS PINS								
Data (SD) and Clock (SC) Pins (SMBus High Power Specification Version 2.0)								
V_{IL}	Input Low Voltage						0.8	V
V_{IH}	Input High Voltage				2.1			V
V_{OL}	Output Low Voltage (SD)	@ I_{SINK}					0.4	V
I_{SINK}	Current Sinking (SD)	V_{OL} = 0.4V			2.5			mA
-	External Pull-Up Voltage						5.5	V
OE and VID[0:5] Pins for VRM 9, Opteron™ and Programmable VID Mode								
V_{IL}	Input Low Voltage						0.8	V
V_{IH}	Input High Voltage				1.7			V
OE and VID[0:5] Pins for VRM 10.X								
V_{IL}	Input Low Voltage						0.4	V
V_{IH}	Input High Voltage				0.8			V

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

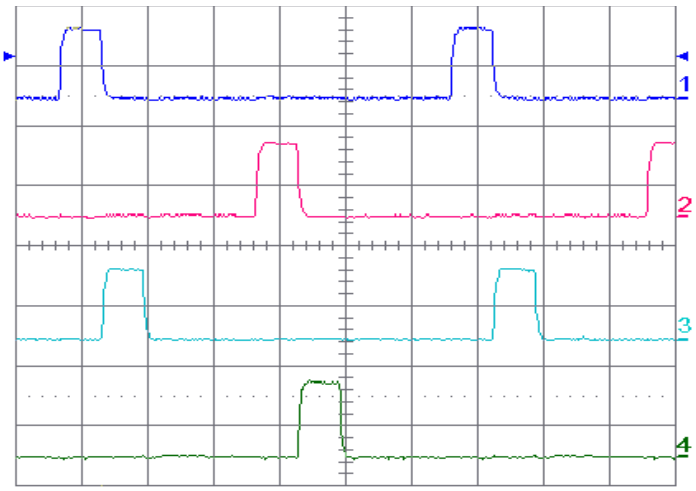
ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PWRGD and FAULTB Pins							
-	PWRGD DC Threshold Error			-40		+40	mV
-	Delay from V_{OUT} to PWRGD	After Startup		8		20	µs
-	PWRGD Lockout after OE goes High (UVLO & OVLO Low)			1.6	2.0	2.4	ms
V_{OL}	Output Low Voltage	@ I_{SINK}				0.4	V
I_{SINK}	Current Sinking (PWRGD, FAULTB)	V_{OL} = 0.4V		2.5			mA
OVP							
-	DC Threshold Error			-40		+40	mV
-	OVP Lockout OE goes High (UVLO & OVLO Low)			1.6	2.0	2.4	ms
OCP							
I_{OCP}	OCP Inception Point	Refer to Table 1C (I_{OCP} for all I_{MAX} settings)					
I_{SC-PK}	Peak Current for Short Circuit	Refer to Table 1D (I_{SC-PK} for all I_{MAX} settings)					
-	Hiccup Period			46	50	54	ms
-	Hiccup Duty Cycle				10		%
-	Latch Off Delay			4.5	5.0	5.5	ms
Undervoltage and Overvoltage Lockout 12V Supply							
IN_UVLO_{RE}	12V UVLO Reference Voltage Rising Edge			1.262	1.300	1.338	V
IN_UVLO_{FE}	12V UVLO Reference Voltage Falling Edge			1.191	1.230	1.269	V
$IN\_UVLO_{HYSTERESIS}$	UVLO Hysteresis			30	67		mV
IN_OVLO_{RE}	12V OVLO Reference Voltage Rising Edge			1.262	1.300	1.338	V
IN_OVLO_{FE}	12V OVLO Reference Voltage Falling Edge			1.191	1.230	1.269	V
$IN\_OVLO_{HYSTERESIS}$	OVLO Hysteresis			30	67		mV
t_{UVLO}, t_{OVLO}	12V UVLO and OVLO Response Time	Including time to shut down the slave			7.25		µs
$t_{UVLO-REC}$, $t_{OVLO-REC}$	12V UVLO and OVLO Recovery Time	Not including soft-start delay			7.25		µs
Undervoltage Lockout 3.3V Supply (Master-Internal)							
3_3V_UVLO	3.3V Internal UVLO	Rising Threshold				2.85	V
		Falling Threshold		2.69			V
$3\_3V\_UVLO_{HYSTERESIS}$	Hysteresis				100		mV
Slave FAULTB Ball (VT1115S, VT1125S, VT1135S)							
$V_{OL-FAULTB}$	FAULTB Output Low Voltage	With 4.7kΩ external pull-up			0.1	0.4	V
$R_{PULLDOWN-FAULTB}$	FAULTB Pull-down Resistance				50	200	Ω
SMBus Reporting							
-	SMBus Current Reporting Error			-10		+10	% of I_{MAX}
SPHASE							
-	SPHASE Clock Period Tolerance	Including 1% Resistor Tolerance	*	-6		+6	%

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS

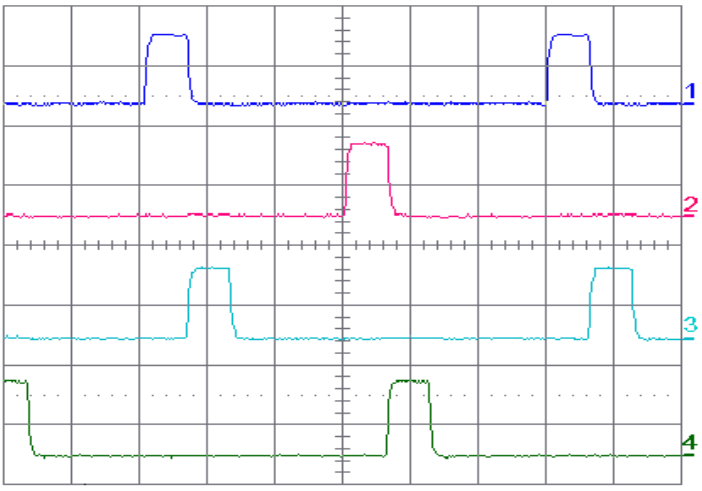
Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 1-4)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #1 (10V/div)
2: Vx Switching Node for Slave #2 (10V/div)
3: Vx Switching Node for Slave #3 (10V/div)
4: Vx Switching Node for Slave #4 (10V/div)
(Triggered From Slave #1)

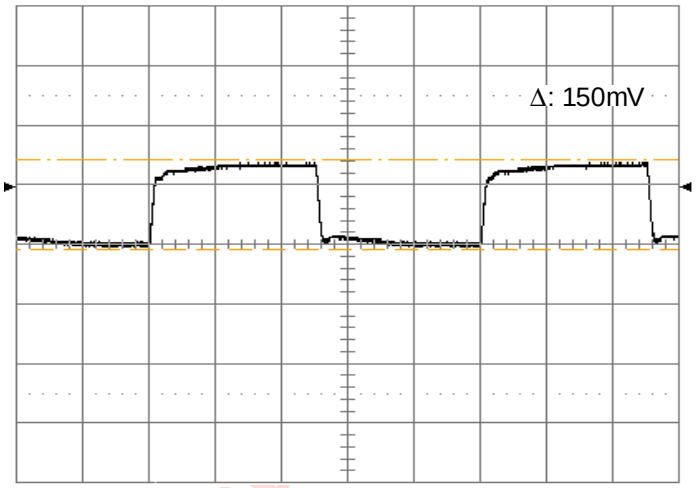
Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 5-8)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #5 (10V/div)
2: Vx Switching Node for Slave #6 (10V/div)
3: Vx Switching Node for Slave #7 (10V/div)
4: Vx Switching Node for Slave #8 (10V/div)
(Triggered From Slave #1)

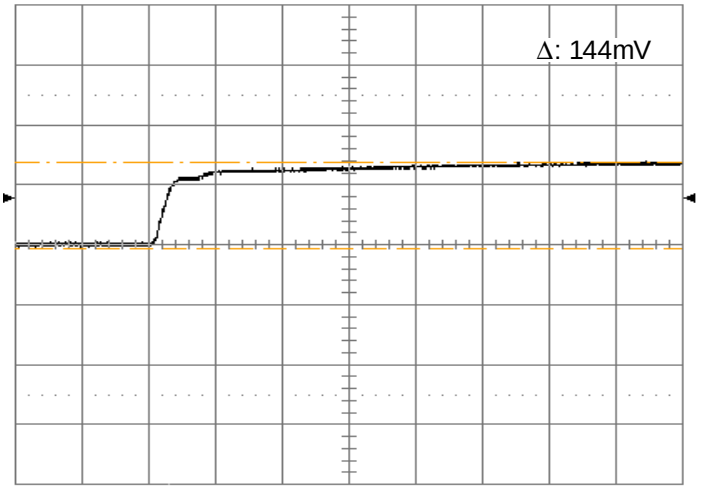
Load Transient Response - 8 Slave VT1105S System



Time/Div: 20µs

Conditions: V_{OUT} = 1.2V, No Load
I_{OUT} = 100A-0A Load Step
Slew Rate > 1000A/µs
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

Output Voltage Overshoot - 8 Slave VT1105S System



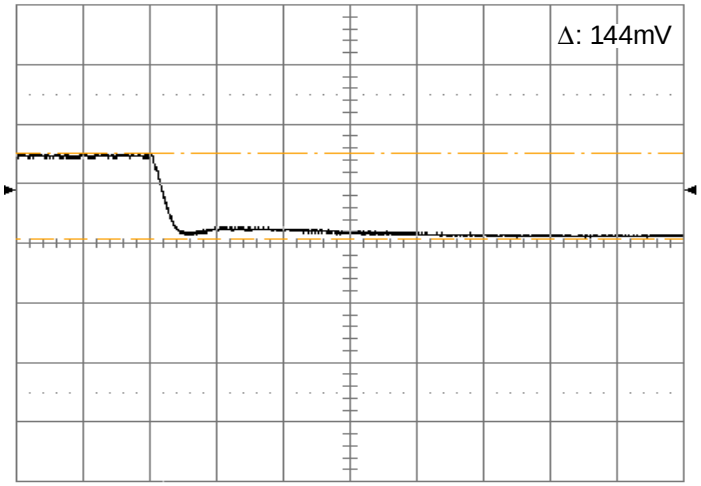
Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A-0A Load Step
Loadline = 1.28mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

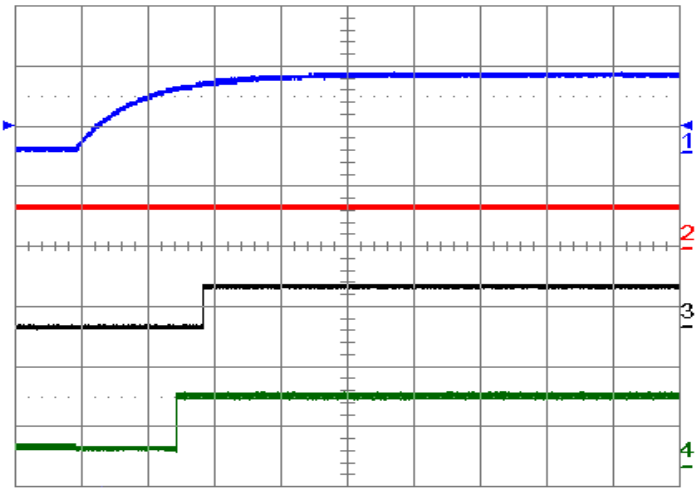
Output Voltage Undershoot - 8 Slave VT1105S System



Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 0-100A Load Step
Loadline = 1.28mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

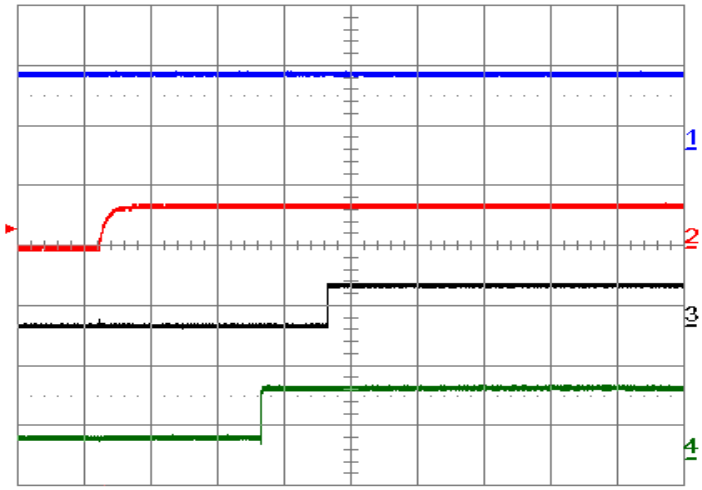
Startup Response References 12V Supply



Time/Div: 5ms

Conditions: V_{OUT} = 1.2V, No Load
1: 12V Input Voltage (10V/div)
2: 3.3V Input Voltage (5V/div)
3: PWRGD Signal (5V/div)
4: Output Voltage (1V/div)

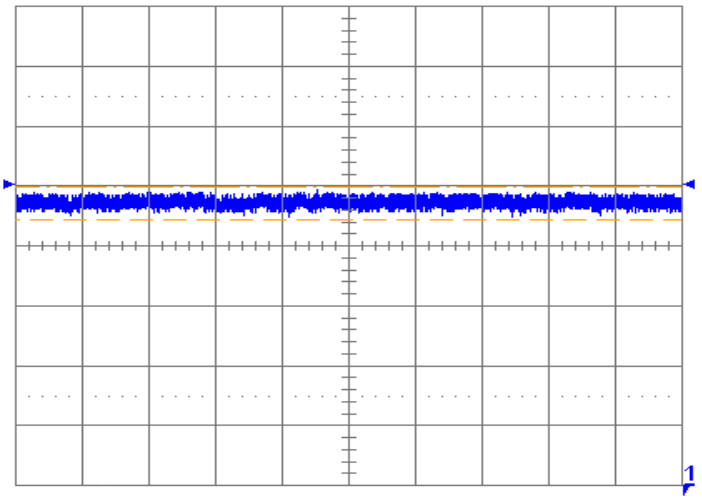
Startup Response References 3.3V Supply



Time/Div: 2ms

Conditions: V_{OUT} = 1.2V, No Load
1: 12V Input Voltage (10V/div)
2: 3.3V Input Voltage (5V/div)
3: PWRGD Signal (5V/div)
4: Output Voltage (1V/div)

Output Ripple - 8 Slave VT1105S System



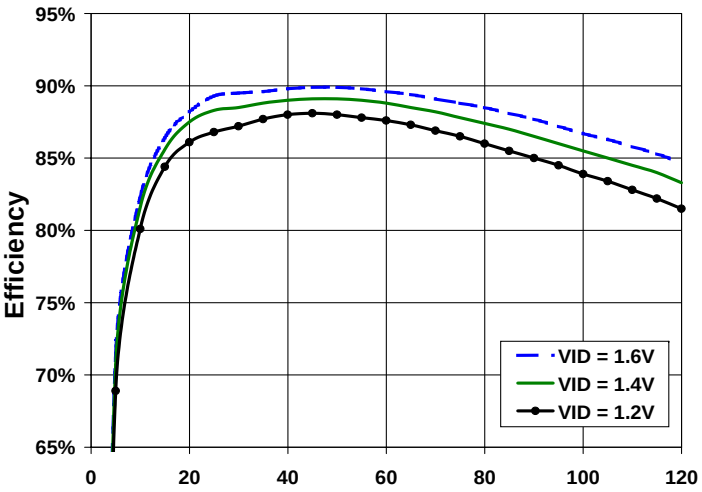
Time/Div: 20µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 160A
C_{OUT} = 58 x 22µF
1: Output Voltage (20mV/div)
25MHz BWL
Measured @ Output Capacitor

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

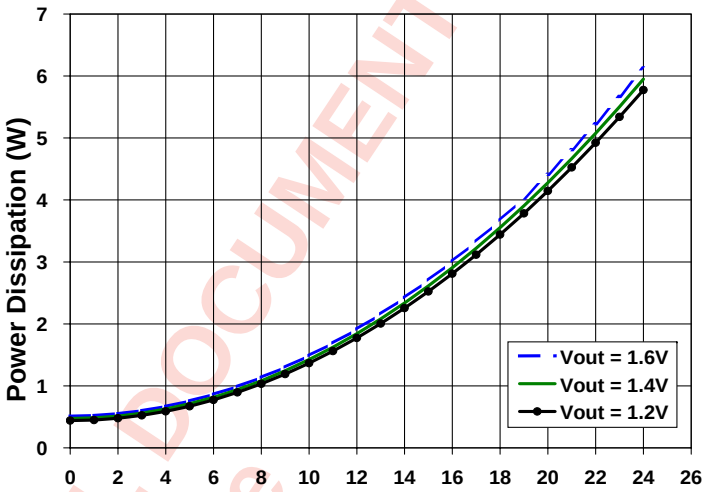
TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

System Efficiency - 5 VT1105S Slaves



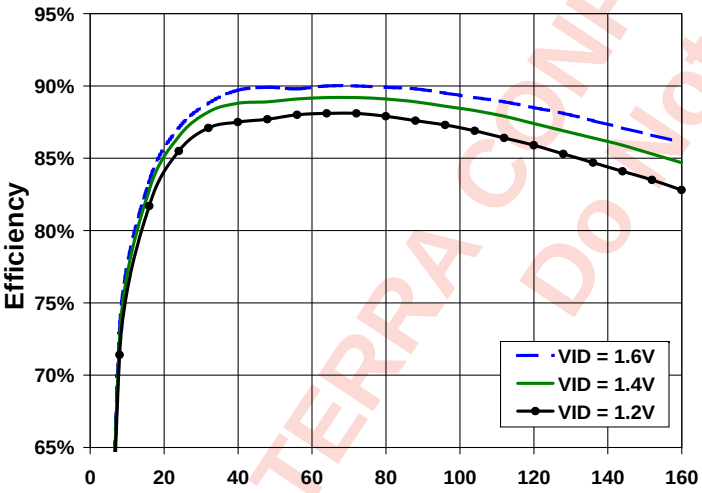
Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 804kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.25mΩ
V_{OUT} Measured @ Inductor

Estimated Power Dissipation - 1 VT1105S Slave



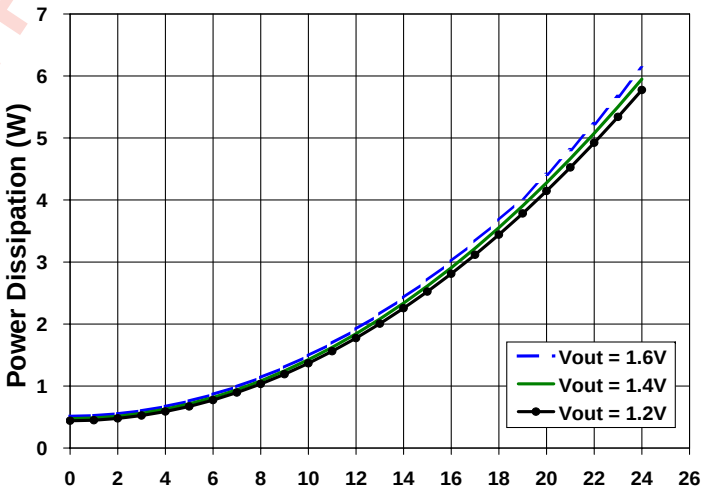
Conditions: V_{IN} = 1.2V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

Typical System Efficiency - 3 VT1135S Slaves



Conditions: V_{IN} = 12V
L_{OUT} = 50nH, 3 phase Coupled L
Fsw = 800kHz
T_A = 25°C
System Loadline = 1.25mΩ
V_{OUT} Measured @ Inductor

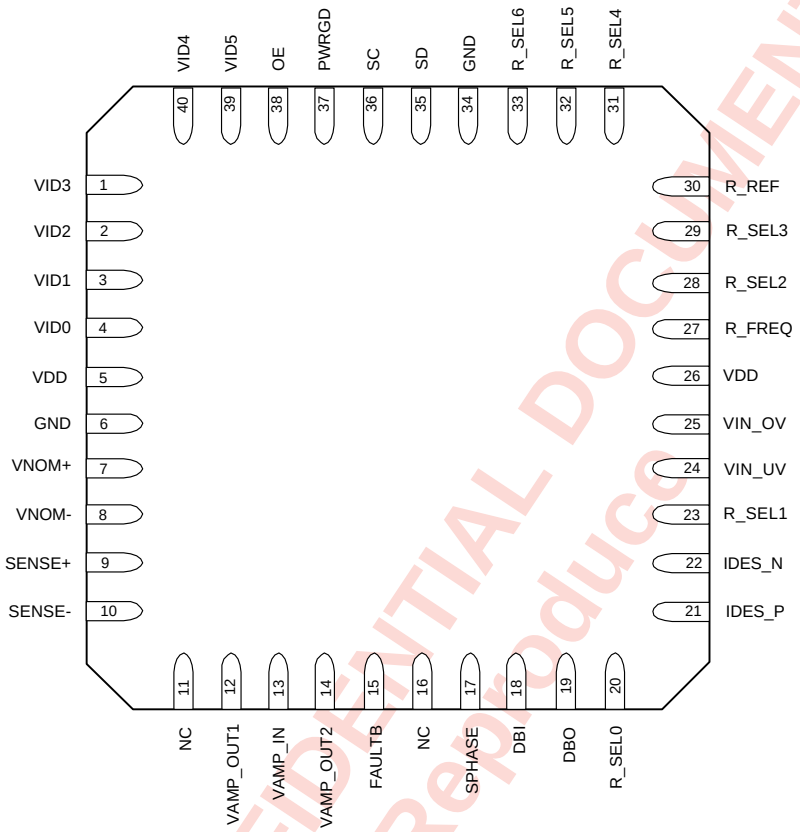
Estimated Power Dissipation - 1 VT1135S Slave



Conditions: V_{IN} = 1.2V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1165M (QFN-40) PINOUT



PIN INFORMATION FOR MASTER CONTROLLER

VID[5:0] (Pins 1-4, 39, 40): Output voltage identification code.

VDD (Pins 5, 26): 3.3V power.

GND (Pins 6, 34): Ground.

VNOM+, VNOM- (Pins 7, 8): DAC output used as the regulation reference. The no-load output voltage is equal to this reference. See the Output Voltage Programming section for additional design information.

SENSE+ (Pin 9): Positive remote sense.

SENSE- (Pin 10): Negative remote sense.

NC (Pin 11, 16): No connect.

VAMP_OUT1 (Pin 12): Sense amplifier output.

VAMP_IN (Pin 13): Error amplifier inverting input.

VAMP_OUT2 (Pin 14): Error amplifier output.

FAULTB (Pin 15): Active low fault condition flag. This open drain output should be externally pulled high with a resistor.

SPHASE (Pin 17): Slave phase clock output. This pin provides a switching frequency reference clock signal to each slave in the system. It should be connected to each slave's SPHASE input.

DBI (Pin 18): Digital control bus input.

DBO (Pin 19): Digital control bus output.

R_SEL[6:0] (Pins 20, 23, 28, 29, 31-33): System configuration resistors. (Programmable features detailed in Table 5.)

IDES_P (Pin 21): Idesired command (+).

IDES_N (Pin 22): Idesired command (-).

VIN_UV (Pin 24): Scaled version of slave VDDH voltage for undervoltage shutdown. This pin is used to program the input undervoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VIN_OV (Pin 25): Scaled version of slave VDDH voltage used for overvoltage shutdown. This pin is used to program the input overvoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

R_FREQ (Pin 27): Resistor used to program switching frequency.

R_REF (Pin 30): Reference resistor used to calibrate R_SEL.

SD (Pin 35): Serial data pin for SMBus interface. See the SMBus Communication with the VT1165M section for additional design information. When not in use, this pin should be connected to VDD.

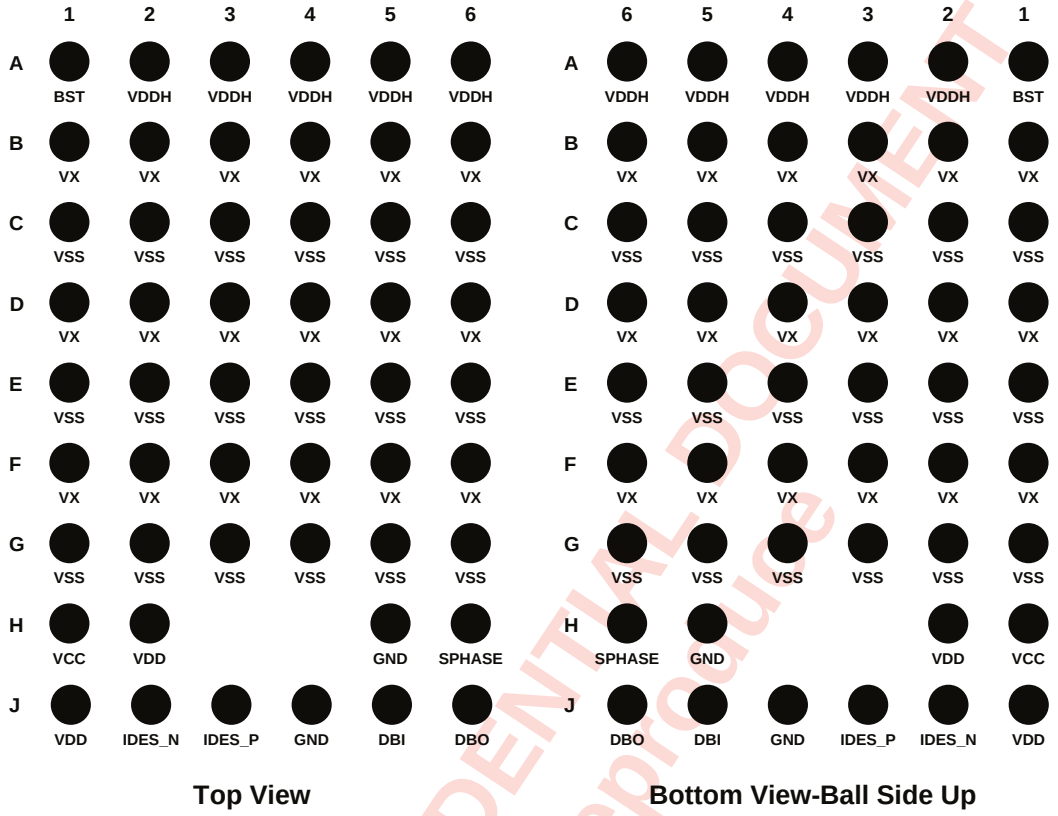
SC (Pin 36): Serial clock pin for SMBus interface. See the SMBus Communication with the VT1165M section for additional design information. When not in use, this pin should be connected to VDD.

PWRGD (Pin 37): Power good output pin. This pin indicates whether the output voltage is within regulation. This open-drain output should be externally pulled HIGH with a resistor. See the Power Good and Undervoltage and Overvoltage Programming and Protection sections for additional design information.

OE (Pin 38): Output enable input pin. When this pin is HIGH, the output voltage is enabled. When this pin is LOW, the output voltage is disabled.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1105S (CSP-52) PINOUT



PIN INFORMATION FOR VT1105S SMART SLAVE™

BST (Ball A1): Bootstrap supply for high side drivers.

VDDH (Balls A2-A6): 12V input supply voltage node. These balls connect to the 12V input power supply source.

VX (Balls B1-B6, D1-D6, F1-F6): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls C1-C6, E1-E6, G1-G6): Power FETs ground node. These balls connect directly to the ground plane.

VCC (Ball H1): 3.3V supply for low side drivers.

VDD (Balls H2, J1): 3.3V supply for control circuits.

GND (Balls H5, J4): Ground for control circuits.

SPHASE (Ball H6): SPHASE clock input from VT1165M master controller.

IDES_N (Ball J2): Negative input side of differential desired current signal.

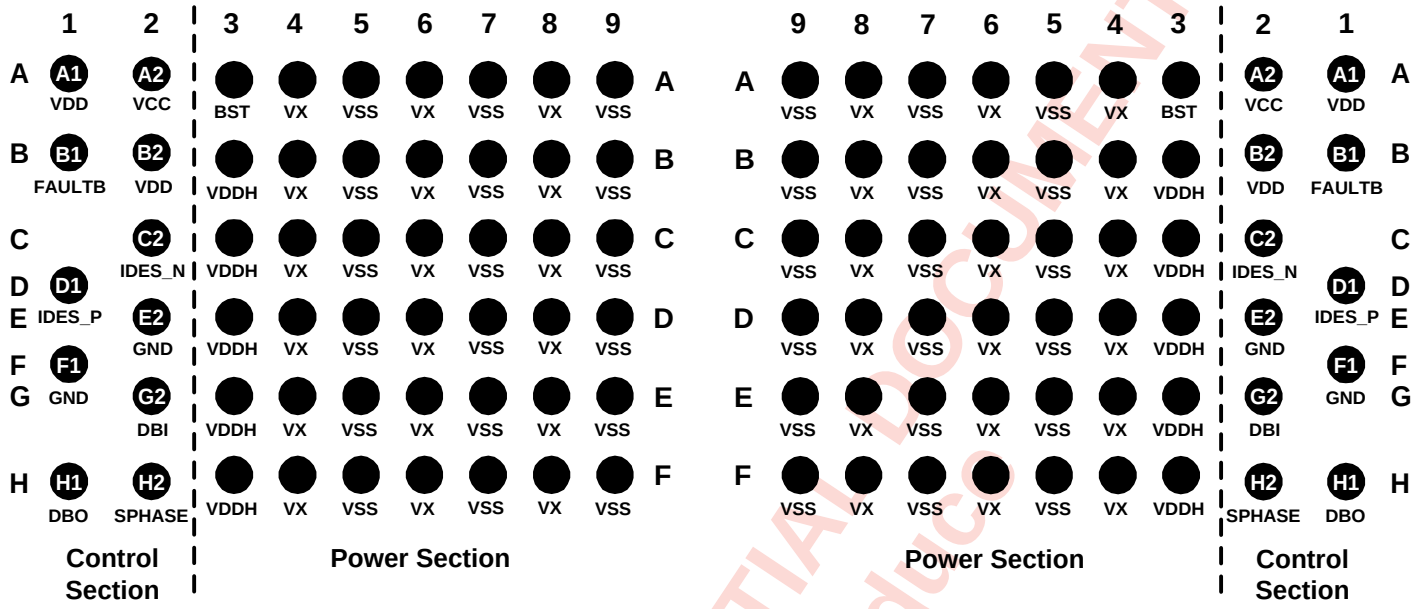
IDES_P (Ball J3): Positive input side of differential desired current signal.

DBI (Ball J5): Digital control bus input.

DBO (Ball J6): Digital control bus output.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1115S (CSP-53) PINOUT



PIN INFORMATION FOR VT1115S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-F4, A6-F6, A8-F8): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-F5, A7-F7, A9-F9): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-F3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

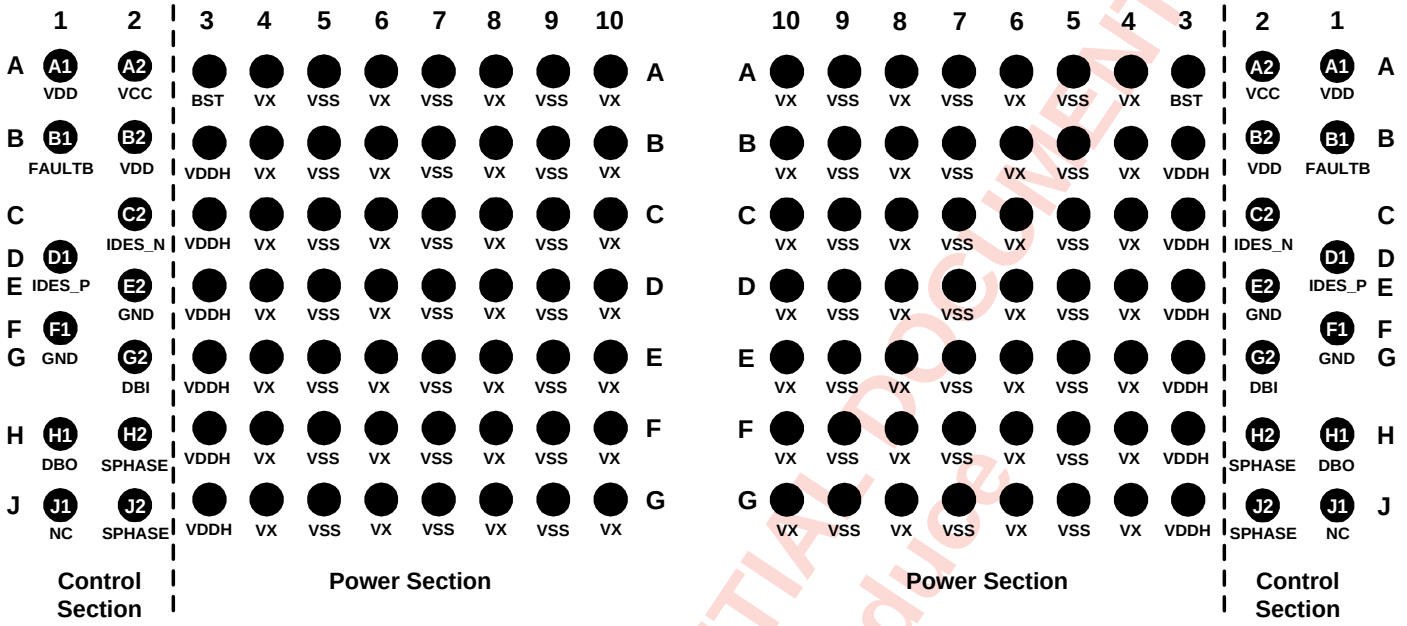
DBI (Ball G2): Digital control bus input.

DBO (Ball H1): Digital control bus output.

SPHASE (Ball H2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1125S (CSP-69) PINOUT



PIN INFORMATION FOR VT1125S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-G4, A6-G6, A8-G8, A10-G10): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-G5, A7-G7, A9-G9): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-G3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

DBI (Ball G2): Digital control bus input.

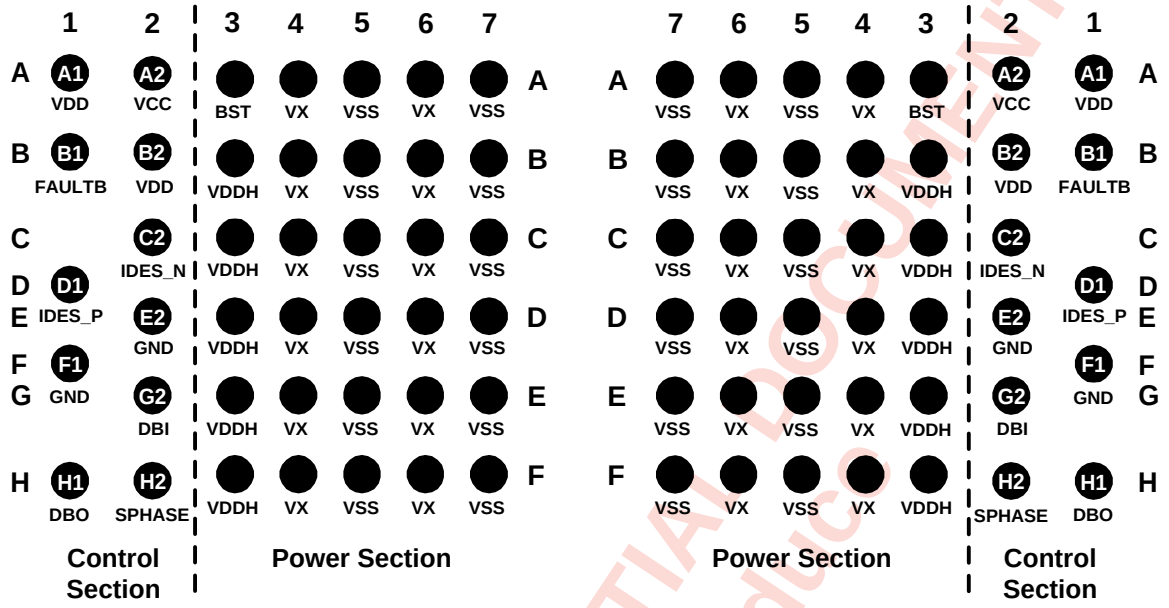
DBO (Ball H1): Digital control bus output.

SPHASE (Balls H2, J2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

NC (Ball J1): No connect.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1135S (CSP-41) PINOUT



PIN INFORMATION FOR VT1135S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-F4, A6-F6): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-F5, A7-F7): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-F3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

DBI (Ball G2): Digital control bus input.

DBO (Ball H1): Digital control bus output.

SPHASE (Ball H2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

OPERATION

The VT1165M chipset provides a high frequency, highly integrated, compact multi-phase solution for high performance, low-voltage power conversion. The basic system architecture consists of a master controller and multiple Smart Slave™ devices. These integrated circuits, along with a small number of external components, provide a complete solution for multi-phase buck voltage regulation.

Synchronous Rectification

Each Smart Slave™ utilizes the full benefits of a synchronous rectification topology. Both the Sync FET and Control FET Power FETs are integrated on-chip and no external power components (MOSFETs or Schottky diodes) are required. During normal device operation, the bottom side switch acts as a synchronous rectifier, carrying the current that would normally flow through an external catch diode. This technique reduces losses associated with the diode's forward voltage drop. The resulting power savings are especially important in low-output-voltage applications.

Control Architecture

The VT1165M system has a fully differential voltage feedback path with excellent common mode rejection and adjustable gain and compensation. The remote output voltage is connected directly to the VT1165M at the SENSE+ and SENSE- pins. The gain of the error amplifier can be set by two external resistor values across the VAMP pins (VAMP_IN, VAMP_OUT1, VAMP_OUT2). Additional resistors and capacitors in parallel with these resistors can provide additional poles and zeros for different compensation schemes.

Desired output current (I_{DES}) is an analog differential signal communicated to the slaves by an Idesired bus (IDES_N, IDES_P). The slaves respond to the Idesired signal by producing a DC current proportional to the differential Idesired voltage, with zero volts commanding zero amps and 1.6V corresponding to the full scale current of the slave. The value of the full scale current is programmable via the selection resistor R_SEL4. The slaves use their own internal control and current sense to switch their own FETs to control their inductor currents at the correct DC level, phase and frequency.

Volterra provides standard reference designs with all of the programmable parameters optimized for common VRM applications.

Output Current Scalability

Each Smart Slave™ incorporates all MOSFETs, gate drivers, control and sense circuitry required to implement a single phase of a multi-phase buck regulation system. The output current of each slave is user programmable via the R_SEL4 resistor of the master controller. Each master controller supports up to 8 phase shifted slaves, controlled via the differential current signal (I_{DES}). Thus with one basic topology the load supplied can be scaled to any output current level and the total maximum output current equals the slave count times the maximum output current setting of each slave. No more

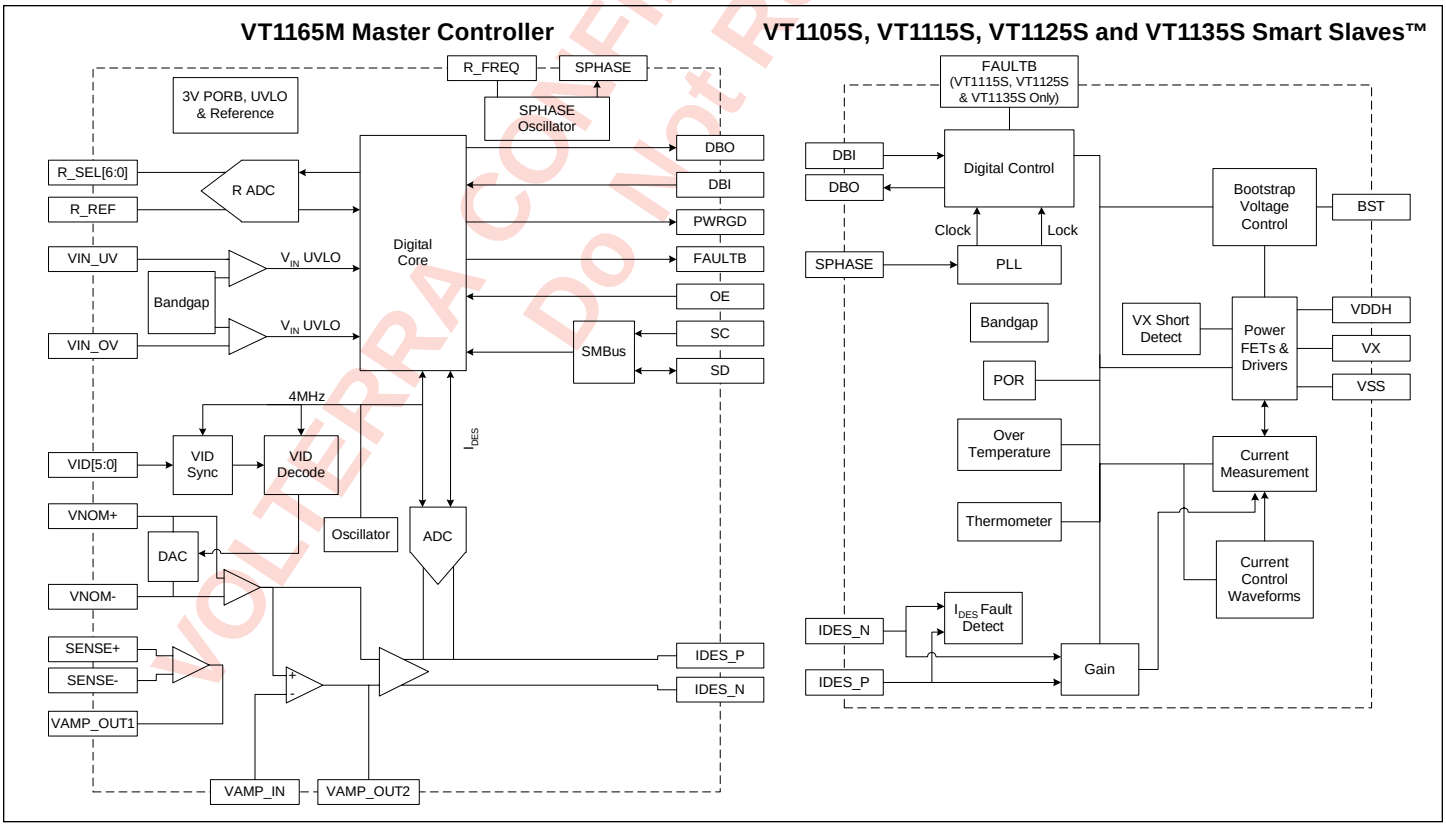


Figure 2. VT1165M Chipset Block Diagram

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

than eight slaves should be connected to a single master, due to fan-out limitations.

Because the architecture requires no additional components or other modifications to support different output currents, a single PCB layout can support a wide range of load currents with simple loading (or unloading) options. The VT1165M supports all Smart Slave™ devices in Volterra's fourth generation architecture.

The maximum output current of each slave is selected by connecting a resistor between the R_SEL4 pin and ground. Tables 1A and 1B provide lists of typical values for R_SEL4 and I_{MAX}. For example, in a VT1125S system where the maximum operating current per slave is 20A, choosing I_{MAX} = 24A is the recommended setting to provide headroom for excursions around the 20A operating value.

Fore each I_{MAX} setting (programmed by R_SEL4), there are two relevant current levels: I_{OCP} and I_{SC_PK}. I_{OCP} indicates the current level at which the system enters the user-specified OCP mode (i.e., hiccup, latchoff or CCM.) I_{SC-PK} indicates the peak current observable during short-circuit conditions. The average DC short-circuit current depends on the OCP mode chosen. Tables 1C and 1D provide detailed current levels.

The R_SEL4 resistor also controls an internal slave setting which affects the current control algorithm during an unloading transient. For applications using uncoupled inductors, internal setting “1” is recommended to minimize the output voltage overshoot during a transient event. When using coupled inductors, setting “3” will provide the optimal transient response.

Output Voltage Programming

The output voltage of the VT1165M chipset is digitally programmable from 0.800V to 1.850V with a DC set point accuracy of ±0.8%. The master controller provides built-in support for the industry standard VID codes as follows:

Table 1A: I_{MAX} Programming for VT1105S and VT1125S

R_SEL4 (Ω)	I_{MAX} (A)	Internal Slave Setting
340	24	1
1.02k	24	2
1.74k	24	3
2.43k	24	4
5.90k	32	1
6.49k	32	2
7.15k	32	3
7.87k	32	4
8.66k	28	4
9.31k	28	3
10.0k	28	2
10.7k	28	1

Table 1B: I_{MAX} Programming for VT1115S and VT1135S

R_SEL4 (Ω)	I_{MAX} (A)	Internal Slave Setting
340 (GND)	24	1
1.02k	24	2
1.74k	24	3
2.43k	24	4
3.09k	36	4
3.74k	36	3
4.42k	36	2
5.11k	36	1
5.90k	32	1
6.49k	32	2
7.15k	32	3
7.87k	32	4
8.66k	28	4
9.31k	28	3
10.0k	28	2
10.7k	28	1
11.3k	26	1
12.1k	26	2
13.0k	26	3
14.0k	26	4
15.4k	38	4
16.9k	38	3
18.7k	38	2
20.5k	38	1
23.7k	34	1
27.4k	34	2
31.6k	34	3
39.2k	34	4
49.9k	30	4
69.8k	30	3
118k	30	2
348k (VDD)	30	1

Table 1C: I_{OCP} Levels for All I_{MAX} Settings

I_{MAX} Setting Programmed by R_SEL4 (A)	I_{OCP} (A)		
	Min	Typ	Max
24	20.9	22.6	24.2
26	22.7	24.5	26.2
28	25.0	26.3	28.2
30	26.3	28.2	30.2
32	28.0	30.1	32.2
34	30.0	32.0	34.2
36	31.6	33.9	36.1
38	33.4	35.8	38.1

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 1D: I_{SC-PK} Levels for All I_{MAX} Settings

I_{MAX} Setting Programmed by R_SEL4 (A)	I_{SC-PK} (A)		
	Min	Typ	Max
24	22.6	23.8	25.0
26	24.6	25.9	27.2
28	26.6	28.0	29.4
30	28.6	30.1	31.6
32	30.5	32.1	33.7
34	32.5	34.2	35.9
36	34.5	36.3	38.1
38	36.4	38.3	40.2

- VRM 9 specification (1.100V to 1.850V)
- VRM 10.X specification (0.8375V to 1.600V)
- Opteron™ VID code specification (0.800V to 1.550V)
- Serial VID (SVID) Mode (0.450V to 2.0375V)

See Tables 19, 20 and 21 for VID tables.

VID code selection is accomplished by connecting a resistor between the R_SEL3 pin and ground. The value of this resistor determines the VID code selected, as shown in Table 2A. In conjunction with the R_SEL3 pin, the VID[5:0] pins program an internal DAC that sets the regulator's output voltage. External resistors can be used to set VID[5:0]. At zero output load, the output voltage is equal to the nominal voltage value. This value depends on the VID standard, VID code and setpoint value. Table 2A shows the nominal voltage for each VID standard.

The VT1165M includes a new Serial VID (SVID) Mode with the following modified behavior for the traditional six VID bits.

- Two pins to select a V_{START} voltage
- Two pins to select between 4 SMBus programmable output voltages
- Two pins tied to V_{DD-M}

In SVID Mode, the 6-bit VID defines a starting (V_{START}) V_{NOM} DAC voltage according to Table 2B.

Override is an SMBus programmable bit which is 0 at power-up, so that until the VT1165M receives an SMBus DAC code or override command, the V_{NOM} DAC voltage (subject to OE and other shutdown/fault conditions) must be equal to V_{START}.

The VID [3:2] bits should both be tied high for default operation.

Programmable Setpoint

The regulator's output voltage setpoint can be adjusted by connecting a resistor from the R_SEL1 pin to ground. The value of this resistor determines the magnitude of the setpoint adjustment, as summarized in Table 3, as well as the OCP mode. Overcurrent protection is discussed in more detail in the Overcurrent Protection Mode section.

Table 2A: VID Code Selection

R_SEL3 (Ω)	Code	VID Code	FAULTB = VRM_HOT	V_{NOM} Value (V)
340 (GND)	0	VRM 10.X	No	VID - 25mV + SP
1.02k	1	VRM 10.X	No	VID - 25mV + SP
1.74k	2	VRM 10.X	Yes	VID - 25mV + SP
2.43k	3	VRM 10.X	Yes	VID - 25mV + SP
3.09k	4	Opteron™	No	VID + 25mV + SP
3.74k	5	Opteron™	No	VID + 25mV + SP
4.42k	6	Opteron™	Yes	VID + 25mV + SP
5.11k	7	Opteron™	Yes	VID + 25mV + SP
5.90k	8	VRM 9	No	VID - 12.5mV + SP
6.49k	9	VRM 9	No	VID - 12.5mV + SP
7.15k	10	VRM 9	Yes	VID - 12.5mV + SP
7.87k	11	VRM 9	Yes	VID - 12.5mV + SP
8.66k	12	SVID Mode	No	SMBus Value
9.31k	13	SVID Mode	No	SMBus Value
10.0k	14	SVID Mode	Yes	SMBus Value
10.7k	15	SVID Mode	Yes	SMBus Value

Table 2B: SVID Functionality (VID [3:2] = 11)

2-Bit Code	Override = 0 V_{START} (VID[1:0])	Override = 1 V_{OUT} Select (VID[5:4])
00	1.00V	SMBus Voltage 1 (Register 21d)
01	1.05V	SMBus Voltage 2 (Register 22d)
10	1.10V	SMBus Voltage 3 (Register 23d)
11	1.15V	SMBus Voltage 4 (Register 24d)

Programmable Droop

The VT1165M chipset enables flexibility in matching system load lines. To achieve the correct system load line, the proper system gain must be chosen via resistor settings on the VT1165M.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 3: Setpoint and Overcurrent Programmability		
R_SEL1 (Ω)	Setpoint Adjust (mV)	OCP Action
340 (GND)	+21.9	Hiccup
1.02k	+18.8	Hiccup
1.74k	+15.6	Hiccup
2.43k	+12.5	Hiccup
3.09k	+9.4	Hiccup
3.74k	+6.3	Hiccup
4.42k	+3.1	Hiccup
5.11k	0	Hiccup
5.90k	-3.1	Hiccup
6.49k	-6.3	Hiccup
7.15k	-9.4	Hiccup
7.87k	-12.5	Hiccup
8.66k	-15.6	Hiccup
9.31k	-18.8	Hiccup
10.0k	-21.9	Hiccup
10.7k	-21.9	Hiccup
11.3k	-21.9	Latch off
12.1k	-18.8	Latch off
13.0k	-15.6	Latch off
14.0k	-12.5	Latch off
15.4k	-9.4	Latch off
16.9k	-6.3	Latch off
18.7k	-3.1	Latch off
20.5k	0	Latch off
23.7k	+3.1	Latch off
27.4k	+6.3	Latch off
31.6k	+9.4	Latch off
39.2k	+12.5	Latch off
49.9k	+15.6	Latch off
69.8k	+18.8	Latch off
118k	+21.9	Latch off
348k (VDD)	FAULT	

System gain relates total system current to output voltage droop where system gain (in current per droop voltage) is described in the following equation:

$$I_{SLAVE} = \frac{R2}{R1} \cdot \left(\frac{I_{MAX}}{1.6}\right) \cdot \{6,13,20\} \cdot V_{DROOP}$$

Where I_{SLAVE} is the current per slave. For a total slave count of N_{SLAVES} the total regulator current is simply given by:

$$I_{OUT} = N_{SLAVES} \cdot I_{SLAVE}$$

R2 and R1 are external resistors connected around an amplifier as shown in Figure 3. For best performance, the ratio of R2/R1 should be between 0.5 and 5. The recommended value for R1 is 500Ω.

I_{MAX} is selectable via R_SEL4 as described previously in Tables 1A and 1B. The choice of gain (6 or 13 or 20) is made with R_SEL0 as shown in Table 4.

Example Droop Calculation

Consider a system with 120A, 1.25mΩ load line, with 6 VT1125S slaves and 20A per slave.

1. In order to ensure that there is some tolerance for current ripple, choose I_{MAX} = 24. Based on Table 1A, use R_SEL4 = 340Ω.
2. Note that with 120A and 1.25mΩ load line, the voltage droop at full load is 150mV.

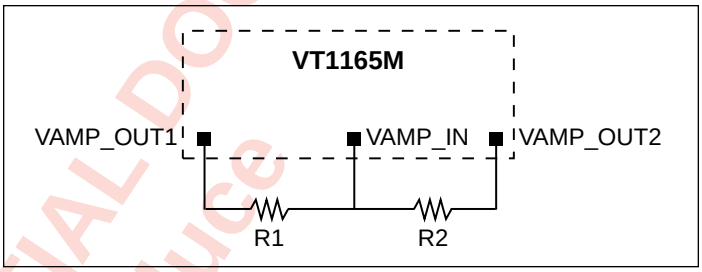


Figure 3. Amplifier Gain Programmability Resistors

Table 4: System Gain and SMBus Address Programming			
R_SEL0 (Ω)	Code	Gain	SMBus Addr[2:0]
340 (GND)	0	20	0
1.02k	1	20	1
1.74k	2	20	2
2.43k	3	20	3
3.09k	4	20	4
3.74k	5	20	5
4.42k	6	20	6
5.11k	7	20	7
5.90k	8	13	0
6.49k	9	13	1
7.15k	10	13	2
7.87k	11	13	3
8.66k	12	13	4
9.31k	13	13	5
10.0k	14	13	6
10.7k	15	13	7
11.3k	16	6	0
12.1k	17	6	1
13.0k	18	6	2
14.0k	19	6	3
15.4k	20	6	4
16.9k	21	6	5
18.7k	22	6	6
20.5k	23	6	7

3. Using the equation above, with V_{DROOP} = 150mV, I_{SLAVE} = 20A, I_{MAX} = 24A, R2/R1 • {6,13,20} = 8.89.
4. Choose gain of 6. Thus R_SEL0 is 11.3kΩ (for SMBus address = 0).
5. The remaining gain is R2/R1 = 1.48. Choose R1 = 500Ω, R2 = 741Ω.

On-the-Fly VID

The VT1165M chipset meets AMD® Opteron™ and Intel® VRM 10.X 'VID on the fly' VID specifications.

Output Enable

The OE pin enables or disables the regulator's output voltage. It should be pulled HIGH using an external pull-up resistor. When forced LOW, the output voltage is disabled.

Power Good

The Power Good (PWRGD) pin provides an open drain output that indicates the status of the output voltage. This pin is externally pulled HIGH using a pull-up resistor of 10kΩ or higher. The signal remains high during normal regulator operation. A low signal indicates an output voltage deviation above or below V_{NOM} for at least 20µs. The deviation threshold is user programmable using R_SEL2 as shown in Table 9.

FAULTB Flags

The FAULTB pin on the master provides an open drain output that indicates a fault condition in the system. This pin should be externally pulled HIGH using a 10kΩ or larger pull-up resistor. During normal operation, the signal on the pin will remain HIGH unless one of the following fault conditions occurs, in which case it will latch in the LOW position:

- R_FREQ resistor is out of range (less than 10kΩ or greater than 300kΩ).
- Master cannot configure itself due to improper R_SEL selection.
- A slave reports an over-temperature event or V_X fault.
- The daisy-chain digital bus connecting the slaves is broken.

For the VT1115S, VT1125S and VT1135S slaves, the slave fault is directly indicated on the slave's FAULTB ball as well. Cycling the 3.3V power supply resets the slave and clears the fault condition.

MASTER-SLAVE DIGITAL INTERFACE

The Smart Slaves™ are configured and monitored via a digital daisy chain interface between the master and all slaves where all devices are connected in a ring. The master controller automatically detects the number of phases present and then sets the phase spacing appropriately. Each slave is assigned its own sequential number via the daisy chain control bus and switches in accordance to its required phase offset to the SPHASE signal. For example, with only two slaves, phase spacing is 180 degrees; with three slaves, spacing is 120 degrees.

Each slave's phase offset and other configuration settings are communicated over the digital bus during startup. Fault conditions are communicated from slave to master during normal operation.

SMBus COMMUNICATION WITH THE VT1165M

The following sections assume basic familiarity with the SMBus interface. Additional background information is available at http://www.smbus.org. The SMBus interface follows the following subset of the SMBus 2.0 specification (appropriate section numbers in parentheses):

- Compliant with 3.3V to 5V ±10% supply levels (2.0)
- SMBus slave support only
- No packet error checking (PEC) (5.4)
- No support for Address Resolution Protocol (5.6)
- Resistor setting allows unique addressing of eight VT1165M devices per bus
- Supports SMBus protocols:
  - Write byte/word (5.5.4)
  - Read byte/word (5.5.5)

The following regulator monitoring information is available over the SMBus interface:

- Average regulator output current
- Peak regulator output current (max average)
- Individual slave junction temperature
- Number of slaves
- Slave status monitoring at the master (VX short, over-temperature, bus break)
- Slave status for each slave (VX short, over-temperature, phase lock, boost voltage, desired current)
- Status of power good signal
- Status of input undervoltage monitor
- Status of input overvoltage monitor
- Status of output overvoltage monitor
- Status of output enable signal
- Status of output overcurrent monitor
- Status of digital bus monitor
- Status of slave configuration
- Status of system clock reference
- VID code settings
- Controller ID number
- Controller revision number
- System RADC programmable settings

The following regulator control capabilities are supported over the SMBus interface:

- Override the VID code settings to program the output voltage
- Override the OE signal to shutdown the regulator

SMBus details, features and programmability are described separately in Volterra Application Note 11.

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Setting the SMBus Address

Addr[2:0] are determined by the resistor value connected to the R_SEL0 pin. Table 4 explains this relationship between resistor value and addr[2:0]. Table 5 shows the bit description for this register.

Table 5: Address Byte for VT1165M

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	addr[2]	addr[1]	addr[0]	R/W

SMBus and Output Voltage Programming in SVID Mode

The relevant SMBus locations are the DAC registers (registers 21d-24d), the override bit (register 25d, bit0) and write_enable (register 29d). Table 6 shows the bit descriptions for these registers. Table 7 shows a typical startup flow.

Table 6: Data Format for Registers 21d-24d

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	800mV	400mV	200mV	100mV	50mV	25mV	12.5mV

NOTE: An auxiliary 450mV DAC leg is forced on in SVID Mode, so the voltage code written to these registers should be 450mV less than the desired output voltage. For example, if 1.1V is desired, then the value that should be written to the DAC register is 1.1V – 0.45V = 0.65V (0011 0100b).

Table 7: Startup Flow

Step	Description	V_{OUT} Value
1	Chip OE low	Disabled
2	OE asserted	V_{START}
3	Write DAC code to registers 21d-24d	V_{START}
4	Read back DAC codes to ensure correct value was written	V_{START}
5	Apply VID[5:4] (V_{OUT_SELECT}) in preparation for writing the override bit (this can be done earlier if desired)	V_{START}
6	Write the User Key (0101 0101b) to register 29d	V_{START}
7	Write 0000 0001b (override) to register 25d	SMBus DAC code selected by VID[5:4]

To prevent accidental writing, register 25d is protected. Each time that it is to be written, the User Key must first be written to write_enable (29d) to unlock the register.

Whenever the system is shut down due to a fault condition or by lowering OE, the override bit will be cleared if SVID Mode is active. This way the system starts regulating to V_{START} and not one of the alternate DAC codes.

Table 8 shows a specific example with the VID pins initially set as follows: VID[1:0] = 10b, VID[3:2] = 11b, VID[5:4] = 10b.

Table 8: SVID Design Example

Action	V_{OUT} Value	Description
Chip OE low	Disabled	System not regulating
Assert OE	1.1V	System enabled – regulates to V_{START}
Write 0010 0000b to register 21d	1.1V	Sets up SMBus voltage 1 to be 850mV (recall that a 450mV DAC leg is forced on, so 400mV + 450mV = 850mV)
Write 0010 1000b to register 22d	1.1V	Sets up SMBus voltage 2 to be 950mV
Write 0011 0000b to register 23d	1.1V	Sets up SMBus voltage 3 to be 1.05V
Write 0101 0000b to register 24d	1.1V	Sets up SMBus voltage 4 to be 1.45V
Read back 21d to 24d	1.1V	Verify correct values were written
Write 0101 0101b to register 29d	1.1V	Unlock User Key
Write 0000 0001b to register 25d	1.05V	Set the override bit; SMBus voltage 3 is selected (because VID[5:4] = 10b)
VID[5:4] = 11	1.45V	SMBus voltage 4 is selected
OE = 0	Disabled	System stops regulating
OE = 1	1.1V	The override bit has been cleared, so the system regulates to V_{START} again
Write 0101 0101b to register 29d	1.1V	Unlock User Key
Write 0000 0001b to register 25d	1.300V	Set the override bit; SMBus voltage registers are not cleared, so again the value is clamped at 1.300V

ADDITIONAL PROGRAMMABLE FEATURES AND SETTINGS

Programmable features for the regulator system are read by the VT1165M at startup. Table 9 shows how the programmable features are related to the R_SEL pins. For calibration, the reference resistor R_{REF} must be 11kΩ with an accuracy of ±0.5%. For setting programmable features, the variable resistors R_SEL[0:6] must be accurate to ±1%. Temperature coefficient mismatch between the reference and variable

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Table 9: Programmable Features	
Feature	**R_SEL[6:0] Pin**
SMBus Address	0
System Gain	0
Setpoint	1
OCP Behavior	1
Power Good Thresholds	2
OVP Threshold	2
VID Select	3
Slave Configuration	4 - 6

resistors must not exceed 100ppm/°C.

R_SEL5 and R_SEL6 are used to program the slaves. A resistor must be connected between these pins and ground. For R_SEL5, a 340Ω resistor should be used. The value for R_SEL6 depends on whether coupled or uncoupled inductors are used. For uncoupled inductor systems use a 340Ω resistor. For coupled inductor systems use a 1.02kΩ resistor.

Programmable Switching Frequency

The per-phase switching frequency of the regulator is programmed by connecting a resistor between the R_FREQ pin and ground. Nominal per phase switching frequencies are selected by choosing an appropriate resistor value as specified in Table 10 or the equation below. Interleaved, multiphase operation results in an effective switching frequency equal to the number of phases times the per-phase switching frequency.

$$F_{SPHASE} = 1/(26 \bullet 10^{-9} + R_{FREQ} \bullet 46 \bullet 10^{-12})$$

Higher switching frequencies enable smaller and faster regulator solutions; lower switching frequencies maximize system efficiency.

Table 10: Nominal Switching Frequency Programmability	
R_{FREQ} (Ω)	**F_{SPHASE} (kHz)**
14.0k	1450
17.8k	1150
22.6k	920
26.1k	800
28.7k	730
36.5k	580

Undervoltage and Overvoltage Programming and Protection

Programming for Power Good and OVP thresholds is via R_SEL2 as shown in Table 11. The master controller provides programmable input and undervoltage and overvoltage protection. Lockout thresholds for the primary 12V input supply are programmed using the VIN_UV and VIN_OV pins as shown in Figure 4.

Table 11: Power Good and Overvoltage Protection Limit Programmability		
R_SEL2 (Ω)	**Power Good (mV) Above or Below V_{NOM}**	**OVP (mV) Above V_{NOM}**
340 (GND)	120	270
1.02k	120	120
1.74k	120	150
2.43k	120	210
3.09k	30	270
3.74k	30	120
4.42k	30	150
5.11k	30	210
5.90k	60	270
6.49k	60	120
7.15k	60	150
7.87k	60	210
8.66k	90	270
9.31k	90	120
10.0k	90	150
10.7k	90	210
11.3k	150	270
12.1k	150	120
13.0k	150	150
14.0k	150	210
15.4k	210	270
16.9k	210	120
18.7k	210	150
20.5k	210	210
23.7k	240	270
27.4k	240	120
31.6k	240	150
39.2k	240	210
49.9k	180	270
69.8k	180	120
118k	180	150
348k (VDD)	180	210

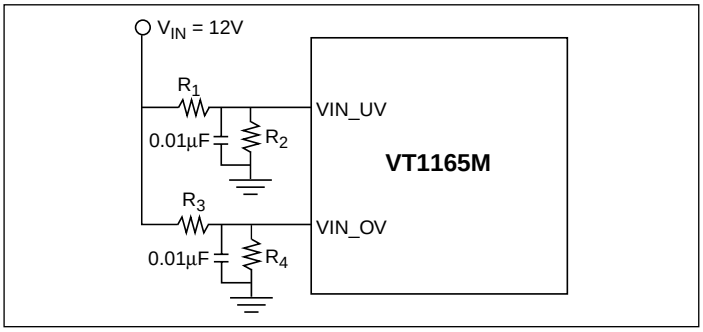

Figure 4. Programming Voltage Lockout Thresholds

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The input undervoltage falling threshold is set using the equation:

$$VIN\_UV_{(FALLING)} = \left(1 + \frac{R_1}{R_2}\right) IN\_UVLO_{FE}$$

The input overvoltage falling threshold is set using the equation:

$$VIN\_OV_{(FALLING)} = \left(1 + \frac{R_3}{R_4}\right) IN\_OVLO_{FE}$$

The input undervoltage rising threshold is set using the equation:

$$VIN\_UV_{(RISING)} = \left(1 + \frac{R_1}{R_2}\right) IN\_ULVO_{RE}$$

The input overvoltage rising threshold is set using the equation:

$$VIN\_OV_{(RISING)} = \left(1 + \frac{R_3}{R_4}\right) IN\_OVLO_{RE}$$

where IN_UVLO and IN_OVLO are defined in the Electrical Characteristics table. Typical values of the two resistors used to program each threshold should sum to approximately 100kΩ. A 0.01µF capacitor should also be used to bypass the VIN_UV and VIN_OV pins.

The master controller also incorporates internal circuitry to monitor the 3.3V input supply through its VDD pin to detect undervoltage conditions.

During startup, the master controller monitors these pin voltages to ensure that both the 3.3V and 12V supplies are valid before initiating its startup sequence. If, at any time, the input supplies violate one of these lockout thresholds, the system turns off. Once the supplies become valid again, the system resumes normal operation.

The master controller includes programmable output overvoltage protection (OVP). Overvoltage events are detected by monitoring the SENSE+ and SENSE- pin voltages. The system enters OVP mode when SENSE+ exceeds V_{NOM} for 20µs by a user-defined amount. Refer to Table 11 for appropriate R_SEL2 values to set the OVP threshold.

Overvoltage protection is incorporated as part of normal system operation. When the output voltage rises above its nominal value, the slaves conduct negative DC current in an effort to lower the output voltage. If the output voltage continues to rise and the programmable overvoltage threshold is reached, the master controller flags this event and the chipset immediately enters a latched shutdown state. The OVP flag can be read through the SMBus (see SMBus Application Note 11 for details). Restarting the regulator then requires either toggling the OE pin or cycling the input power supply.

Overcurrent Protection Mode

When the I_{DES} signal indicates a max current command for more than 5ms, the VT1165M chipset enters one of two available OCP protection modes. The OCP strategy used is programmable and can either force the system to a latched off condition or a hiccup OCP mode. The mode is selected via R_SEL1 (in combination with the regulator setpoint adjustment) as specified in Table 3.

In the hiccup OCP mode, the master controller alternately enables and disables the output voltage with a 10% duty cycle. Initially, the controller attempts to charge the output node for a period of approximately 5ms. If the output voltage has not recovered within this interval, the output is disabled for approximately 45ms and the cycle repeats. Once the output voltage becomes valid, the system self-recovers. The purpose of this hiccup mode is to minimize stresses during fault conditions, such as a short circuit.

Integrated Thermal Protection (Slave)

Each Smart Slave™ includes integrated thermal protection circuitry. When the slave's junction temperature exceeds 155°C, the device enters a latched shutdown state, and a fault condition is reported to the master. This fault flag is indicated by the associated master's FAULTB pin going low and can also be read through the SMBus. For the VT1115S, VT1125S and VT1135S slaves, the slave fault is directly indicated on the slave's FAULTB ball as well. Cycling the 3.3V input power supply resets the slave and clears the fault condition.

MASTER-SLAVE DIGITAL INTERFACE

The Generation 4 slaves are configured and monitored via a digital daisy chain interface between the master and all slaves where all devices are connected in a ring. Digital_Bus_Out (DBO) is the first output from the VT1165M, and is connected to the Digital_Bus_In of the first slave (DBI). The DBO of each slave is then daisy-chain connected to the DBI of each subsequent slave. After all slaves are connected, the ring is terminated back at the DBI of the VT1165M. The master controller automatically detects the number of phases present and then sets the phase spacing appropriately. Each slave is assigned its own sequential number via the daisy chain control bus and switches in accordance to its required phase offset to the SPHASE signal. For example, with only two slaves, phase spacing is 180 degrees; with three slaves, spacing is 120 degrees.

Each slave's phase offset and other configuration settings are communicated over the digital bus during startup. Fault conditions are communicated from slave to master during normal operation.

EXTERNAL COMPONENT SELECTION

Table 12 provides a list of external components required to complete the VT1165M regulation system. More detailed

Table 12: Recommended External Components

Master Components			
Description	**Value**	**Package**	**Quantity**
VDD Capacitor	1µF / 6.3V	0603	1
VNOM Capacitor	6800pF / 6.3V	0603	1
UV/OV Capacitors	0.1µF / 6.3V	0603	2
UV/OV Resistors	Varies	0603	4
R2/R1 Resistors	Varies	0603	2
Configuration Resistor	Varies, 1% tolerance	0603	7
Configuration Reference Resistor	11.0kΩ, 0.5% tolerance	0603	1
Frequency Resistor	Varies, 1% tolerance	0603	1
PWRGD Pull-Up Resistor	10kΩ	0603	1
FAULTB Pull-Up Resistor	10kΩ	0603	1
SC/SD Pull-Up Resistor	10kΩ	0603	2
VID[0:5], OE Resistor	10kΩ	0603	7
Bleed Resistor	100Ω	0603	1
Slave Components			
Description	**Value**	**Package**	**Quantity**
V_{DD} 3.3V Capacitor	1µF / 6.3V / 125°C	0603	1
V_{CC} 3.3V Capacitor	1µF / 6.3V / 125°C	0603	1
Boost Capacitor	1µF / 6.3V / 125°C	0603	1
V_{DDH} HF Capacitor	1µF / 16V / 125°C	0603	3*
V_{DDH} Bulk Capacitor	10µF* / 16V / 125°C	1206	2

***NOTE:** Under review - Volterra may relax these recommendations.

component selection information is provided in the following sections.

Bleed Resistor

A small 100Ω bleed resistor should be connected between the output of the regulator and ground for applications with very low output current loads in shutdown. This pull-down resistor ensures that the output is in a known low-voltage state during shutdown.

Inductor Selection

The output inductor has an important influence on the overall size, cost and efficiency of the voltage regulator. Smaller inductor values usually correspond to larger saturation current ratings, smaller physical sizes, or both. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response.

The current slew rate through the output inductor is given by:

$$\text{Slew Rate} = \frac{dI_L}{dt} = \frac{V_L}{L}$$

where I_L is the inductor current, L is the output inductance, and V_L is the voltage drop across the inductor. This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current "catches up" to the load.

In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current for a single slave is given by the following equation:

$$I_{PP} = \frac{1}{fL}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)V_{OUT}$$

where f is the switching frequency, L is the output inductor value, V_{IN} is the input voltage, and V_{OUT} is the output voltage. From this equation, it is clear that for the same switching frequency, ripple current increases inversely as L decreases. This increased ripple current results in increased AC loss, larger peak current and, for the same output capacitance, results in increased output voltage ripple.

The saturation current rating of the inductor is another important consideration. At steady-state full load, the peak

inductor current is given by:

$$I_{PK} = I_{MAX} + \frac{I_{PP}}{2}$$

where I_{MAX} is the desired, maximum DC load current per slave (see the Output Current Scalability section) and I_{PP} is the peak-to-peak inductor current ripple, defined above. For proper operation of the regulator, it is important that I_{PK} never exceeds the saturation current rating of the inductor, I_{SAT}, during steady-state operation. It is recommended that a margin of at least 20% is included between I_{PK} and I_{SAT}:

$$I_{SAT} > 1.2 \bullet I_{PK}$$

For example, in a 12V to 1.2V application with f = 1MHz and L = 100nH, I_{PP} = 10.8A. With I_{MAX} programmed to 24A, the peak inductor current is I_{PK} = 29.4A, and an inductor with a saturation current rating of at least 36A is recommended. Also note that the saturation current of an inductor is generally smaller at high temperature than at room temperature. It is therefore recommended that the saturation current of the inductor be specified at the maximum case temperature of 125°C.

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss, and AC resistance loss. For the best efficiency, inductors with ferrite core material exhibiting low loss in the range of 0.5MHz to 2MHz, DC winding resistance below 1mΩ, and AC winding resistance below 10mΩ at 2MHz are recommended.

Table 13 and Table 14 provide a summary of recommended inductor suppliers and part numbers. Each inductor meets the electrical requirements of VT1165M applications and has been characterized and guard-banded by Volterra to specify minimum saturation current at 125°C over part-to-part and lot-to-lot variations. In addition, most of these inductors share a common printed circuit board (PCB) footprint, simplifying parts procurement.

The choice of 100nH inductors with per-phase switching frequencies in the range of 700kHz to 1MHz are generally recommended as a good trade-off between efficiency, transient response, current ripple, voltage ripple and overall system size in a typical 12V to low-voltage application with large load steps and transient windows greater than 100mV. For applications with more demanding transient requirements, 70nH or 50nH inductors and switching frequencies above 1MHz are recommended.

Coupled Inductor Selection

The VT1165M chipset has the capability to work with a coupled buck topology, a Volterra proprietary technology (U.S. Patent No. 6,362,986) that utilizes magnetic coupling to achieve cost/performance improvements over a conventional multi-phase buck topology. In particular, the benefit of using the coupled buck topology can be maximized in a multi-phase system where transient response is critical and/or space or cost is constrained.

The industry-standard voltage regulator topology most

Table 13: Inductor Contacts

Company	Phone	Website
Cooper Electronics	(561) 752-5000	www.cooperet.com
ICE Components	(800) 729-2099	www.icecomponents.com
Pulse	(858) 674-8159	www.pulseeng.com
Vitec	(760) 918-8831	www.viteccorp.com

Table 14: Output Inductors

Inductor	Vendor	Part Number	Value (nH)	I_{SAT} (A)	R_{DC} (mΩ)	Footprint (mm)	Height (mm)
100nH	Cooper Electronics	FP4-100	100	44	0.59	10.2 x 6.8	5
	ICE Components	LP02-101-2	100	45	0.43	9.0 x 7.0	5
	Pulse	PA0511.101	120	41	0.55	10.2 x 7.0	5
	Vitec	59P9011	120	41	0.37	10.4 x 7.0	5
70nH	ICE Components	LP02-800-1S	85	44	0.35	7.2 x 6.5	5.2
	Pulse	PA0512.700	72	48	0.45	7.0 x 7.0	5
	Vitec	59P9003	70	45	0.30	7.6 x 7.5	5
50nH	Cooper Electronics	FP2-V050	50	60 [2]	0.46	7.2 x 6.7	5
	ICE	LP02-500-1S	50	60 [2]	0.37	7.2 x 6.5	5.2
	Vitec	59P9002	50	52	0.29	7.6 x 7.5	5

NOTE 3: Inductance drop less than 20% for I_{DC} up to 60A.
NOTE 4: Saturation current (I_{SAT}) and DC winding resistance (R_{DC}) as characterized by Volterra at 125°C.
NOTE 5: I_{SAT} is defined by Volterra as a 20% drop in zero-bias inductance at 125°C.

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often used to deliver high-current low-voltage power is the multi-phase buck converter. The multi-phase implementation distributes the power among several phases and some ripple current cancellation is achieved in the input and output capacitor banks by interleaving the phases. However, for the same value of inductance and switching frequency, the ripple current in the inductors and switches remains the same as that in a single-phase buck converter. Although a smaller-valued inductor would improve the transient response of the converter, it would increase ripple current and decrease system efficiency.

Instead of using discrete inductors, Volterra's coupled buck topology uses proprietary magnetically coupled inductors (U.S. patent pending). The current cancellation in a multi-phase buck converter then can be extended to the inductors and the switches by multi-phase inductor coupling. In comparison to the conventional multi-phase buck, with magnetic coupling, smaller-valued inductors can be used at the same switching frequency without inducing more ripple current. Thus, faster transient response can be achieved without sacrificing converter efficiency.

The coupled inductors that Volterra enabled to work with the VT1165M chipset have an inductance of 50nH per phase, which enhances the transient response by more than 50% compared to a typical 100nH non-coupled system. Thus, in a transient limited system, more than 50% output capacitance can be eliminated to achieve the same performance.

Because of magnetic coupling, the equation used to calculate the ripple current is different in a coupled buck system. By first order estimation (assuming coupling is perfect), the peak-to-peak current ripple for a slave in a coupled buck system is given by the following equation:

$$I_{PP} = \frac{1}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)(V_{OUT})$$

where f is the switching frequency, L is the output inductor value, n is the number of coupled phases, V_{IN} is the input voltage, and V_{OUT} is the output voltage. For example, in a 12V to 1.2V application with n = 5, f = 1MHz and L = 50nH, I_{PP} = 2.4A. In practice, coupling will not be perfect, but "good coupling" can be achieved with careful design of the magnetic. Thus, the real ripple current will be close to what is calculated by this equation.

Table 15 provides a summary of recommended coupled inductor suppliers and their part numbers. Each part meets the electrical requirements of VT1165M applications and has been characterized and guard-banded by Volterra to work at 125ºC over part-to-part and lot-to-lot variations. In addition, most of these coupled inductors share a common PCB footprint, simplifying parts procurement.

The choice of 50nH coupled inductors with per-phase switching frequencies around 800kHz are generally recommended as a good trade-off between efficiency, transient response, current ripple, voltage ripple, and overall system size in a typical 12V to low-voltage application with large load steps. When using coupled inductors, internal slave setting "3" (see Tables 1A and 1B) will provide the optimal transient response.

Output Capacitor Selection

Output capacitance is selected to provide suitable transient tolerance and output voltage ripple. For the best performance, lowest cost, and smallest size of the VT1165M system, multilayer ceramic chip (MLCC) capacitors with 1206 or smaller case sizes, capacitance values of 47µF or smaller, 6.3V or 4V voltage ratings, and X5R or better tem-

Table 15: Coupled Inductors

Vendor	Part Number	Phase Count	Value (nH)	R_{DC} (mΩ)	Footprint (mm)	Height (mm)
Cooper Electronics	CPL-2-50	2	50	0.64	18.5 x 8.5	4.8
	CPL-3-50	3	50	0.64	27.5 x 8.5	4.8
	CPL-4-50	4	50	0.64	36.5 x 8.5	4.8
	CPL-5-50	5	50	0.64	45.5 x 8.5	4.8
	CPL-6-50	6	50	0.64	52.9 x 8.5	4.8
Pulse	PA1312NL	2	50	0.80	18.3 x 8.1	5.2
	PA1313NL	3	50	0.80	27.3 x 8.1	5.2
	PA1314NL	4	50	0.80	36.3 x 8.1	5.2
	PA1315NL	5	50	0.80	45.3 x 8.1	5.2
Vitec	59P9852	2	50	0.76	19 x 8.25	4.75
	59P9853	3	50	0.76	28 x 8.25	4.75
	59P9854	4	50	0.76	37 x 8.25	4.75
	59P9855	5	50	0.76	46 x 8.25	4.75

NOTE 6: DC winding resistance (R_{DC}) is characterized by Volterra at 125°C.

perature characteristics are recommended.

In VT1165M systems with large transient load steps and MLCC output capacitors, it is generally the value of capacitance, rather than the series parasitics of those capacitors, that determines the transient tolerance. An all-MLCC capacitance value of 160µF (per slave) guarantees that the output voltage will not deviate by more than 150mV peak-to-peak for 12.5A/slave unloading and loading transients with 1A/ns load current slew rates and a 120nH inductor (per slave).

If desired, more capacitance can be added at the output to tighten transient tolerance at the expense of increased size, cost and component count. For a given load step magnitude ΔI_{LOAD}, output inductor value L, peak-to-peak ripple current I_{PP}, input voltage V_{IN}, and output voltage V_{OUT}, the transient overshoot and undershoot generally scale inversely with the value of output capacitance, C_{OUT}. For larger load steps with the same tolerance, capacitance should be increased with load step magnitude and peak-to-peak ripple current according to the following relationship:

$$C_{OUT} \propto \left(\Delta I_{LOAD} + \frac{I_{PP}}{2}\right)^2$$

The voltage undershoot associated with a loading transient generally scales inversely with (V_{IN} - V_{OUT}). Similarly, the voltage overshoot associated with an unloading transient scales inversely with V_{OUT}. For the same transient tolerance, C_{OUT} generally scales linearly with L (see the Inductor Selection section).

Output voltage ripple is another important consideration in the selection of output capacitors. For a single-phase buck regulator operating in continuous conduction mode, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL, and 3) the piece wise quadratic waveform that results from charging and discharging the output capacitor:

$$V_{PP} = (ESR)(I_{PP}) + (ESL)\left(\frac{V_{IN}}{L}\right) + \left(\frac{I_{PP}}{8fC_{OUT}}\right)$$

where ESR is the equivalent series resistance at the output, I_{PP} is the peak-to-peak inductor current ripple, ESL is the high-frequency equivalent series inductance at the output, V_{IN} is the input voltage, L is the output inductance, f is the switching frequency, and C_{OUT} is the output capacitance. In a typical VT1165M application with a bank of 1206, X5R, 6.3V, 22µF output capacitors, these three components are roughly equal.

In a multiphase regulation system, however, this equation represents only a worst-case upper bound. The actual output voltage ripple depends on the relative phasing of the individual slaves and the PCB parasitics between the output capacitors. In the worst case (when N slave contributions add constructively), the net I_{PP} and ripple current slew rate are N times larger than for a single slave. However, the parallel combination of the output capacitance of N slaves results in a net C_{OUT} which is N times larger, and net ESR and ESL, which are N times smaller than for a single slave. This leads to an identical expression for the absolute worst-case output voltage ripple of the system. Of course, typical phasing of the slaves dramatically improves this ripple.

The ESL effect of an output capacitor on output voltage ripple cannot be estimated from the resonant frequency, but from the high-frequency (10MHz or above) impedance of that capacitor. The contribution to ESL of a single 1206 22µF output capacitor is between 0.3 and 0.4nH, rather than the 1.2nH usually quoted. PCB traces and vias in the V_{OUT} / GND loop contribute additional parasitic inductance.

The final considerations in the selection of output capacitors are ripple current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst case. Because the recommended output capacitors have extremely low ESR values, they easily satisfy this ripple current requirement. For the triangular AC ripple current at the output, the total RMS current that needs to be handled is calculated as:

$$I_{RMS_{COUT}} = \frac{I_{PP}}{\sqrt{12}}$$

and the total power dissipation in the output capacitors is:

$$P_{COUT} = I^2_{RMS_{COUT}} \cdot ESR$$

where ESR is the equivalent series resistance of the entire output capacitor bank. In a 12V to 1.2V application using a 100nH output inductor and switching at 1MHz, the peak-to-peak ripple current is 10.8A per slave, yielding an RMS ripple current of 3.1A. With eight 22µF output capacitors in the 1206 case size, each capacitor must handle a worst-case RMS ripple current of (3.1/8 = 0.39A). This RMS current level corresponds to a total power dissipation of less than 15mW and surface temperature rise of less than 3°C, and thus falls well within the ripple current rating for the parts. Operation under such conservative conditions extends the lifetime of the capacitors and improves system reliability. Table 16 and Table 17 provide a list of recommended capacitor suppliers and MLCC output capacitors for VT1165M systems. Each capacitor has 1206 or smaller case size, X5R or better temperature rating, 6.3V or 4V voltage rating, and value of 47µF or smaller.

In applications where transient tolerance is more constraining than output voltage ripple, the replacement of some

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Table 16: Capacitor Contacts

Company	Phone	Website
AVX	(843) 448-9411	www.avxcorp.com
Murata	(770) 436-1300	www.murata.co.jp
Panasonic	(714) 373-7334	www.panasonic.com
Taiyo Yuden	(408) 753-4150	www.taiyo-yuden.com
TDK	(847) 803-6100	www.component.tdk.com

Table 17: MLCC Output Capacitors

Case Size	Value (µF)	Temperature Rating	Voltage Rating	t [7] (mm)	Vendor	Part Number
1206	10	X5R	6.3V	1.6	AVX Murata Taiyo Yuden TDK	1206D106MAT2A GRM31CR60J106KA01L JMK316BJ226ML C3216X5R0J106M
1206	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	12064W106MAT2A GRM319C80J106KE19D C3216X6S0G106M
1206	22	X5R	6.3V	1.6	AVX Murata Taiyo Yuden TDK	12066D226MAT2A GRM31CR60J226KE19L JMK316BJ226ML C3216X5R0J226M
1206	22	X6S	4V	1.6	AVX Murata TDK	12064W226MAT2A GRM31CC80G226KE19L C3216X6S0G226M
1206	47	X5R	4V 6.3V	1.6	AVX Murata Taiyo Yuden TDK	12064D476MAT2A GRM31CR60J476ME19L JMK316BJ476ML C3216X5R0J476M
1206	47	X6S	4V	1.6	TDK	C3216X6S0G476M
0805	10	X5R	6.3V	1.25 1.25 0.85 1.25	AVX Murata Taiyo Yuden TDK	08056D106MAT2A GRM21BR60J106KE19L JMK212BJ106MD C2012X5R0J106M
0805	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W106MAT2A GRM21BC80J106KE19L C2012X6S0G106M
0805	22	X5R	6.3V	1.25 1.25 1.25 1.25	AVX Murata Taiyo Yuden TDK	08056D226MAT2A GRM21BR60J226ME39L JMK212BJ226MG C2012X5R0J226M
0805	22	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W226MAT2A GRM21BC80J226ME51L C2012X6S0G226M

NOTE 7: t indicates nominal thickness in mm.

MLCC output capacitors with one or more bulk capacitors may be cost effective. Panasonic's 220µF, 9mΩ, 2V SX series of SP-cap (part number EEFSX0D221R) is recommended for these applications.

Input Capacitor Selection

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. For the best high-frequency noise suppression, three pieces of 0603, 1µF, 16V, 125°C MLCC input capacitors are recommended per slave. Bulk input capacitors are designed to absorb the pulsed DC current that is drawn by the regulator. For the best performance, lowest cost and smallest size of the VT1165M

system, multilayer ceramic chip (MLCC) capacitors with 1210 or smaller case sizes, capacitance values of 22µF or smaller, 16V voltage ratings, and X7R or X7S temperature characteristics are recommended as bulk. The minimum required value of bulk capacitance is strongly influenced by the parasitic inductance in the loop, which includes the +12V supply.

Because they must source the pulsed DC input current of the regulator, the power dissipation and self-heating of the bulk input capacitors are far more important than those for the output capacitors. In a conventional single-phase buck regulator, the magnitude of the RMS input capacitor current can be approximated using the following equation:

$$I_{RMS_{CIN}} = \frac{I_{LOAD}\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{LOAD} is the output DC load current per slave. With an equivalent series resistance of the bulk input capacitor bank, ESR_{CIN}, the total power dissipation in these input capacitors is:

$$P_{CIN} = I^2_{RMS_{CIN}} \cdot ESR_{CIN}$$

For a multiphase system, however, this expression for RMS input current represents only a worst-case upper bound. Typical phasing among slaves reduces the overall ripple current demand on each slave's input capacitors. In practice, the ripple cancellation depends strongly on PCB layout parasitics, operating frequencies, load dynamics, and output to input voltage ratios. So the actual RMS current through each slave's input capacitors lies somewhere between these two extremes.

A conservative approach uses the worst-case upper bound to determine the power dissipation and self-heating of the input capacitors. For a VT1165M system converting 12V to 1.2V with 18A of sustained load current per slave, the worst-case RMS current flowing through each slave's input capacitor bank is equal to 5.4A. If two 10µF input capacitors in 1206 cases are used, the overall ESR is 4mΩ. The power dissipation in the input capacitors is 120mW, yielding nearly 12°C in case temperature rise, which are acceptable numbers for most applications. For better efficiency and increased reliability, the number of input capacitors can be increased to three or more.

The proximity of the input capacitors to the Smart Slaves™ can have an important impact on efficiency and regulation. Please see the PCB Layout section that follows for a description of the best design practices.

Table 18 provides a list of recommended input capacitors for VT1165M systems. Each capacitor has 1210 or smaller case size, 125°C temperature rating, and 16V voltage rating. In some applications, the Smart Slaves™ may require a heatsink. The typical heatsink construction includes an extrusion for the Smart Slaves™ slaves. Capacitors with thickness less than the minimum height of the CSP package are indicated in Table 16. These capacitors are likely to

Table 18: MLCC Input Capacitors

Case Size	Value (µF)	Temperature Rating	Voltage Rating	t [8] (mm)	Vendor	Part Number
0603	1	X7S X7S X7R	6.3V 10V 6.3V	0.8 [9]	AVX Murata TDK	06036Z105KAT GRM188C71A105KA12D C1608X7R0J105K
0603	1	X7S X7R	16V 16V	0.8 [9]	Murata TDK	GRM188C71C105KA12D C1608X7R1C105K
0805	2.2	X7R	25V 16V 16V	1.25 1.25 1.25	Murata TDK AVX	GRM21BR71E225KA73L C2012X7R1C225M 0805YC225MAT
0805	4.7	X7R	16V	1.25	Murata	GRM21BR71C475K
1206	4.7	X7R	16V	1.65	AVX Murata	1206YC475MAT GRM31CR71C475KA01L
1206	10	X7R	16V	1.65	Murata TDK AVX	GRM31CR71C106KAC7L C3216X7R1C106M 1206YC106MAT
1210	10	X7R	16V 25V	2.0 2.5	Murata TDK	GRM32DR71C106KA01L C3225X7R1E106M
1210	22	X7R	16V	2.45 2.5 2.5	AVX Murata TDK	1210YC226MAT GRM32ER71A476K C3225X7R1C226M

NOTE 8: t indicates nominal thickness in mm.

NOTE 9: Indicates capacitors with nominal thickness smaller than the minimum CSP package thickness.

fit within the same extrusion as the CSP package, minimizing the cost and complexity of the heatsink design.

PCB Layout

The printed circuit board layout can dramatically affect the performance of the regulator. A poorly designed board can degrade efficiency, noise performance, and even control loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors and output inductor should be placed in close proximity to each slave IC, while the output capacitors should be lumped together as close to the load as possible. **Input bypass capacitors should be placed on the same PCB side as the CSPs, all referenced to a common ground plane directly beneath. High-frequency capacitors with maximum thickness of 0.95mm or less should be used to clear heatsink restrictions, so that capacitors are as close to the CSPs as possible.** Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance. Traces connecting the input capacitors and internal FETs on each slave IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. The input capacitors should be placed as close to the input supply pins as possible. An uninterrupted ground plane is required immediately underneath these high-frequency current paths, with the ground plane located no more than 5 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

A low impedance ground plane is essential to keep all voltages referenced to a common ground and to minimize stray inductance in all high-frequency loops. Multiple vias are recommended for all paths that carry high currents (i.e., ground, VDD, VX). Vias should be placed close to the chips to create the shortest possible current loops. But it should be insured that via placement does not obstruct the flow of currents or the mirror currents induced in the ground plane.

Careful attention should also be paid to the VX traces to minimize noise coupling into surrounding circuits. These traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but are shielded with a GND plane immediately beneath.

Voltage sense lines should be routed differentially directly from the load points. They should be routed in parallel and in close proximity to each other. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and VT1165M controller IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. Ideally, for system stability, all of the output capacitors should be placed as close as possible to the load.

Gerber files with layout information and complete reference designs can be obtained by contacting a Volterra account representative. Please contact Volterra to obtain CSP layout guidelines for optimal design criteria.

APPLICATION NOTES

Important application notes are available for this product. Volterra recommends that relevant application notes are reviewed prior to starting a design. Application notes for this product are available from the device-specific product page on Volterra's website at http://www.volterra.com, or by contacting a Volterra account representative.

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VID CODE TABLES

Table 19: VRM 9 VID Codes - Programmable Output Voltage Settings (R_SEL3 = 5.90kΩ)

VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)	VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
N/A	0	1	1	1	1	1.475	N/A	1	1	1	1	1	No CPU
N/A	0	1	1	1	0	1.500	N/A	1	1	1	1	0	1.100
N/A	0	1	1	0	1	1.525	N/A	1	1	1	0	1	1.125
N/A	0	1	1	0	0	1.550	N/A	1	1	1	0	0	1.150
N/A	0	1	0	1	1	1.575	N/A	1	1	0	1	1	1.175
N/A	0	1	0	1	0	1.600	N/A	1	1	0	1	0	1.200
N/A	0	1	0	0	1	1.625	N/A	1	1	0	0	1	1.225
N/A	0	1	0	0	0	1.650	N/A	1	1	0	0	0	1.250
N/A	0	0	1	1	1	1.675	N/A	1	0	1	1	1	1.275
N/A	0	0	1	1	0	1.700	N/A	1	0	1	1	0	1.300
N/A	0	0	1	0	1	1.725	N/A	1	0	1	0	1	1.325
N/A	0	0	1	0	0	1.750	N/A	1	0	1	0	0	1.350
N/A	0	0	0	1	1	1.775	N/A	1	0	0	1	1	1.375
N/A	0	0	0	1	0	1.800	N/A	1	0	0	1	0	1.400
N/A	0	0	0	0	1	1.825	N/A	1	0	0	0	1	1.425
N/A	0	0	0	0	0	1.850	N/A	1	0	0	0	0	1.450

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VID CODE TABLES (CONTINUED)

Table 20: VRM 10.X VID Codes - Programmable Output Voltage Settings (R_SEL3 = 0.340kΩ)

VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)	VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
0	0	1	0	1	0	0.8375	0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500	1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625	0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750	1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875	0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000	1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125	0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250	1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375	0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500	1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625	0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750	1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875	0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000	1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125	0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250	1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375	0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500	1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625	0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750	1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875	0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF	1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF	0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000	1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125	0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250	1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375	0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500	1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625	0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750	1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875	0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000	1	0	1	0	1	0	1.6000

VID CODE TABLES (CONTINUED)

Table 21: AMD Opteron™ VID Codes - Programmable Output Voltage Settings (R_SEL3 = 3.09kΩ)

VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
N/A	0	0	0	0	0	1.550
N/A	0	0	0	0	1	1.525
N/A	0	0	0	1	0	1.500
N/A	0	0	0	1	1	1.475
N/A	0	0	1	0	0	1.450
N/A	0	0	1	0	1	1.425
N/A	0	0	1	1	0	1.400
N/A	0	0	1	1	1	1.375
N/A	0	1	0	0	0	1.350
N/A	0	1	0	0	1	1.325
N/A	0	1	0	1	0	1.300
N/A	0	1	0	1	1	1.275
N/A	0	1	1	0	0	1.250
N/A	0	1	1	0	1	1.225
N/A	0	1	1	1	0	1.200
N/A	0	1	1	1	1	1.175
N/A	1	0	0	0	0	1.150
N/A	1	0	0	0	1	1.125
N/A	1	0	0	1	0	1.100
N/A	1	0	0	1	1	1.075
N/A	1	0	1	0	0	1.050
N/A	1	0	1	0	1	1.025
N/A	1	0	1	1	0	1.000
N/A	1	0	1	1	1	0.975
N/A	1	1	0	0	0	0.950
N/A	1	1	0	0	1	0.925
N/A	1	1	0	1	0	0.900
N/A	1	1	0	1	1	0.875
N/A	1	1	1	0	0	0.850
N/A	1	1	1	0	1	0.825
N/A	1	1	1	1	0	0.800
N/A	1	1	1	1	1	Shutdown

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REFERENCE DESIGNS

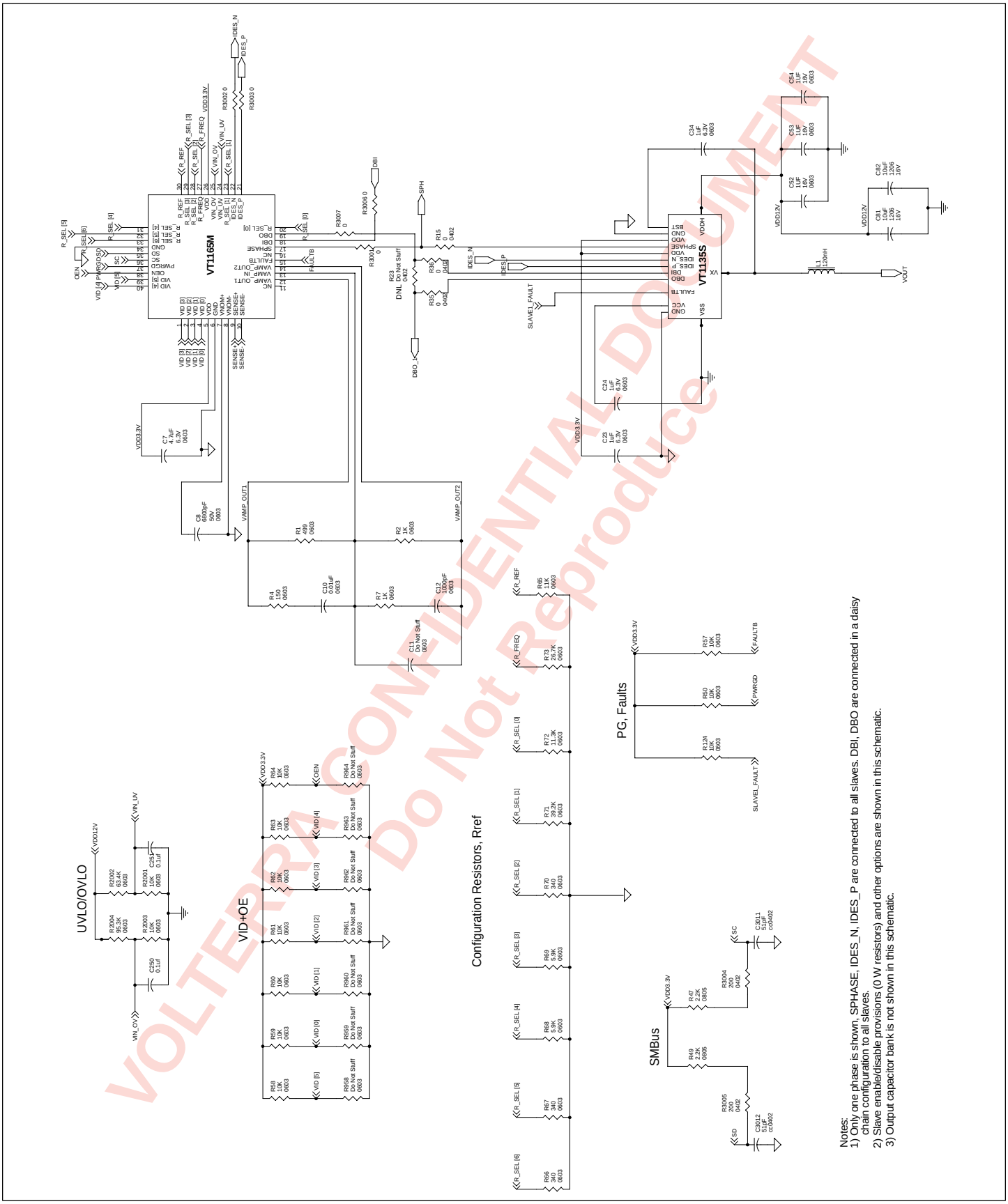

Figure 5. VT1165M/VT1135S Chipset Reference Design Schematic

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

REFERENCE DESIGNS (CONTINUED)

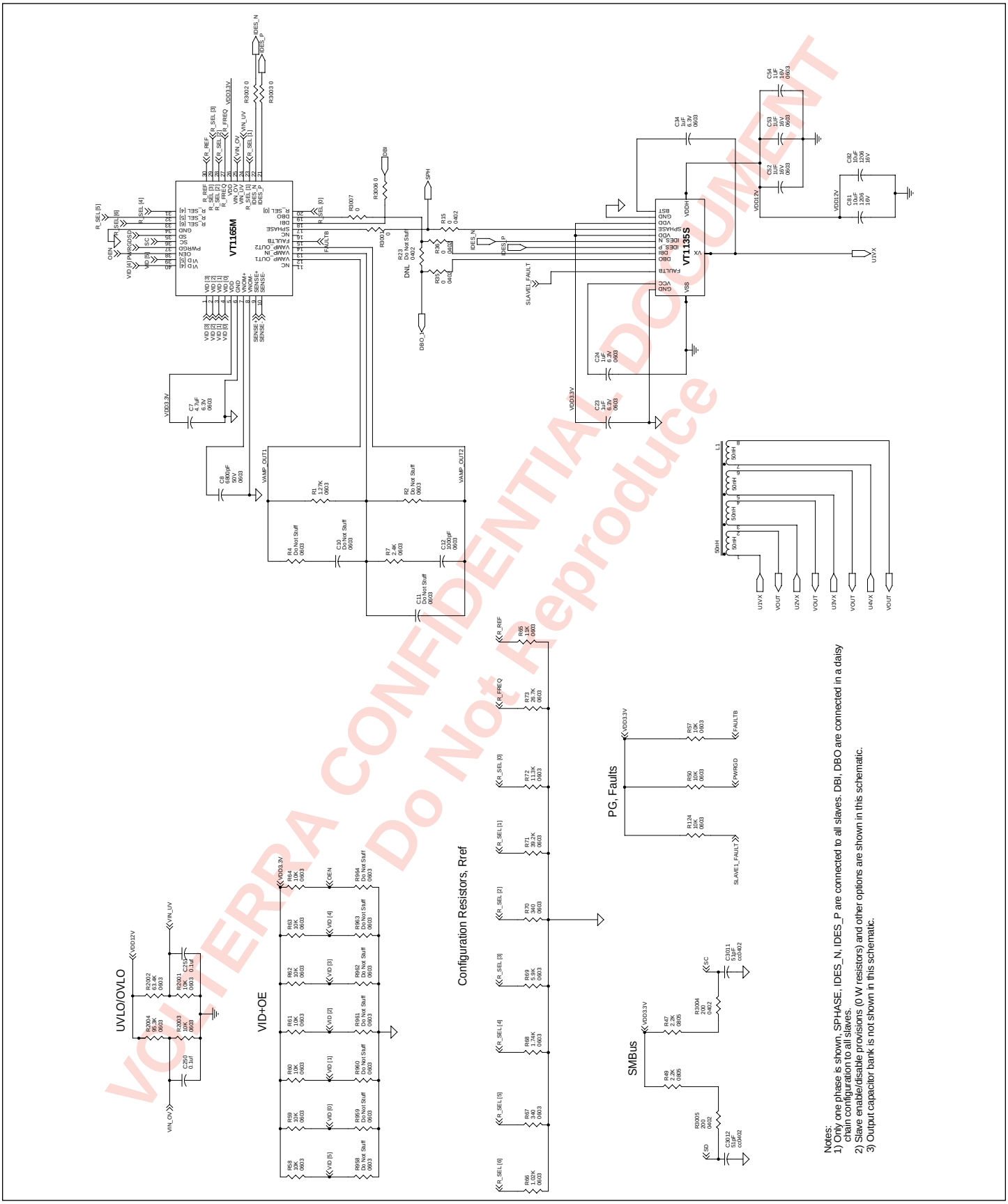

Figure 6. VT1165M/VT1135S Coupled Inductor Chipset Reference Design Schematic

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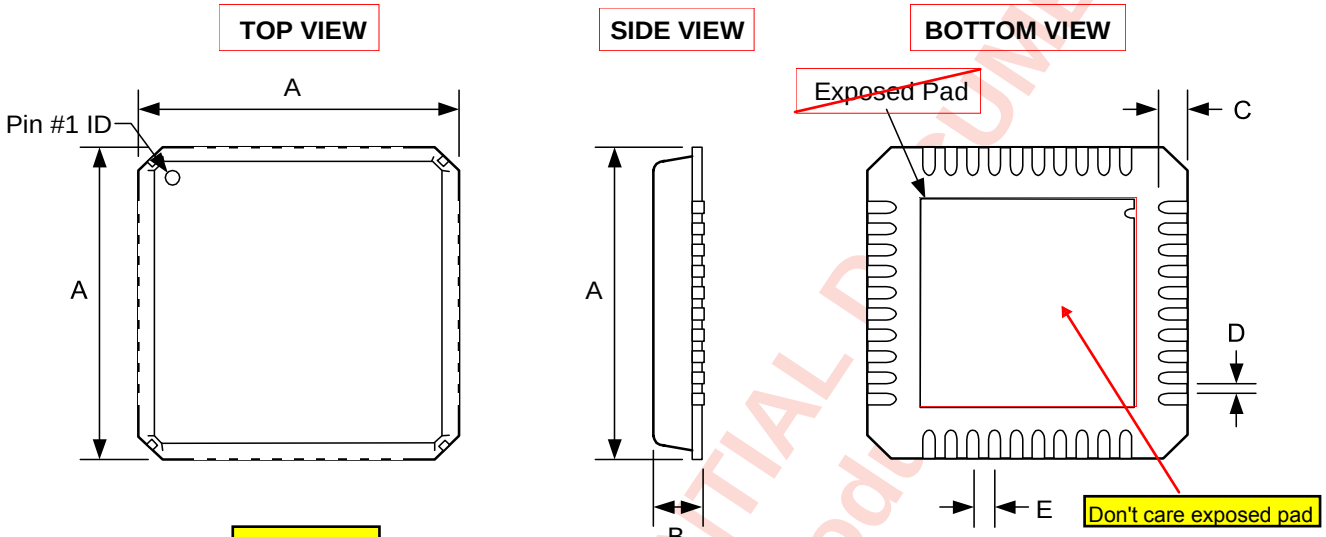
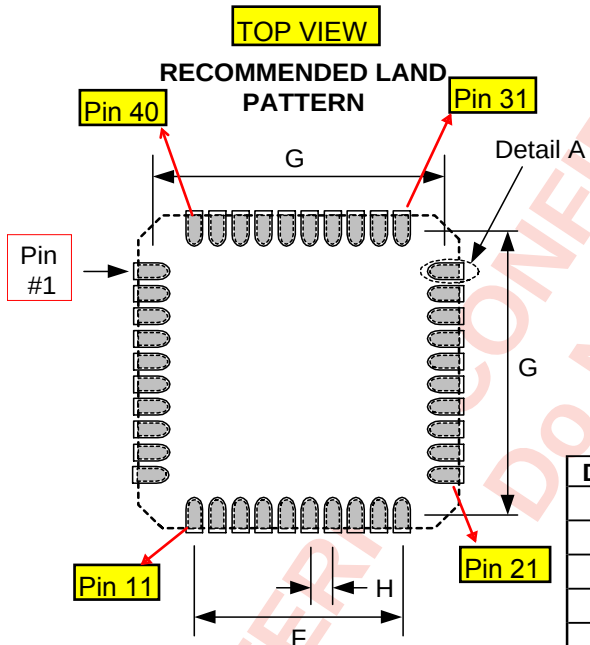
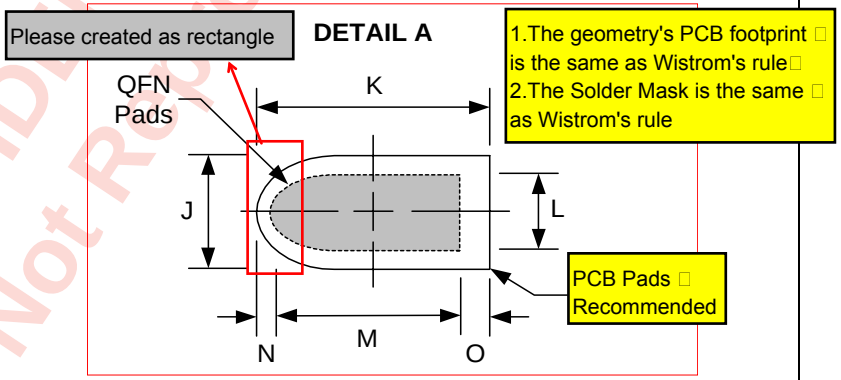
PACKAGE DIMENSIONS - VT1165M

	Title:	Doc No.	Rev.
VOLTERRA	Package Outline - 40 Lead QFN	ES AP-0906	0
		Page 1 of 2	







DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
A	5.9000		6.1000	0.2323		0.2402
B	0.8000		0.9000	0.0315		0.0354
C	0.3000		0.5000	0.0118		0.0197
D	0.1800		0.3000	0.0071		0.0118
E		0.5000			0.0197	
F		4.5000			0.1772	
G		5.6000			0.2205	
H		0.5000			0.0197	
J		0.2800			0.0110	
K		0.6000			0.0236	
L	0.1800		0.3000	0.0071		0.0118
M	0.3000		0.5000	0.0118		0.0197
N	0.0500			0.0020		
O	0.1500			0.0059		

**Inches provided for reference only.*

Notes:
1. Drawings not to scale
2. Controlling dimensions are in millimeters

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

PACKAGE DIMENSIONS - VT1105S

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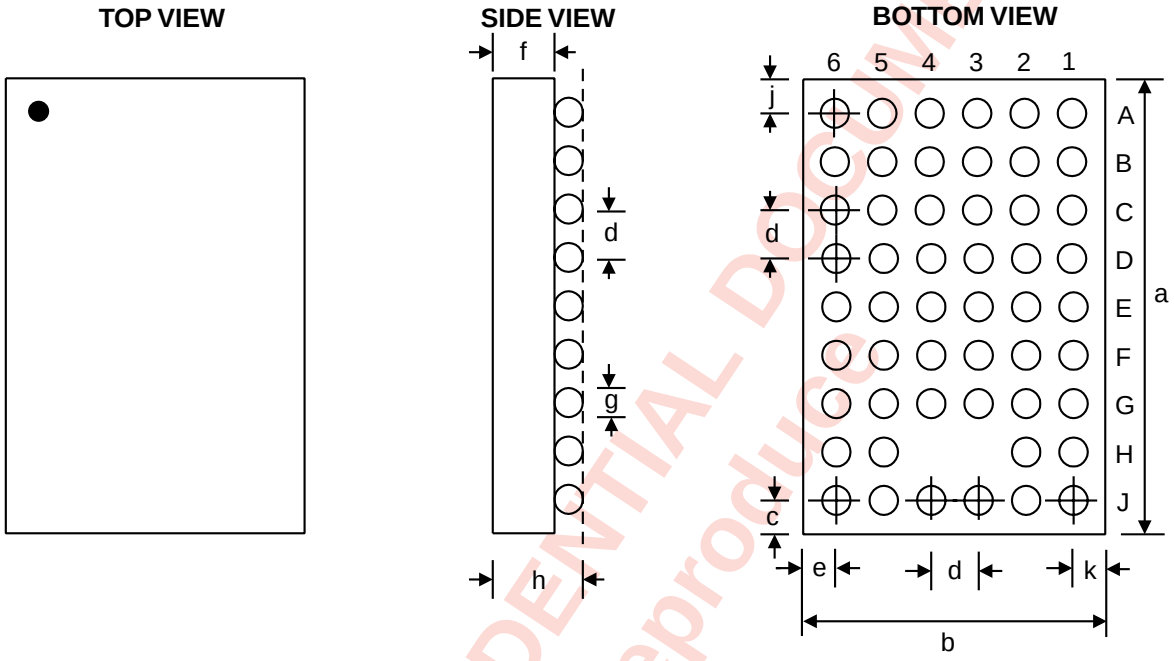
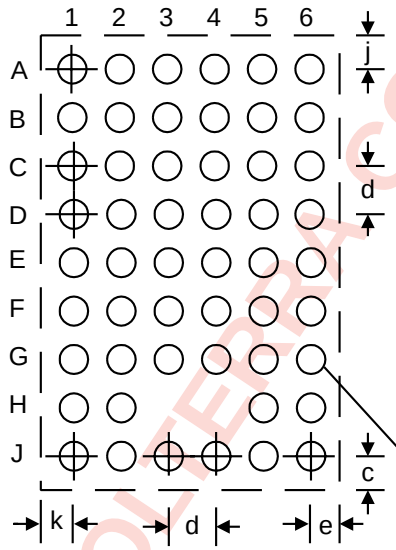
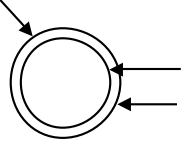
		Page 1 of 2	





DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	5.014		5.064	0.1974		0.1994
b	3.174		3.224	0.1250		0.1269
c		0.453			0.0178	
d		0.500			0.0197	
e		0.341			0.0134	
f	0.635		0.685	0.0250		0.0270
g		0.375			0.0148	
h		0.950			0.0374	
j		0.586			0.0231	
k		0.358			0.0141	

** Inches provided for reference only*



TYPICAL PAD DESIGN
0.280mm ±0.05mm PCB Solder Mask Opening
0.355mm Minimum PCB Pad Diameter

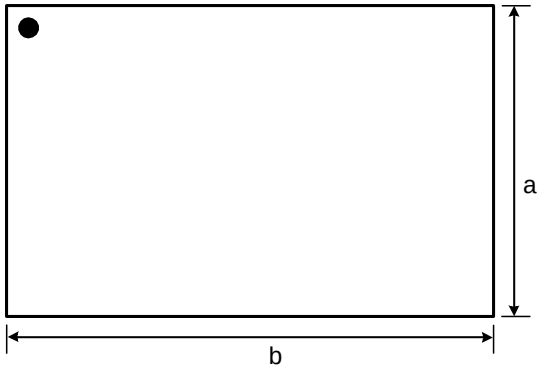
Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

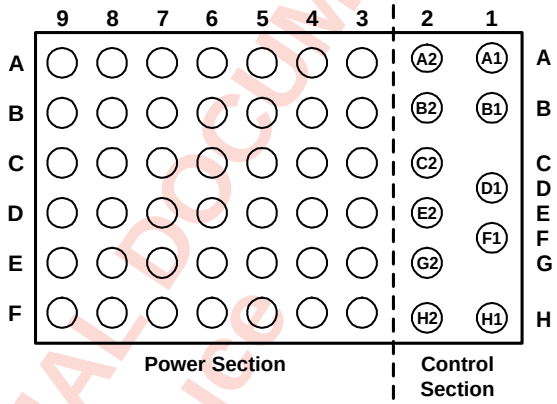
PACKAGE DIMENSIONS - VT1115S

VOLTERRA	Title: Package Outline - 53 Ball CSP VSC1088 / VT1115S	Doc No. ES AP-0794	Rev. 1
		Page 1 of 2	

TOP VIEW

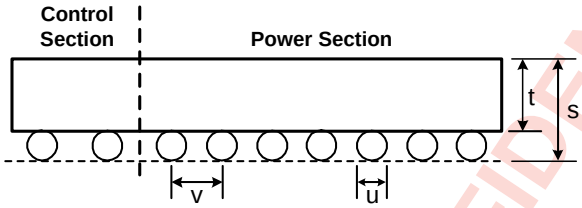


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

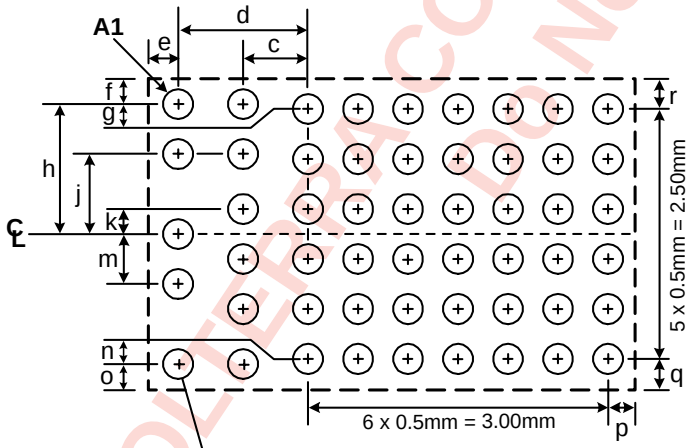
SIDE VIEW



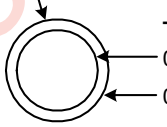
DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	3.173		3.223	0.1249		0.1269
b	5.003		5.053	0.1970		0.1989
c		0.650			0.0256	
d		1.300			0.0512	
e		0.438			0.0172	
f		0.296			0.0117	
g		0.075			0.0030	
h		1.325			0.0522	
j		0.825			0.0325	
k		0.250			0.0098	
m		0.500			0.0197	
n		0.075			0.0030	
o		0.251			0.0099	
p		0.290			0.0114	
q		0.326			0.128	
r		0.371			0.0146	
s		0.930			0.0366	
t		0.650			0.0256	
u		0.375			0.0148	
v		0.500			0.0197	

**Inches provided for reference only.*

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN



0.280 ±0.05mm PCB Solder Mask Opening

0.355mm Minimum PCB Pad Diameter

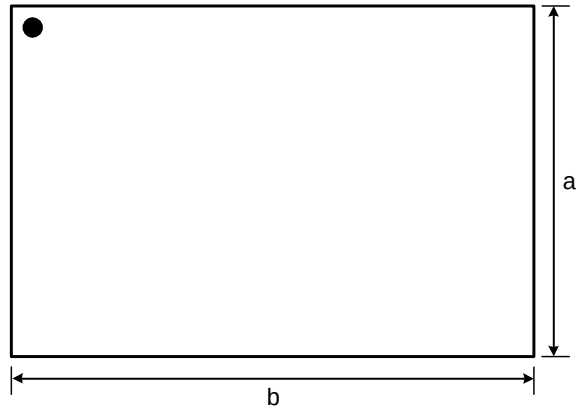
Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

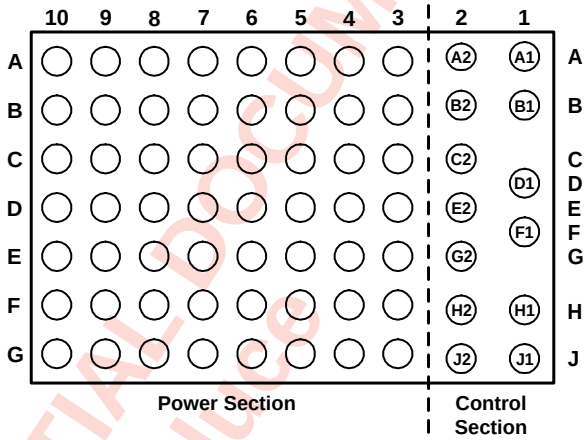
PACKAGE DIMENSIONS - VT1125S

VOLTERRA	Title: Package Outline - 69 Ball CSP VSC1075 / VT1125S	Doc No. ES AP-0760	Rev. 0
		Page 1 of 2	

TOP VIEW

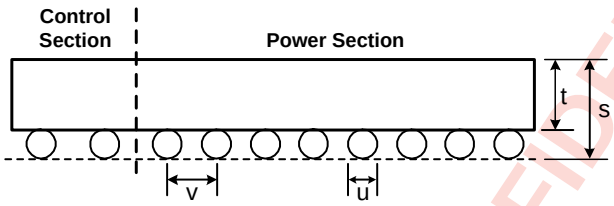


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

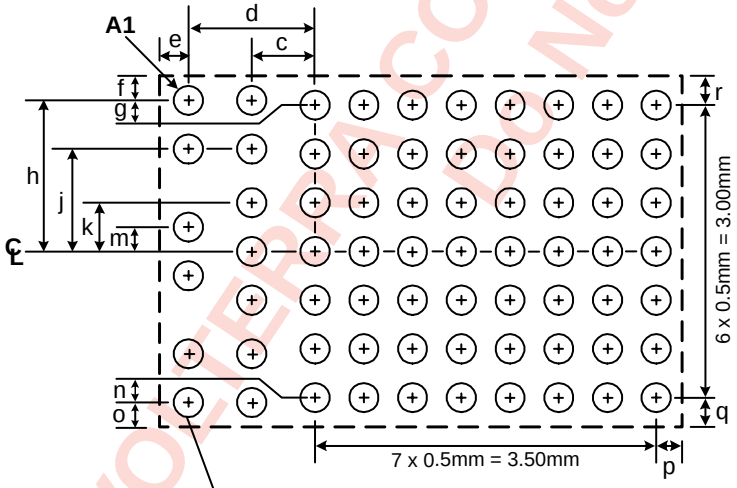
SIDE VIEW



	MILLIMETERS			INCHES*		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
a	3.673		3.723	0.1446		0.1466
b	5.503		5.553	0.2167		0.2186
c		0.650			0.0256	
d		1.300			0.0512	
e	0.413		0.463	0.0163		0.0182
f	0.271		0.321	0.0107		0.0126
g		0.075			0.0030	
h		1.575			0.0620	
j		1.075			0.0423	
k		0.500			0.0197	
m		0.250			0.0098	
n		0.075			0.0030	
o	0.226		0.276	0.0089		0.0109
p	0.265		0.315	0.0104		0.0124
q	0.301		0.351	0.0119		0.0138
r	0.346		0.396	0.0136		0.0156
s		0.930			0.0366	
t		0.650			0.0256	
u		0.375			0.0148	
v		0.500			0.0197	

**Inches provided for reference only.*

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN

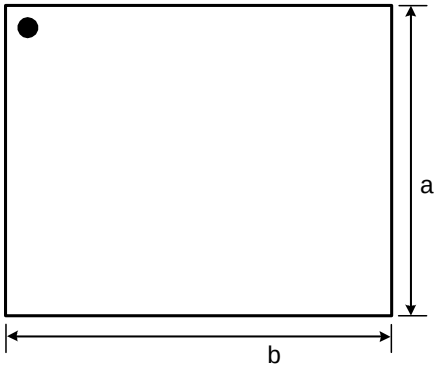
Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

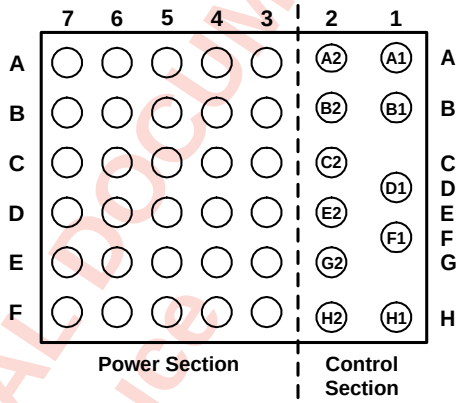
PACKAGE DIMENSIONS - VT1135S

VOLTERRA	Title: Package Outline - 41 Ball CSP VSC1099 / VT1135S	Doc No. ES AP-0804	Rev. 2
		Page 1 of 2	

TOP VIEW

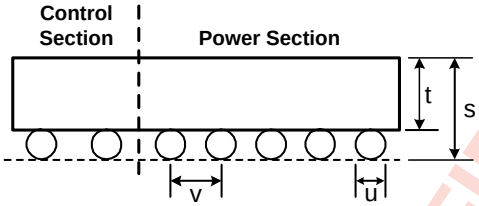


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

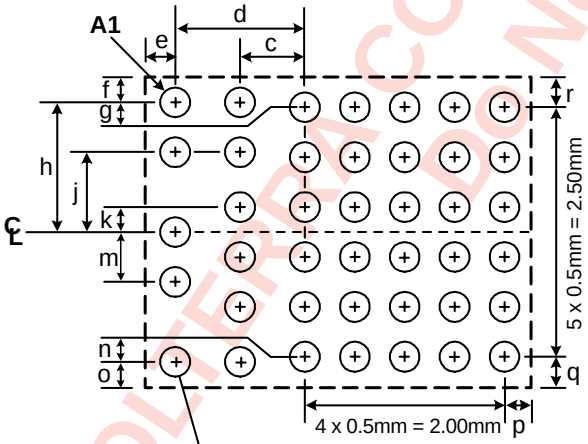
SIDE VIEW



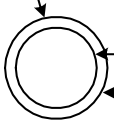
DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	3.213		3.263	0.1265		0.1285
b	3.988		4.038	0.1570		0.1590
c		0.650			0.0256	
d		1.300			0.0512	
e		0.428			0.0168	
f		0.276			0.0109	
g		0.075			0.0030	
h		1.325			0.0522	
j		0.825			0.0325	
k		0.250			0.0098	
m		0.500			0.0197	
n		0.075			0.0030	
o		0.312			0.0123	
p		0.286			0.0112	
q		0.387			0.0152	
r		0.351			0.0138	
s		0.930			0.0366	
t		0.650			0.0256	
u		0.375			0.0148	
v		0.500			0.0197	

**Inches provided for reference only.*

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN



0.280 ±0.05mm PCB Solder Mask Opening

0.355mm Minimum PCB Pad Diameter

Notes
1. Drawing not to scale.
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PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

DATASHEET PHASE DEFINITIONS

PRODUCT PREVIEW: Specifications are to be used as design targets for planning purposes as product is still in development stage.

PRELIMINARY: Specifications are based on limited product and system characterization as product is sampling and has not competed qualification.

NEW PRODUCT: Specifications are based on product and system characterization over all operating conditions as product has passed qualification and released to production.

FINAL: Specifications are based on volume manufacturing data and extensive field data as product has been in production over a year.

WARNING

Volterra products have not been designed, tested, or manufactured for use or resale in applications where the failure, malfunction, or any inaccuracy of the products carries a risk of death or serious bodily injury, including, but not limited to, applications such as use in medical devices (as that term is defined in the Medical Device Amendments Act of 1976), use in nuclear facilities, aircraft navigation or communication, emergency systems, or other applications with a similar degree of potential hazard.

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NOTE

Always check with Volterra Semiconductor Corporation for the latest datasheet before completing a design.

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