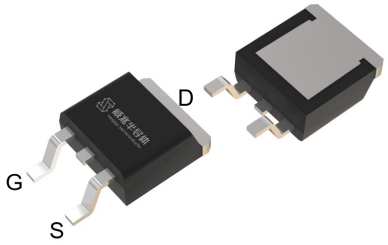
V_{DS}	85	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	4.9	mΩ
I_D	124	A

Features

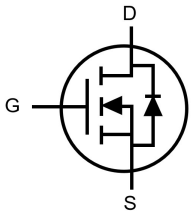
- Enhancement mode
- Very low on-resistance
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested

TO-263



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VSM005NE8HS-G	TO-263	005NE8H	1000pcs/Reel



Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		85	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	124	A
I_D	Continuous drain current @V_{GS}=10V	T_C=25°C	124	A
		T_C=100°C	87	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	496	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	14	A
		T_A=70°C	11	A
EAS	Avalanche energy, single pulsed ②		240	mJ
P_D	Maximum power dissipation	T_C=25°C	150	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	2	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	75	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	85	95	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=85V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)	V_{DS}=85V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=50A	--	4.9	6.1	mΩ
		Tj=100℃	--	6.5	--	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	2770	3695	4915	pF
Coss	Output Capacitance		920	1225	1630	pF
Crss	Reverse Transfer Capacitance		25	35	50	pF
Rg	Gate Resistance	f=1MHz	0.2	1.9	5	Ω
Qg	Total Gate Charge	V_{DS}=40V,I_D=50A, V_{GS}=10V	--	57	76	nC
Qgs	Gate-Source Charge		--	18	24	nC
Qgd	Gate-Drain Charge		--	15	23	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=40V, I_D=50A, R_G=3Ω, V_{GS}=10V	--	18	--	ns
Tr	Turn-on Rise Time		--	84	--	ns
Td(off)	Turn-Off Delay Time		--	41	--	ns
Tf	Turn-Off Fall Time		--	76	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=50A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	I_{sd}=50A, V_{GS}=0V di/dt=100A/μs	--	58	116	ns
Qrr	Reverse Recovery Charge		--	91	182	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.3mH, R_G = 25Ω, I_{AS} = 40A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

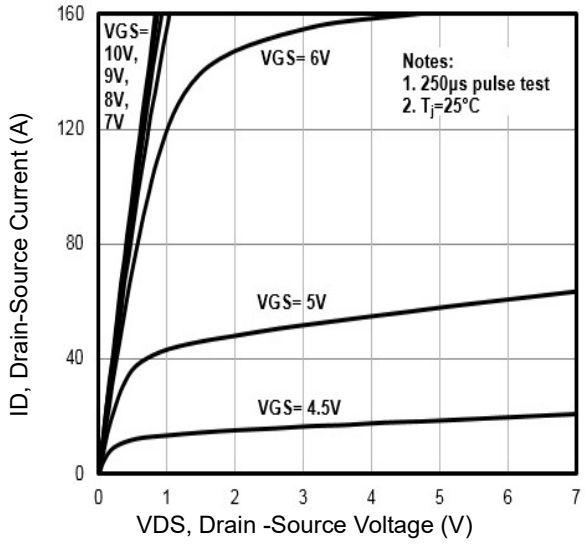


Fig1. Typical Output Characteristics

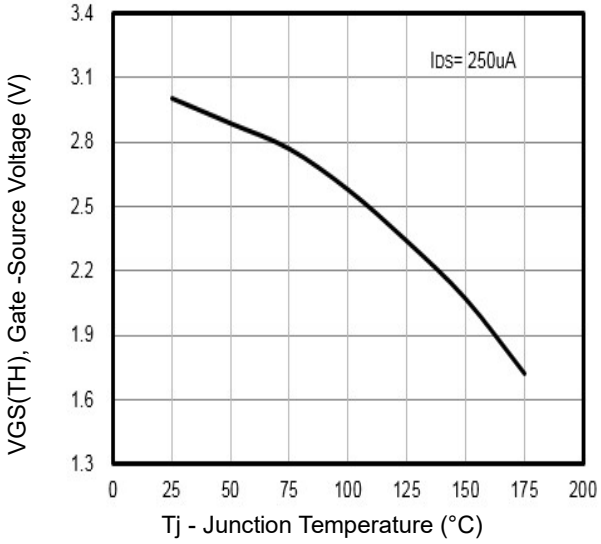


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

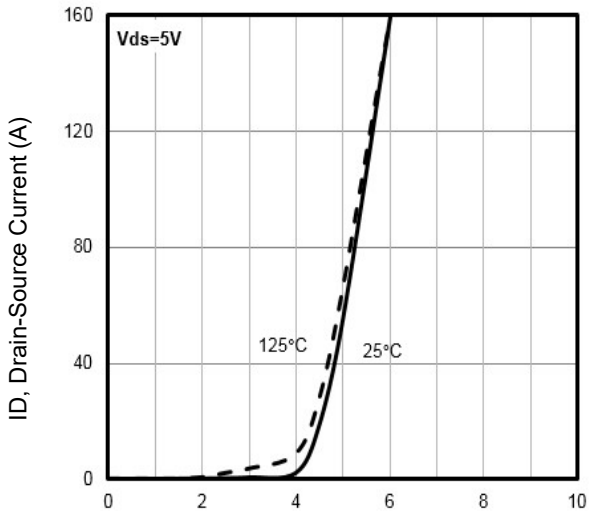


Fig3. Typical Transfer Characteristics

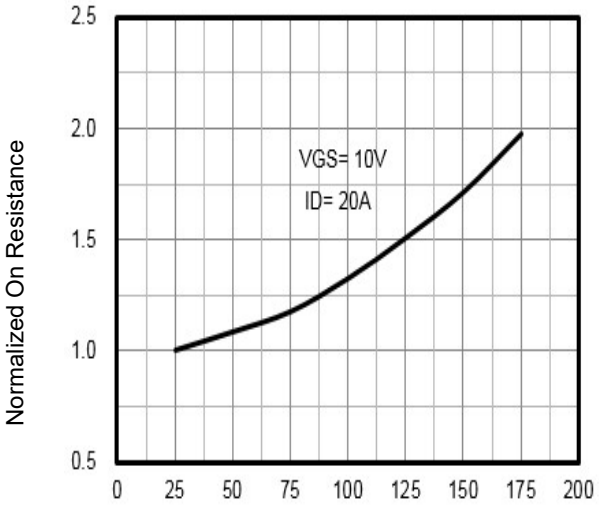


Fig4. Normalized On-Resistance Vs. Temperature

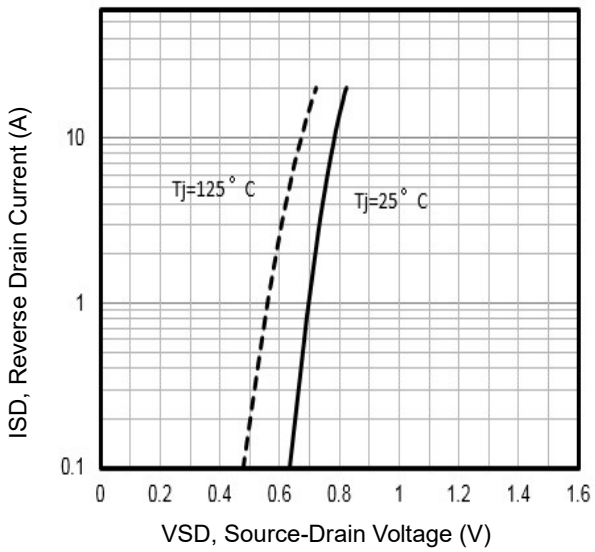


Fig5. Typical Source-Drain Diode Forward Voltage

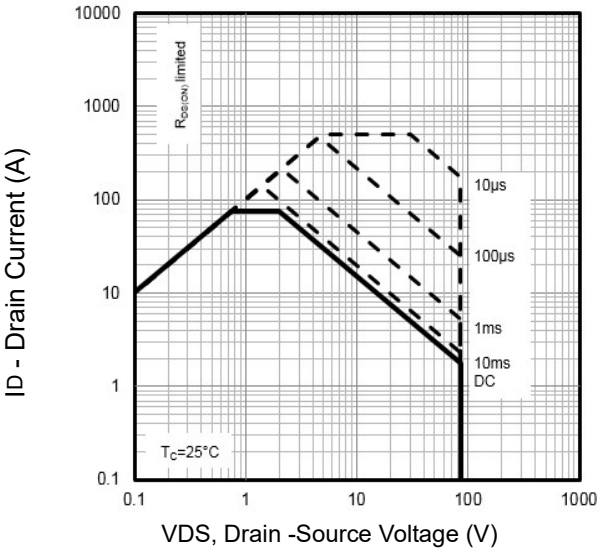


Fig6. Maximum Safe Operating Area

Typical Characteristics

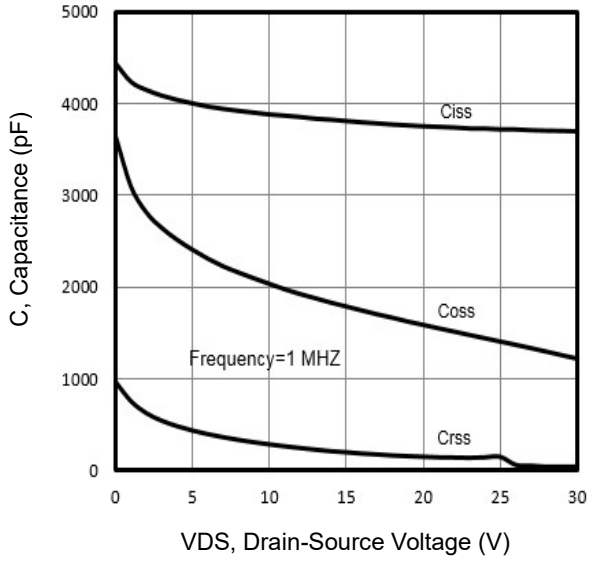


Fig7. Typical Capacitance Vs. Drain-Source Voltage

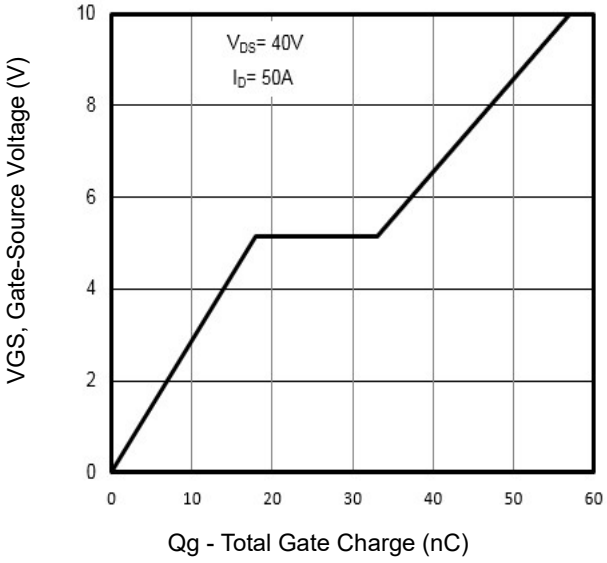


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

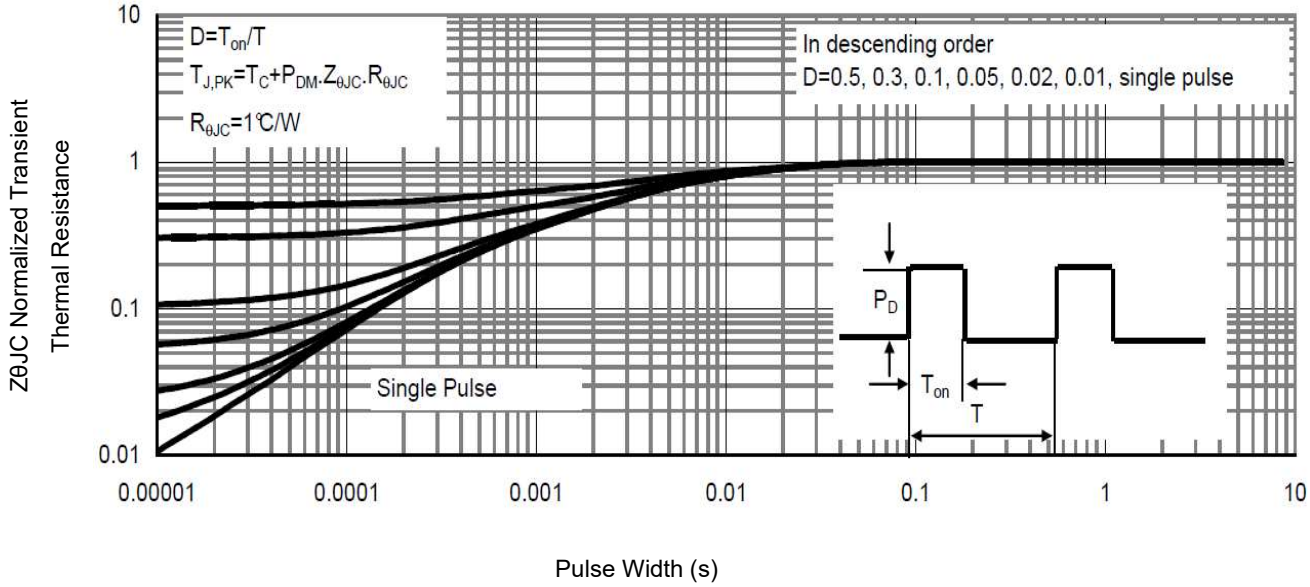


Fig9 . Normalized Maximum Transient Thermal Impedance

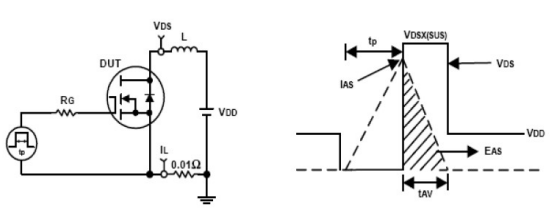


Fig10. Unclamped Inductive Test Circuit and waveforms

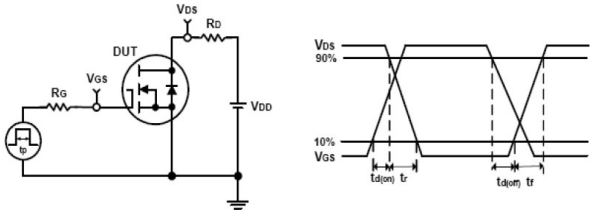
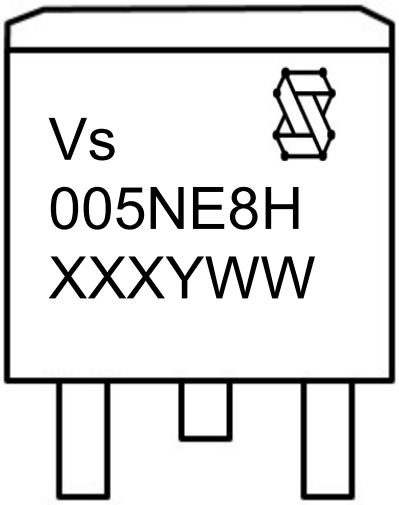


Fig11. Switching Time Test Circuit and waveforms

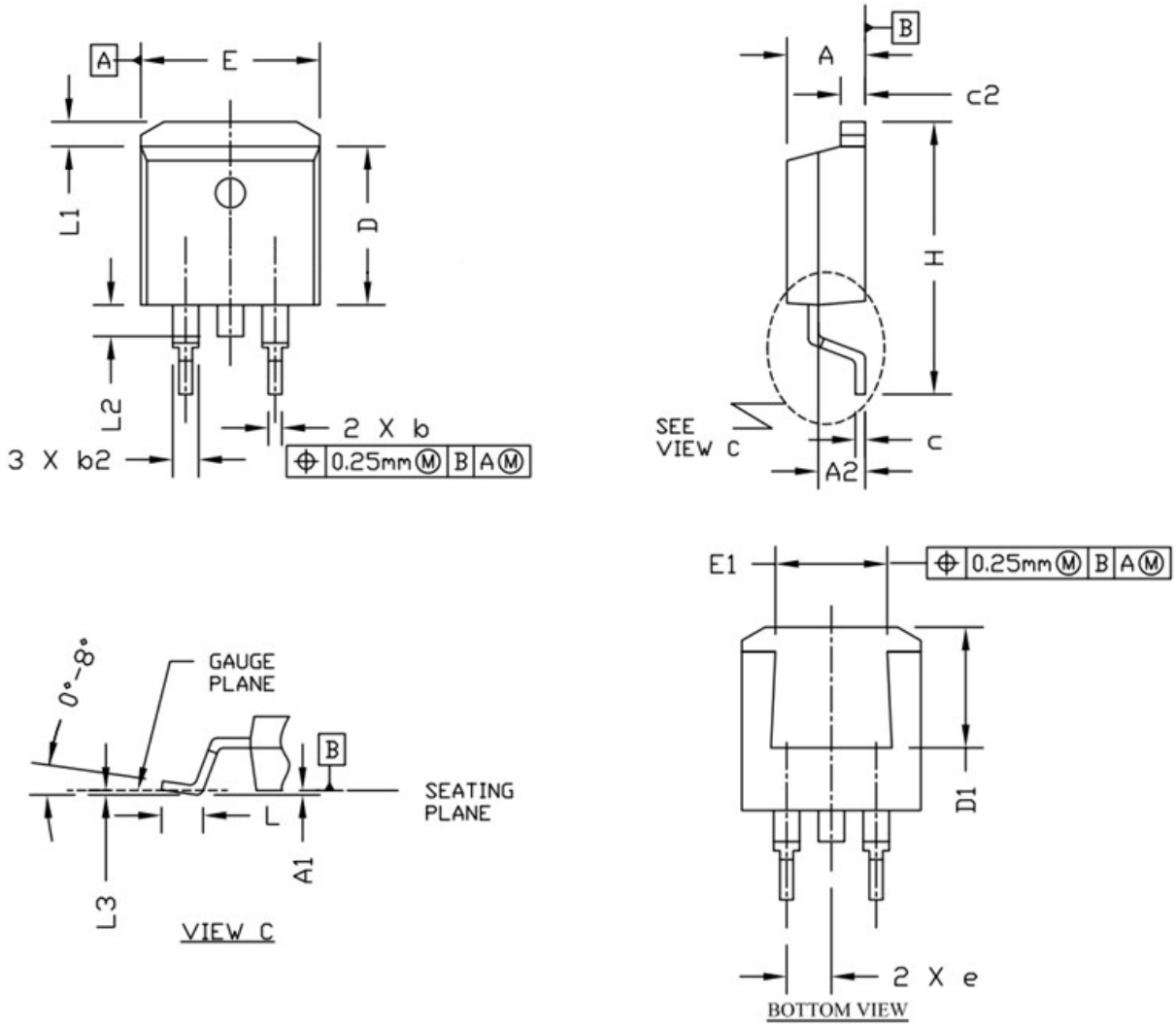
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（005NE8H）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code ， refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.400	4.570	4.700
A1	0.000	0.100	0.200
A2	2.300	2.400	2.500
b	0.700	0.800	0.900
b2	1.200	1.270	1.360
c	0.381	0.500	0.737
c2	1.220	1.300	1.350
D	8.600	9.200	9.300
D1	6.860		
e	2.540 BSC		
E	9.780	9.880	10.260
E1	6.225		
H	14.700	15.100	15.500
L	2.000	2.550	2.750
L1	1.000	1.200	1.400
L2	1.300	1.600	1.700
L3	0.255 BSC		

NNotes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" & "E" do NOT include mold flash, mold flash shall not exceed 0.127mm per side.

Customer Service

Sales and Service:
sales@vgsemi.com

Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: www.vergiga.com