

## Schottky Rectifier, 200 A


**ADD-A-PAK**

### PRODUCT SUMMARY

$I_{F(AV)}$	200 A
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### MECHANICAL DESCRIPTION

The Generation 5 of ADD-A-PAK module combine the excellent thermal performance obtained by the usage of direct bonded copper substrate with superior mechanical ruggedness, thanks to the insertion of a solid copper baseplate at the bottom side of the device.

The Cu baseplate allow an easier mounting on the majority of heatsink with increased tolerance of surface roughness and improved thermal spread.

The Generation 5 of ADD-A-PAK module is manufactured without hard mold, eliminating in this way any possible direct stress on the leads.

The electrical terminals are secured against axial pull-out: they are fixed to the module housing via a click-stop feature already tested and proved as reliable on other Vishay HPP modules.

### FEATURES

- 175 °C  $T_J$  operation
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- UL pending
- Totally lead (Pb)-free, RoHS compliant
- Designed and qualified for industrial level


**RoHS**  
COMPLIANT

### DESCRIPTION

The VSKDS409.. Schottky rectifier doubler module has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS VALUE	ES	UNITS
$I_{F(AV)}$	Rectangular waveform	200	A
$V_{RRM}$		150	V
$I_{FSM}$	$t_p = 5 \mu s$ sine	20 000	A
$V_F$	200 Apk, $T_J = 125^\circ C$	0.79	V
$T_J$	Range	- 55 to 175	°C

### VOLTAGE RATINGS

PARAMETER SY	MBOL	VSKDS409/150P	UNITS
Maximum DC reverse voltage	$V_R$	150	V
Maximum working peak reverse voltage	$V_{RWM}$		

ABSOLUTE MAXIMUM RATINGS				
PARAMETER SYMBOL		TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	50 % duty cycle at $T_C = 94\text{ }^{\circ}\text{C}$ , rectangular waveform	200	A
Maximum peak one cycle non-repetitive surge current	$I_{FSM}$	5 $\mu\text{s}$ sine or 3 $\mu\text{s}$ rect. pulse	20 000	
		10 ms sine or 6 ms rect. pulse	2300	
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_{AS} = 5.5\text{ Amps}$ , $L = 1\text{ mH}$	15	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu\text{s}$ Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical	1A	

ELECTRICAL SPECIFICATIONS						
PARAMETER SYMBOL		TEST CONDITIONS		VALUES	UNITS	
Maximum forward voltage drop	$V_{FM}^{(1)}$	200 A	$T_J = 25\text{ }^{\circ}\text{C}$	0.98	V	
		400 A		1.23		
		200 A	$T_J = 125\text{ }^{\circ}\text{C}$	0.79		1.03
		400 A				
Maximum reverse leakage current	$I_{RM}^{(1)}$	$T_J = 25\text{ }^{\circ}\text{C}$	$V_R = \text{Rated } V_R$	6	mA	
		$T_J = 125\text{ }^{\circ}\text{C}$		85		
Maximum junction capacitance	$C_T$	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^{\circ}\text{C}$		6000	pF	
Typical series inductance	$L_S$	From top of terminal hole to mounting plane		5.0	nH	
Maximum voltage rate of change	dV/dt	Rated $V_R$		10 000	V/μs	
RMS insulation voltage	$V_{INS}$	50 Hz, circuit to base, all terminals shorted (1 s)		3500	V	

**Note**(1) Pulse width < 300  $\mu\text{s}$ , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER SYMBOL			TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T <sub>J</sub> , T <sub>Stg</sub>		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg		R <sub>thJC</sub>	DC operation	0.36	°C/W
Maximum thermal resistance, case to heatsink		R <sub>thCS</sub>	Mounting surface, smooth and greased	0.1	
Approximate weight				110	g
				40	z.
Mounting torque ± 10 %	to heatsink			5	Nm
	busbar			4	
Case style			JEDEC	TO-240AA	

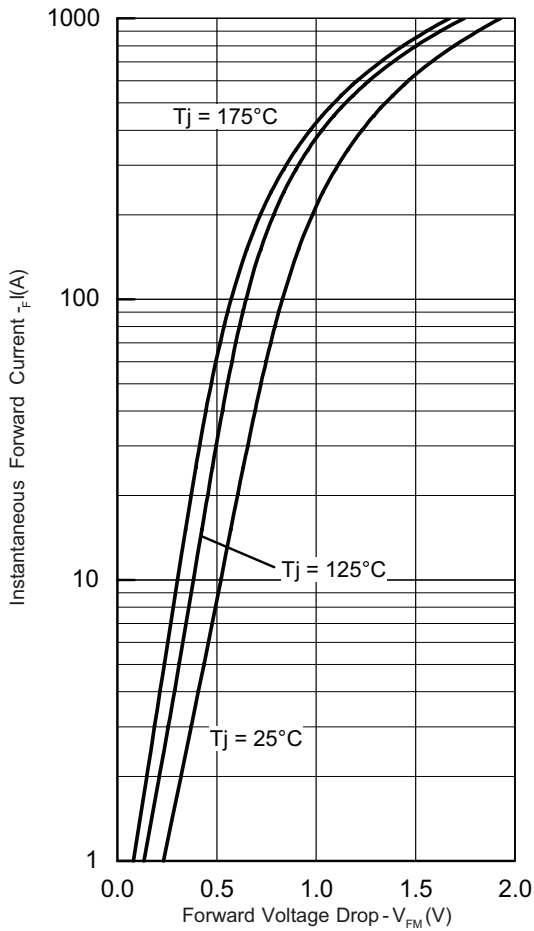


Fig. 1 - Maximum Forward Voltage Drop Characteristics

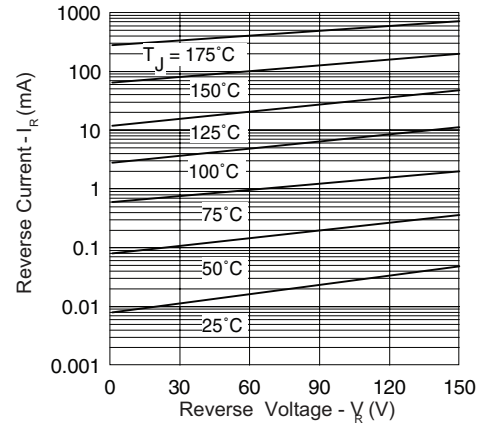


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

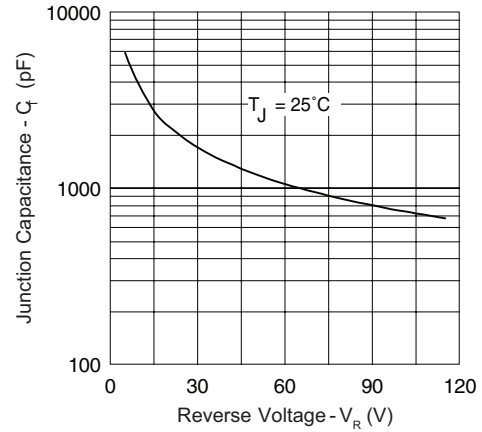
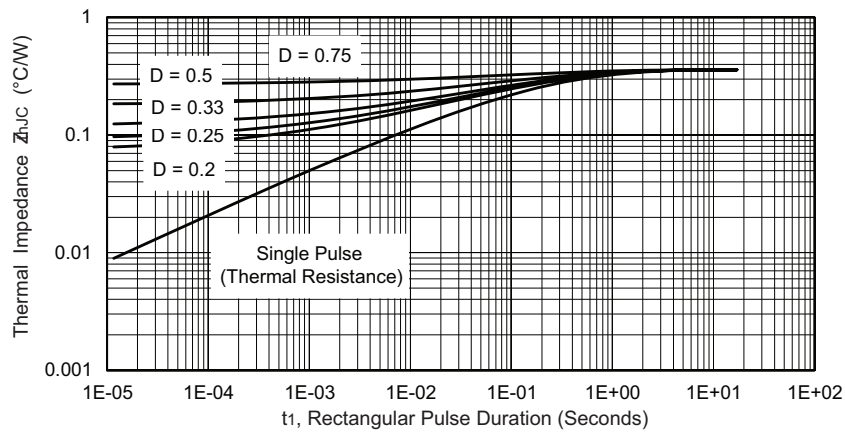


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics

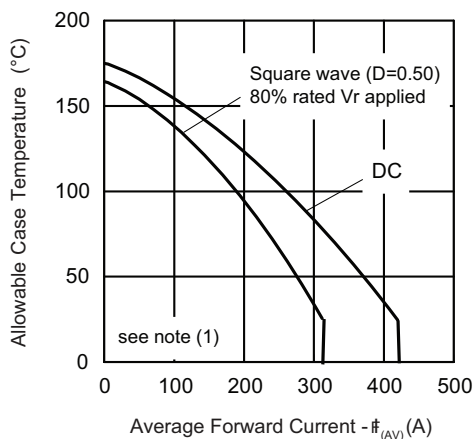


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

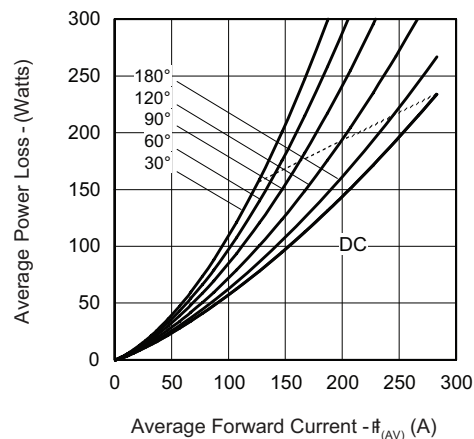


Fig. 6 - Forward Power Loss Characteristics

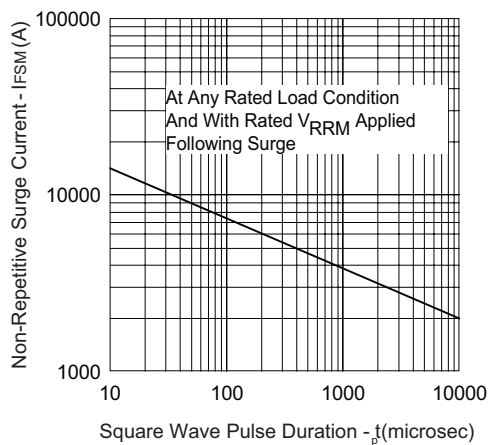


Fig. 7 - Maximum Non-Repetitive Surge Current

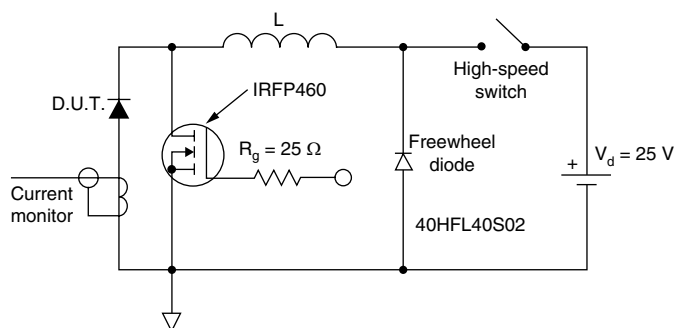


Fig. 8 - Unclamped Inductive Test Circuit

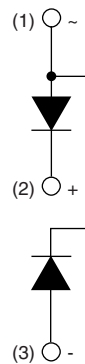
### Note

- (1) Formula used:  $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$ ;  
 $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  
 $P_{dREV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1} = 80\%$  rated  $V_R$

**ORDERING INFORMATION TABLE**

Device code	<b>VS</b>	<b>KD</b>	<b>S</b>	<b>40</b>	<b>9</b>	<b>/</b>	<b>150</b>	<b>P</b>
	①	②	③	④	⑤		⑥	⑦

- 1** - Vishay HPP
- 2** - Circuit configuration:  
KD = ADD-A-PAK - 2 diodes in series
- 3** - S = Schottky diode
- 4** - Average rating (x 10)
- 5** - Product silicon identification
- 6** - Voltage rating (150 = 150 V)
- 7** - Lead (Pb)-free

**CIRCUIT CONFIGURATION****LINKS TO RELATED DOCUMENTS**

Dimensions

<http://www.vishay.com/doc?95174>



### Disclaimer

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