

Vishay High Power Products

Schottky Rectifier, 300 A



ADD-A-PAK

PRODUCT SUMMARY				
I _{F(AV)}	300 A			

MECHANICAL DESCRIPTION

The Gene ration 5 of ADD-A-PAK modul e combine the excellent thermal performance obtained by the usage of direct bond ed copper substrate with superior mechanical ruggedness, than ks to the insertion of a solid copper baseplate at the bottom side of the device.

The Cu baseplate allow an easier mounting on the majority of heatsink with in creased tole rance of surface roughness and improved thermal spread.

The Generation 5 of ADD-A-PAK module is manufactured without hard mold, eliminating in this way any possible direct stress on the leads.

The electrical terminals are secured against axial pull-out: they are fixed to the module housing via a click-stop feature already tested and proved as reliable on other Vishay HPP modules.

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- · High frequency operation
- Guard ring for e nhanced ru ggedness an d lo ng term reliability
- UL pending
- Totally lead (Pb)-free, RoHS compliant
- Designed and qualified for industrial level

DESCRIPTION

The VSKCS303.. Schottky rectifier common cathode h as been optimized for low reverse leakage at high temperature. The proprie tary barrie r te chnology allows for reliable operation up to 150 $^{\circ}$ C junction temperature.

Typical app lications are in high curren t switching pow er supplies, plating power supplies, UPS systems, converters, freewheeling d iodes, we lding, and re verse battery protection.

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS V	ALUES	UNITS	
I _{F(AV)}	Rectangular waveform	300	A	
V _{RRM}		100	V	
I _{FSM}	t _p = 5 μs sine	22 000	A	
V _F	150 Apk, T _J = 125 °C	1.0	V	
TJ	Range	- 55 to 175	°C	

VOLTAGE RATINGS				
PARAMETER SY	MBOL	VSKCS303/100P	UNITS	
Maximum DC reverse voltage	V _R	100	V	
Maximum working peak reverse voltage	V _{RWM}		V	





ABSOLUTE MAXIMUM RATINGS						
PARAMETER SYMBO		L	TEST CONDITIONS		VALUES	UNITS
Maximum average	per module	I	50 % duty cycle at T _C = 96 °C, rectangular waveform		300	
forward current	per leg	I _{F(AV)}			150	
Maximum peak one cycle		5 μs sine or 3 μs rect. pulse	Following any rated load condition and with	22 000	A	
non-repetitive surge current		IFSM		rated V_{RRM} applied	2500	
Non-repetitive avalanche energ	IУ	E _{AS}	$T_J = 25 \text{ °C}, I_{AS} = 5.5 \text{ Amps}, L = 1 \text{ mH}$ 15		15	mJ
Repetitive avalanche current		I _{AR}	$\begin{tabular}{ c c c c c } \hline Current decaying linearly to zero in 1 \mbox{μs} \\ \hline Frequency limited by T_J maximum V_A = 1.5 x V_R typical $$1A$ \end{tabular}$			

ELECTRICAL SPECIFICATIONS					
PARAMETER SYMBOL		TEST CONDITIONS VALUES		UNITS	
Maximum forward voltage drop		150 A	T _J = 25 °C	0.95	V
	V _{EM} ⁽¹⁾	300 A		1.28	
	V FM (*)	150 A	- T _J = 125 °C	1.0	
		300 A		1.06	
Maximum reverse leakage current	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	4.5	mA
	'RM \''	T _J = 125 °C		60	
Maximum junction capacitance	CT	$V_{\rm R}$ = 5 $V_{\rm DC}$ (test signal range 100 kHz to 1 MHz) 25 °C		4150	pF
Typical series inductance	L _S	From top of terminal hole to mounting plane		7.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
RMS insulation voltage	V _{INS}	50 Hz, circuit to base, all terminals shorted (1 s) 3500		V	

Note

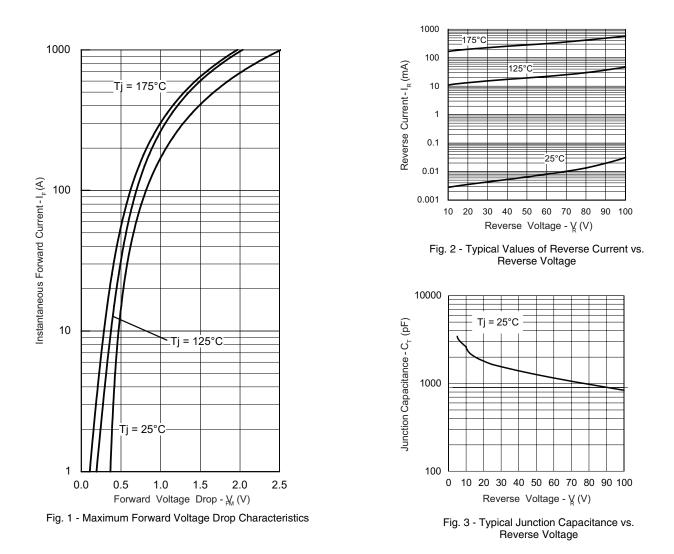
⁽¹⁾ Pulse width < 500 μ s

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER SYMBOL			TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T _J , T _{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg		R _{thJC} D	C operation	0.45	°C/W
Maximum thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.1	0/10
Approximate weight				110	g
			40	Z.	
	to heatsink			5	Nm
Mounting torque ± 10 %	busbar			4	INITI
Case style			JEDEC	TO-2	40AA



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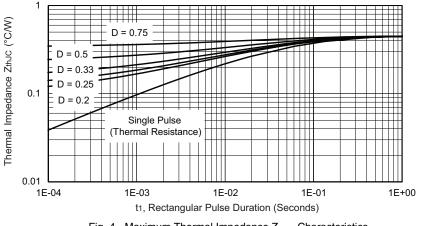
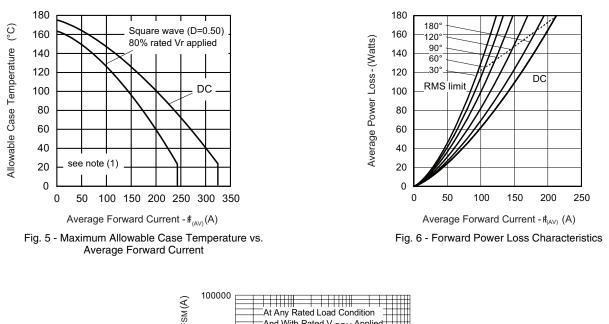


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

VSKCS303/100P

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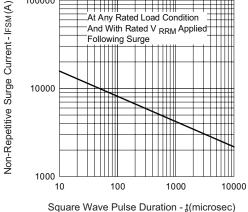


Fig. 7 - Maximum Non-Repetitive Surge Current

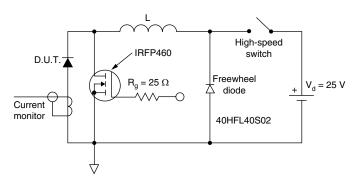


Fig. 8 - Unclamped Inductive Test Circuit

Note

 $\begin{array}{l} \mathsf{Pd} = \mathsf{Forward} \ \mathsf{power} \ \mathsf{loss} = \mathsf{I}_{\mathsf{F}(\mathsf{AV})} \ x \ \mathsf{V}_{\mathsf{FM}} \ \mathsf{at} \ (\mathsf{I}_{\mathsf{F}(\mathsf{AV})}/\mathsf{D}) \ (\mathsf{see fig. 6}); \\ \mathsf{Pd}_{\mathsf{REV}} = \mathsf{Inverse} \ \mathsf{power} \ \mathsf{loss} = \mathsf{V}_{\mathsf{R1}} \ x \ \mathsf{I}_{\mathsf{R}} \ (\mathsf{1} - \mathsf{D}); \ \mathsf{I}_{\mathsf{R}} \ \mathsf{at} \ \mathsf{V}_{\mathsf{R1}} = \mathsf{80} \ \% \ \mathsf{rated} \ \mathsf{V}_{\mathsf{R}} \end{array}$

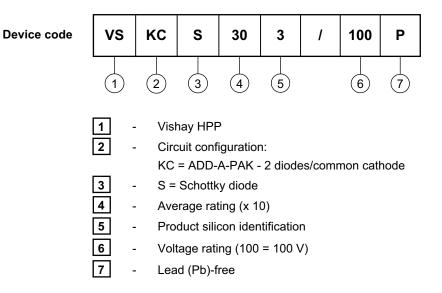
⁽¹⁾ Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;



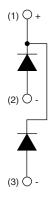
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ORDERING INFORMATION TABLE



CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS				
Dimensions	http://www.vishay.com/doc?95174			



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