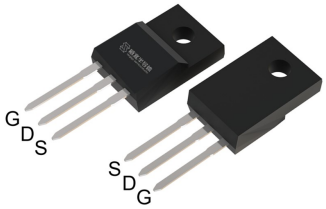
V_{DS}	800	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	240	mΩ
I_D	11	A

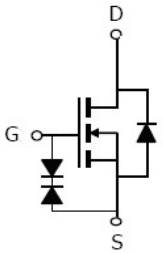
Features

- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=10 V
- Super Junction Technology
- 100% Avalanche test,100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-220F



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSF270N80HS	TO-220F	270N80H	50pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		800	V
V_{GS}	Gate-Source voltage		±30	V
I_S	Diode continuous forward current	T_C = 25°C	11	A
I_D	Continuous drain current @VGS=10V	T_C = 25°C	11	A
I_D	Continuous drain current @VGS=10V	T_C = 100°C	7	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	40	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	1.8	A
		T_A = 70°C	1.5	A
EAS	Avalanche energy, single pulsed ②		845	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	89	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	2.5	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	1.2	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	42	50	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	800	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=800V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)⑦	V_{DS}=640,V_{GS}=0V	--	--	50	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±30V,V_{DS}=0V	--	--	±5	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	3.4	3.9	4.4	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=9A	--	240	290	mΩ
		T_j=100℃ ⑦	--	422	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=400V,V_{GS}=0V, f=1MHz	--	1920	--	pF
Coss	Output Capacitance ⑦		--	40	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	2	--	pF
Rg	Gate Resistance	f=1MHz	--	2.1	--	Ω
Qg	Total Gate Charge ⑦	V_{DS}=400V,I_D=9A, V_{GS}=10V	--	30	--	nC
Qgs	Gate-Source Charge ⑦		--	12	--	nC
Qgd	Gate-Drain Charge ⑦		--	6.6	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=400V, I_D=9A, R_G=10Ω, V_{GS}=10V	--	20	--	ns
Tr	Turn-on Rise Time		--	16	--	ns
Td(off)	Turn-Off Delay Time		--	42	--	ns
Tf	Turn-Off Fall Time		--	21	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=18A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time ⑦	I_{sd}=9A, V_{GS}=0V di/dt=100A/μs	--	355	--	ns
Qrr	Reverse Recovery Charge ⑦		--	4.4	--	uC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② EAS of 845mJ is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 13A, V_{GS} =10V；100% FT tested at L = 10mH, I_{AS} = 6.5A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad).

⑥ The value of RθJA is measured with the device in a still air environment with TA =25° C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

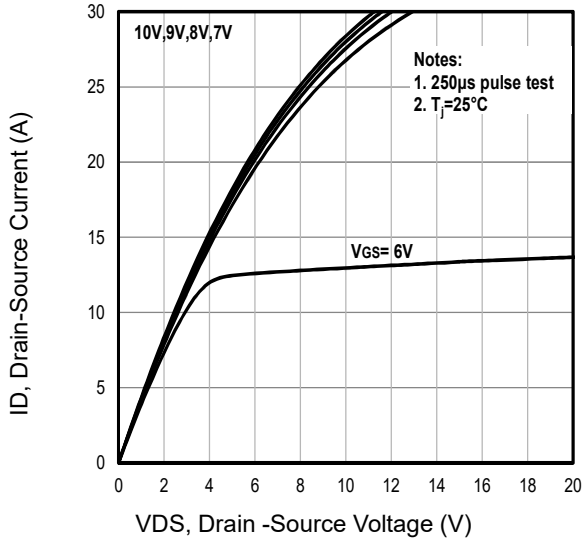


Fig1. Typical Output Characteristics

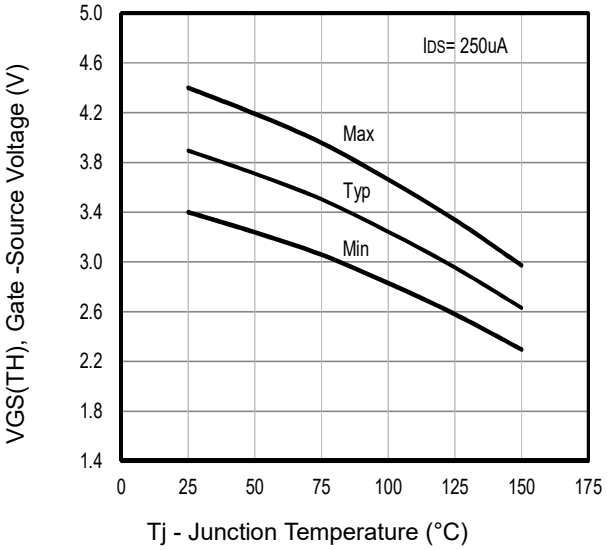


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

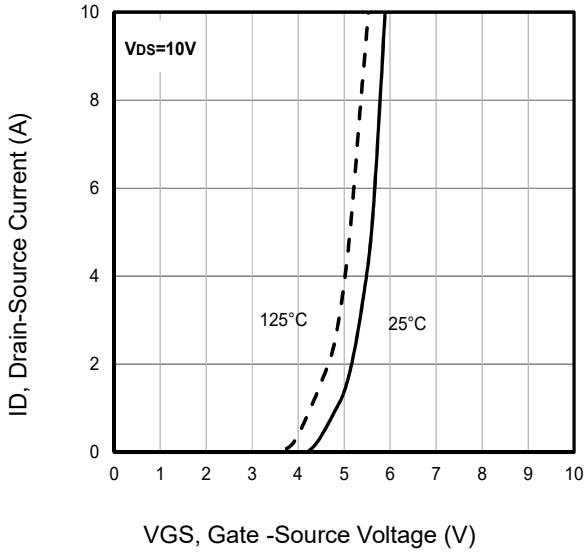


Fig3. Typical Transfer Characteristics

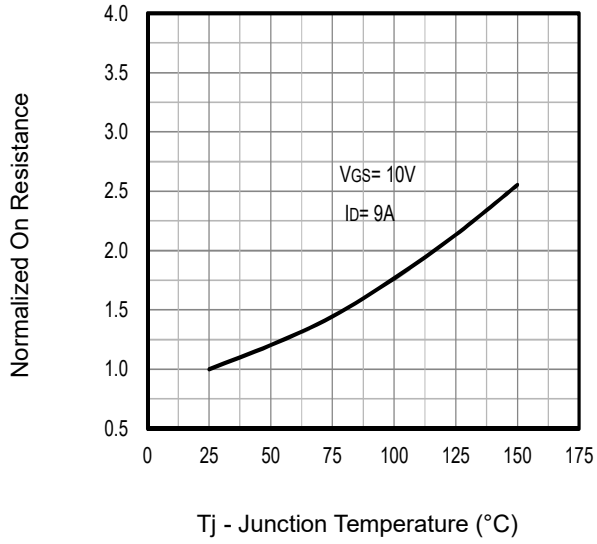


Fig4. Typical Normalized On-Resistance Vs. Tj

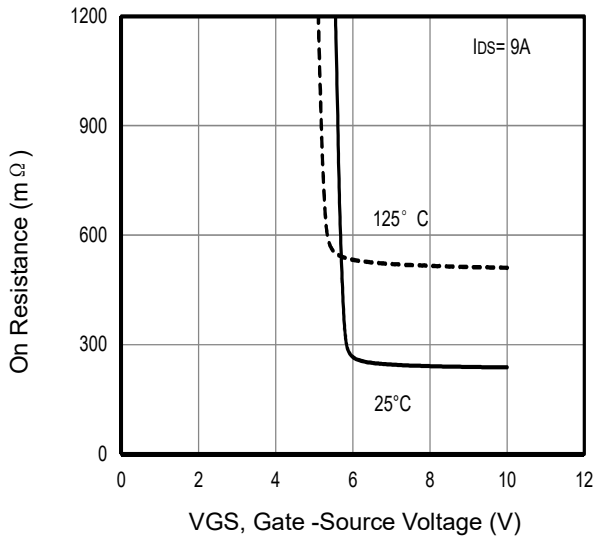


Fig5. Typical On Resistance Vs Gate -Source Voltage

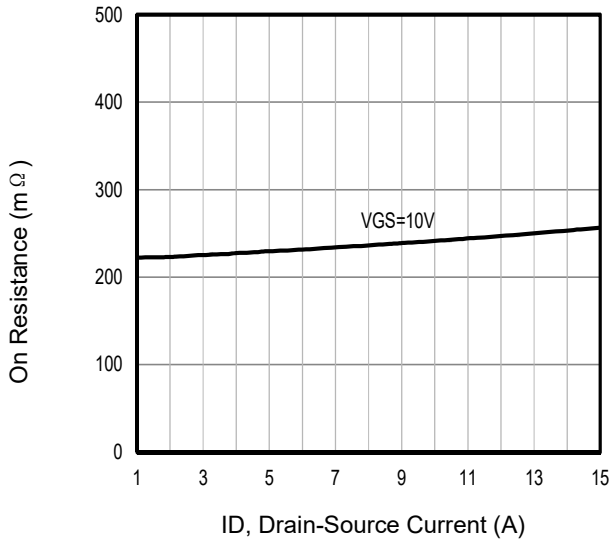


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

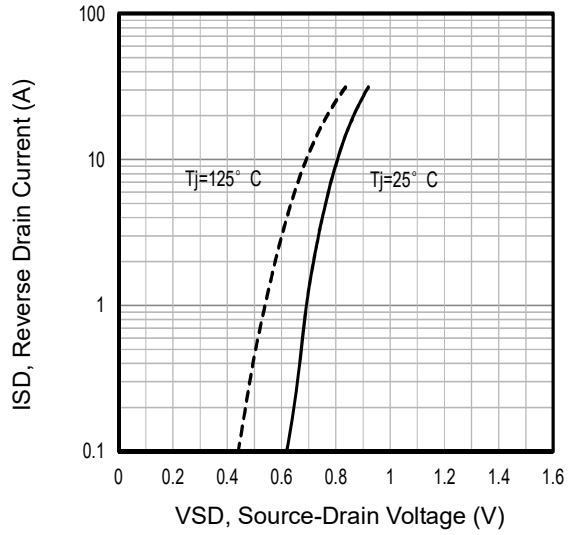


Fig7. Typical Source-Drain Diode Forward Voltage

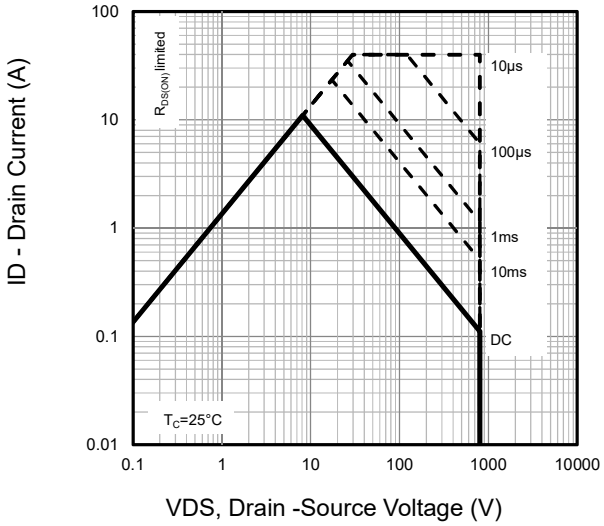


Fig8. Maximum Safe Operating Area

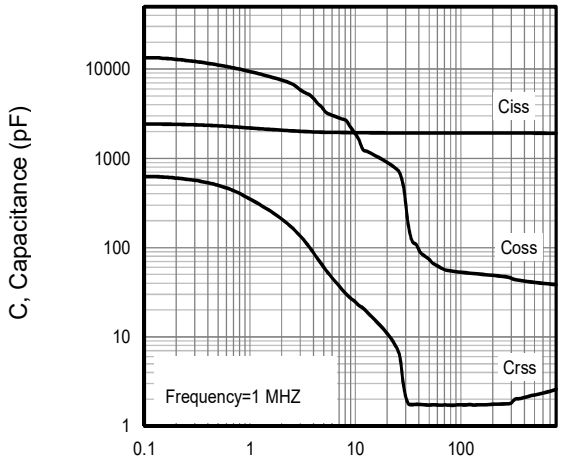


Fig9. Typical Capacitance Vs. Drain-Source Voltage

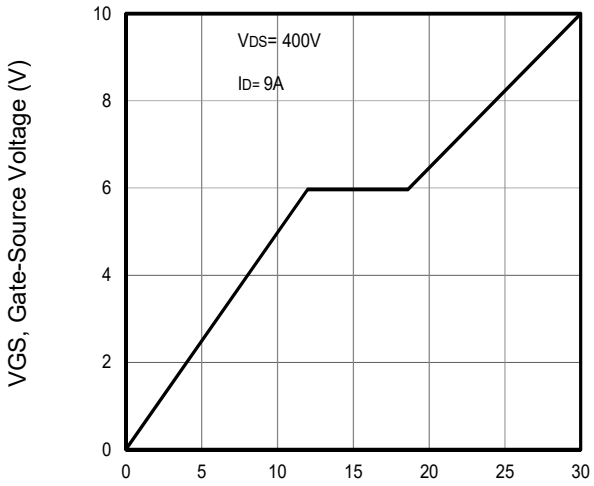


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

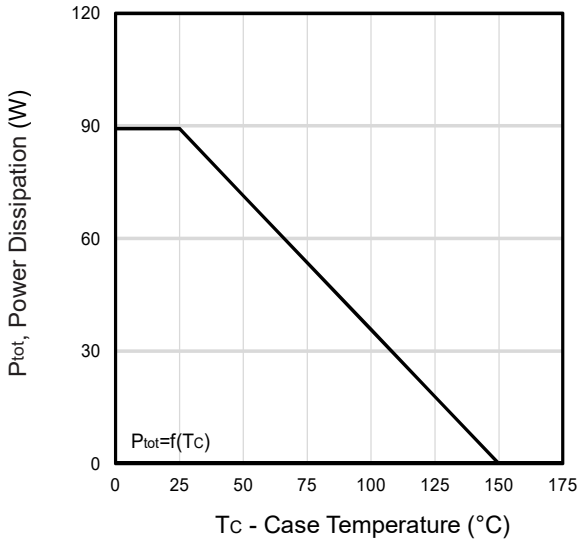


Fig11. Power Dissipation Vs. Case Temperature

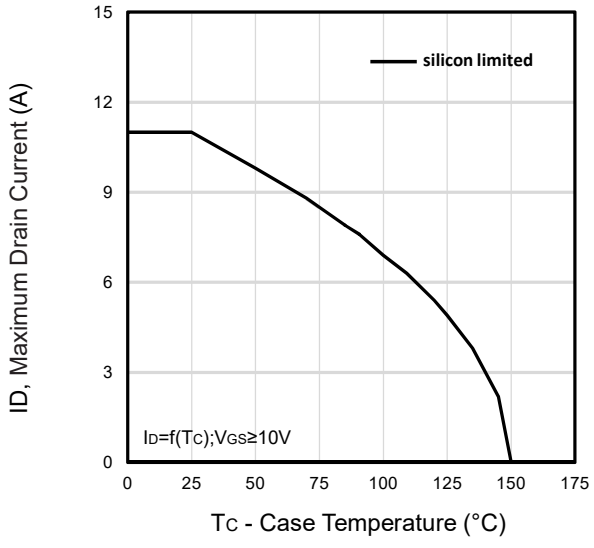


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

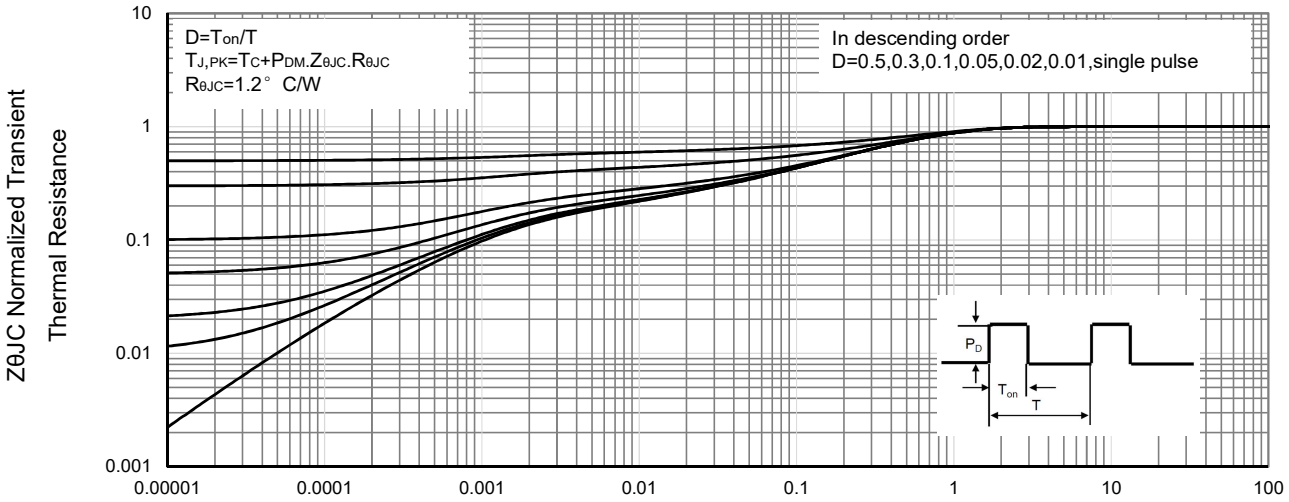


Fig13 . Normalized Maximum Transient Thermal Impedance

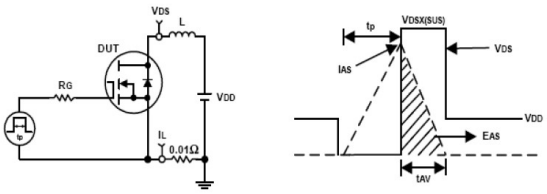


Fig14. Unclamped Inductive Test Circuit and waveforms

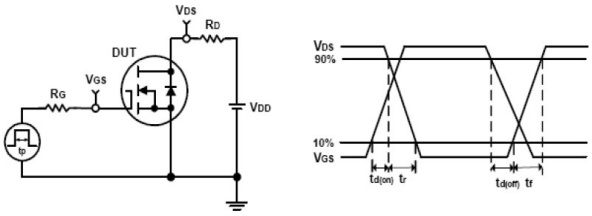
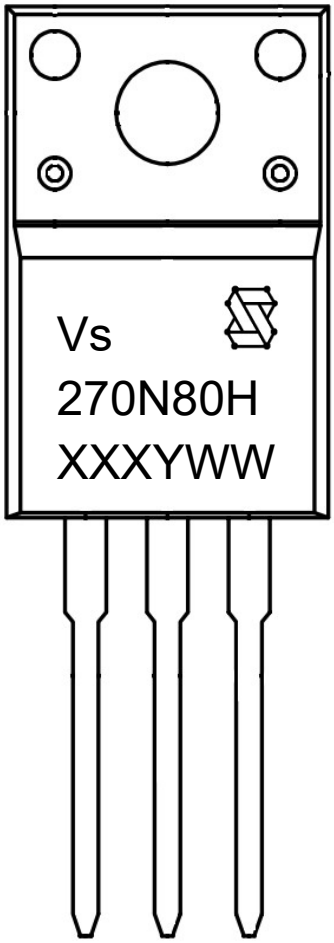


Fig15. Switching Time Test Circuit and waveforms

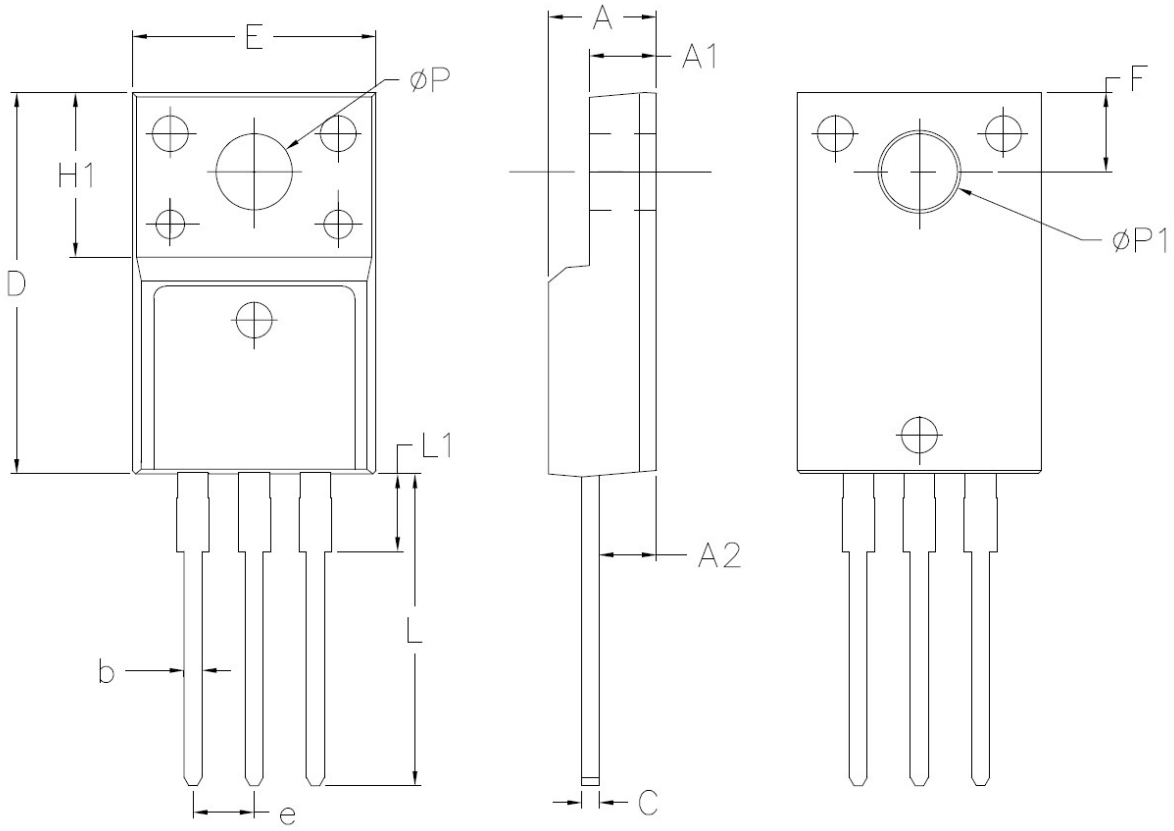
Marking Information



1st line: Vergiga Code（Vs），Vergiga Logo
2nd line: Part Number（270N80H）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220F Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	2.56	2.76	2.96
b	0.70	0.80	0.95
C	0.40	0.50	0.65
D	15.57	15.87	16.17
e	2.54 BSC		
E	9.96	10.16	10.36
F	3.15	3.30	3.45
H1	6.70 REF		
L	12.68	12.98	13.28
L1	3.03	3.23	3.43
ΦP	3.03	3.18	3.38
ΦP1	3.15	3.45	3.65

Customer Service

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