TIMESTREAM® PRODUCT FAMILY

VSC9182

VITESSE

VSC9182 - 40G STS-1 Time Slot Interchange

FEATURES:

Interconnection Matrix

- Time & Space Switches any STS-(n) [n= 1, 3c, 12c] Signal of an Incoming STS-12 into any Byte Position of any STS-12 Output
- Single Stage Non-blocking Structure of the Switch Allows for Multicast and Full Broadcast
- Hitless Switching: Programming is Queued and Takes Effect After user Intervention During the Next Frame Boundary
- Unequipped or AIS Signals can be Substituted into any of the Outgoing STS-1 Timeslots.
- Provides a Capability to Read out the Switch Configuration (address map)

Input Backplane Interface

- Serial 622.08 Mb/s Differential LVDS STS-12/STM-4 Inputs
- Receives 64 Serial 622.08 Mb/s STS-12/STM-4 Signals
- Input Signals are Presumed Frequency Synchronous and Frame aligned to Within +/- 3 Time Slots of the System SYNC Input
- Provides On-chip Data Recovery De-skewing Functionality to Bit-align, Byte-align and Frame-align all Incoming STS-12s (Within the above Tolerance) to the Local Clock
- Flags Out-of-frame (OOF), Loss-of-signal (LOS) and Parity Errors
- Checks B1 Parity of Incoming Data
- Inserts Unequipped or AIS When Channel is in OOF, LOS or Unprovisioned State and Inhibits Alarms
- Optionally De-scrambles Incoming SONET Data

Output Backplane Interface

- Serial 622.08 Mb/s Differential LVDS STS-12/STM-4 Outputs
- Optionally Inserts Byte-interleaved Parity into B1 Byte of Following Frame
- Optionally Scrambles Outgoing SONET Data
- Optionally Inserts AIS or Unequipped on a Per-channel, Per-time-slot Basis

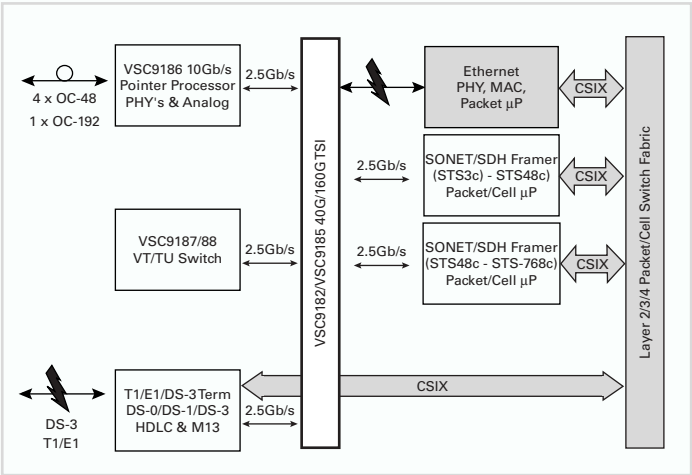
CPU Interface

- Generic Microprocessor (CPU) Interface used for Device Configuration and Status Checking
- 10-bit Data Bus and 11-bit Address Bus
- Interrupt Output Pin to Signal Status Changes of Internal Alarms

Test Interface

- IEEE P1149.1 Test Access Port Controls External Boundary Scan

TIMESTREAM DIAGRAM:



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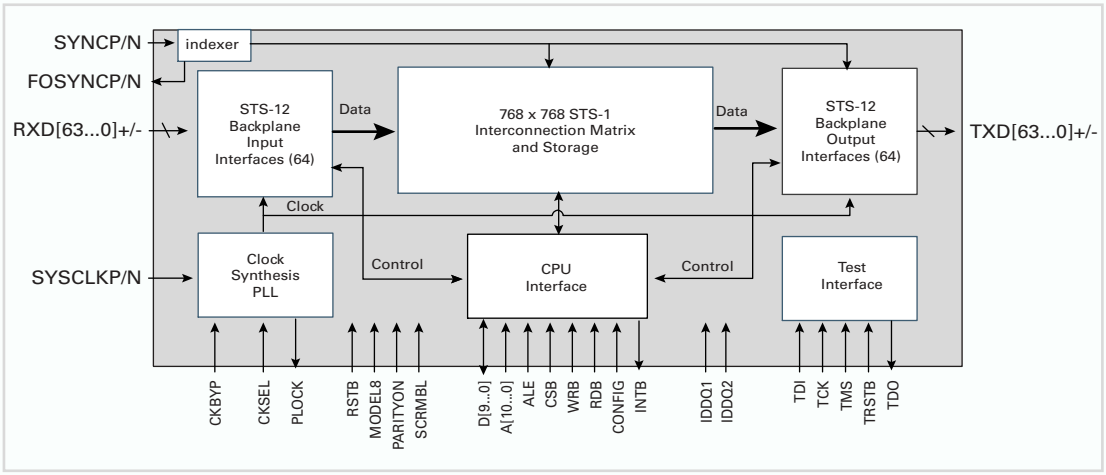
GENERAL DESCRIPTION:

The VSC9182 is a 64x64 STS-12/STM-4 Time Slot Interchange Switch IC. A single device provides 40Gb/s of non-blocking STS-1 connectivity (768x768 STS-1) with support for concatenated tributaries. All STS-12/STM-4 inputs and outputs are differential serial signals running at 622 Mb/s for efficiency in switch card and system backplane design. Backplane BER monitoring and deskew are integrated, and the connection matrix can be hitlessly reconfigured. Path AIS or UNEQ can be optionally inserted into all 768 outgoing STS-1 tributaries. A standard asynchronous CPU interface with event interrupts is also supported.

VSC9182 Architectures

A single VSC9182 provides sufficient connectivity for a 16x16 OC-48 STS-1 grooming solution. Multiple VSC9182 devices can be used in a three layer Clos architecture to construct larger switches, up to 1024 OC-48 ports. The VSC9182 is designed to interface directly with the VSC9186 10Gb/s Pointer Processor & Frame Aligner and VSC9180 2.5Gb/s Backplane Transceiver.

VSC9182 BLOCK DIAGRAM:



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