Preliminary Datasheet

VSC8166

2.488 Gbit/sec
1:16 SONET/SDH Demux with Clock Recovery

Features

- 2.488Gb/s 1:16 Demultiplexer
- Fully Integrated Clock and Data Recovery
- Single 3.3V Supply Operation
- Differential LVPECL Low Speed Interface
- Maintains Clock Output in the Absence of Data
- Loss of Lock, Loss of Signal Indicators
- 128 Pin 14x20x2 mm Enhanced PQFP Pkg.
- 2.3W Max Power Dissipation

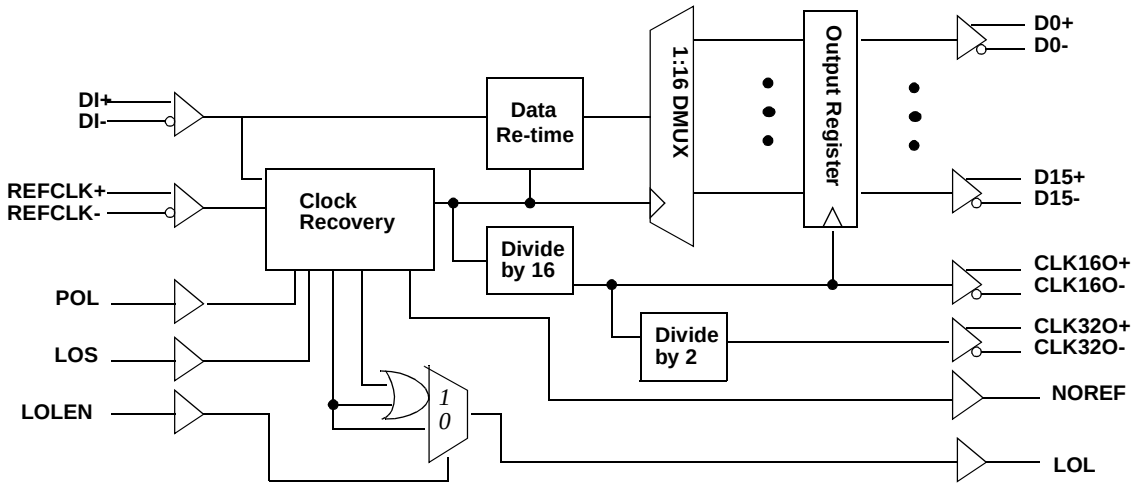
General Description

The VSC8166 demultiplexes a 2.488Gbp/s LVPECL serial input datastream (DI±) to 16-bit wide, LVPECL 155Mb/s parallel data outputs (D0:D15±) for SONET/SDH applications. It has an integrated clock and data recovery unit with an on-chip PLL that internally generates a 2.488GHz clock in phase with the incoming data. Internal divider circuits are used to take the high-speed clock and generate 155.52MHz (CLK16O±) and 77.76MHz (CLK32O±) LVPECL external output clocks. The incoming data is retimed and demultiplexed to a 16-bit word which is clocked out of the demultiplexer by the 155.52MHz output clock.

Alarm functions support typical telecom system applications. A TTL Loss Of Lock (LOL) indicator can be externally enabled (LOLEN) to detect when the device goes out of lock, which would most often occur in the event of a loss of valid data. A TTL No-Reference (NOREF) output indicator flags when the LVPECL Clock Reference (REFCLK) input to the VSC8166 either is removed, or goes severely out of tolerance. For Loss Of Signal (LOS) conditions from an Optics Module, the VSC8166 provides a polarity (POL) input to accommodate any polarity differences.

Only a single 3.3V power supply is required for device operation and the device is packaged in a thermally enhanced 128 Pin 14x20x2 mm PQFP Package.

VSC8166 Block Diagram



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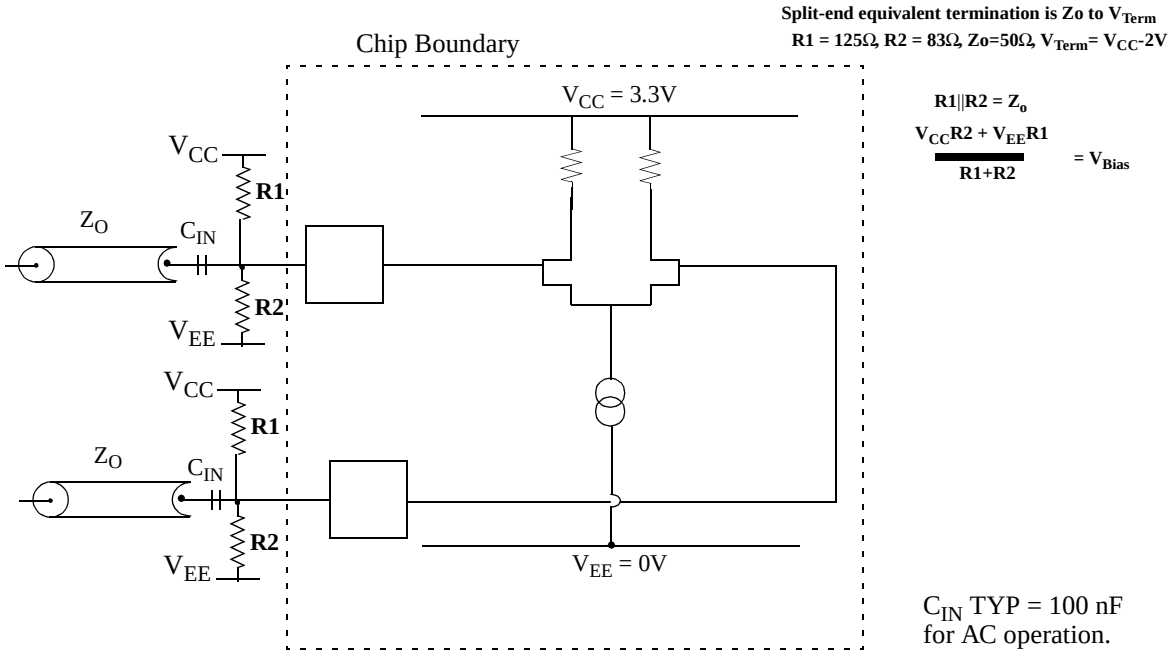
Functional Description

Clock Recovery:

The incoming SONET/SDH data stream is fed both to a re-timing latch and to the integrated clock recovery unit (CRU). The CRU exceeds the SONET/SDH jitter tolerance map. A 77.76MHz reference clock (REFCLK±) is required for CRU operation. Off-chip termination of this input is required. For AC coupling, a bias voltage suitable for AC coupling needs to be provided, see Figure 1 for biasing scheme. The 77.76MHz reference is used to permit the CLK16O± to remain locked to this external reference clock in the event of data loss.

Figure 1: AC Termination of LVPECL REFCLK Input



The VSC8166 has a TTL input LOS to force the part into a Loss of Signal state. Most optics have a TTL output usually called “SD” (Signal Detect), based on the optical power of the incoming light stream. Depending on the optics manufacturer, this signal is either active high or low. To accommodate polarity differences, the internal Loss of Signal is generated when the POL and LOS inputs are of opposite states. Once active, all zeroes “0” will be propagated downstream using the transmit clock until the optical signal is regained and LOS and POL are in the same logic state. When LOS and POL are opposite logic states, an internal LOS is asserted and all output data D(0:15)± will go to zero on the next rising edge of CLK16O+.

If LOLEN is low, and the serial input data consists of 3.3us or more of continuous zeros, LOL will go high and remain high for 100us following the restoration of valid data. If LOLEN is high, loss of data lock “OR” 3.3us of zeros will cause LOL to go high and remain high for 100us after both the return of non-zero data, and phase locking of the Serial data and clock are obtained.

NOREF will go high asynchronously when REFCLK is lost, or when REFCLK is not locked to the internal 2.488GHZ clock. It will remain high until the condition is corrected.

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Low Speed Interface

The demultiplexed serial stream is made available by a 16 bit differential LVPECL interface D(15:0)± with accompanying differential LVPECL divide by 16 clock CLK16O± and divide by 32 clock CLK32O±. The low speed LVPECL output drivers are designed to drive a 50Ω transmission line. The transmission line can be DC terminated with a split end termination scheme, see Figure 2, or DC terminated by 50Ω to V_{CC}-2V on each line, see Figure 3. At any time, the equivalent split-end termination technique can be substituted for the traditional 50Ω to V_{CC}-2V on each line. AC coupling can be achieved by a number of methods. Figure 4 illustrates an AC coupling method for the occasion when the downstream device provides the bias point for AC coupling. If the downstream device were to have internal termination, the line to line 100Ω resistor may not be necessary. The divide by 32 output can be used to provide a reference clock for the clock multiplication unit on the VSC8163.

Figure 2: Split-end DC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs

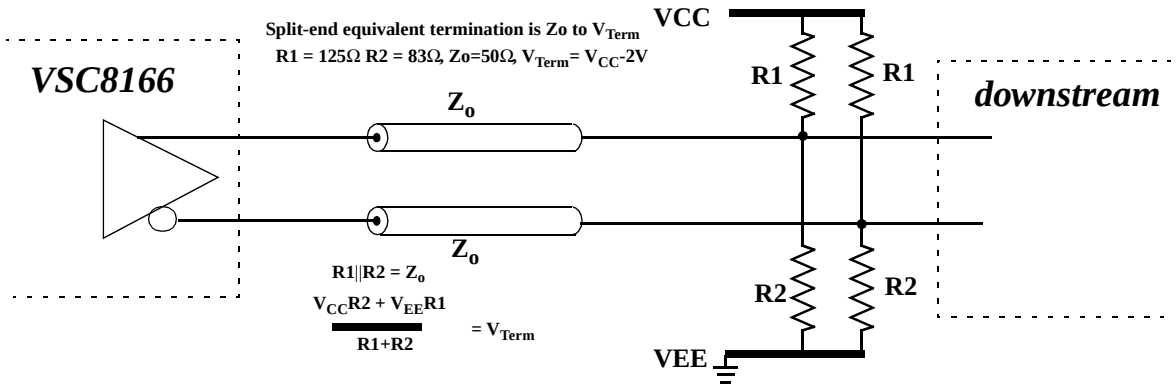

Figure 3: Traditional DC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs

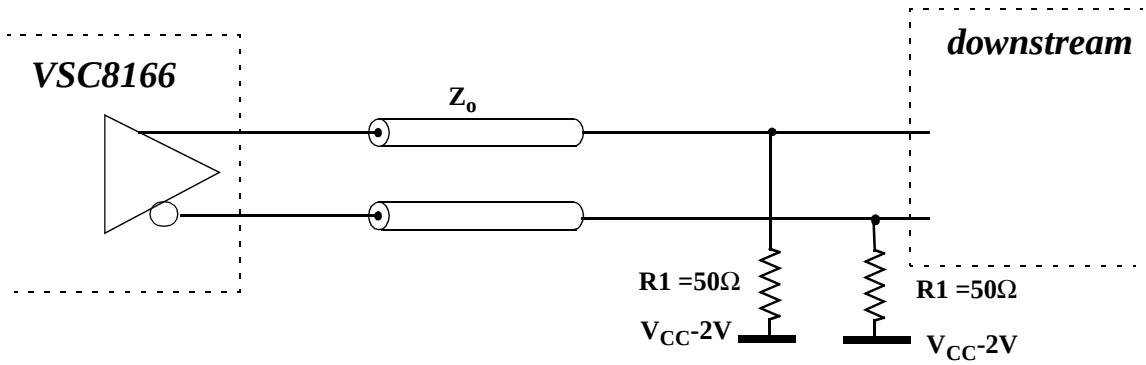

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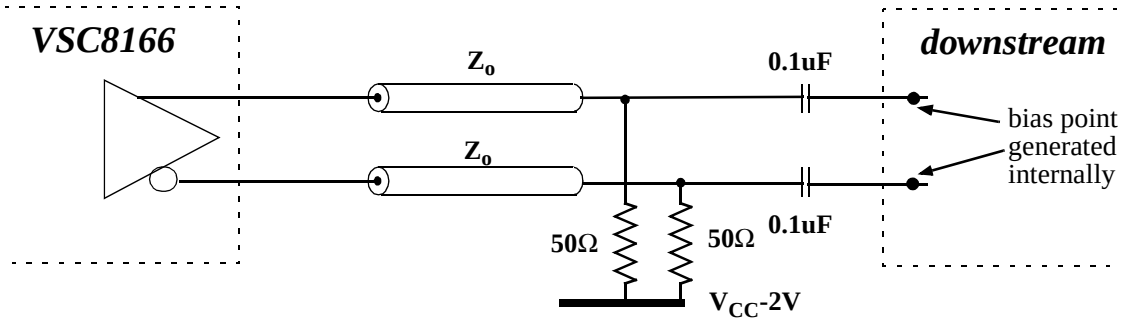
Figure 4: AC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs



High Speed Interface

The incoming 2.488Gb/s data is received by high speed inputs DI±. The data inputs are internally terminated by a center-tapped resistor network. For differential input DC coupling, the network is terminated to the appropriate termination voltage V_{TERM} (pins HSDREF) providing a 50Ω to V_{TERM} termination for both true and complement inputs. For differential input AC coupling, the network is terminated to V_{TERM} via a blocking capacitor.

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. Serial data inputs have the circuit topology shown in Figure 5. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude (ΔV_{CMI}, ΔV_{IHS}). For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

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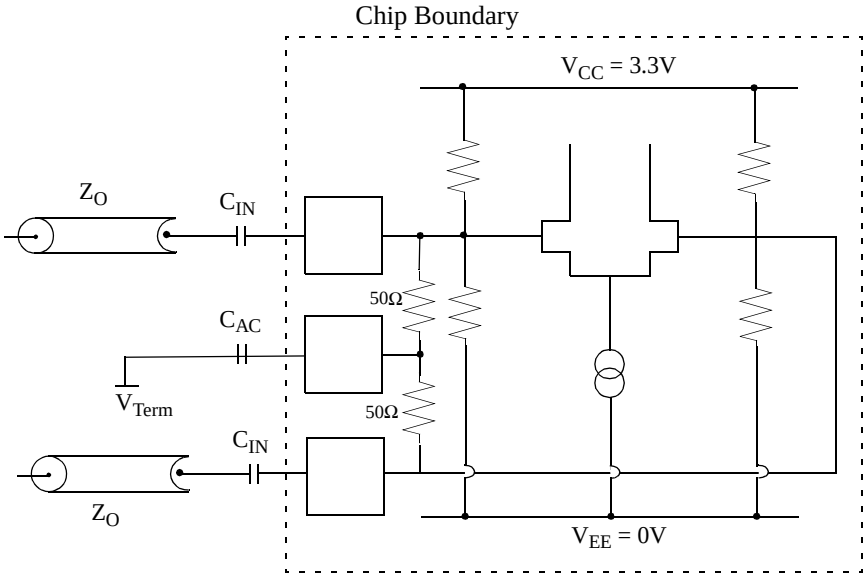
Figure 5: High Speed Serial Data Inputs



C_{IN} TYP = 100 pF

C_{AC} TYP = 100pF

Supplies

This device is specified as a LVPECL device with a single positive 3.3V supply. Should the user desire to use the device in a ECL environment with a negative 3.3V supply, then VCC will be ground and VEE will be -3.3V.

Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0403 packages.

For low frequency decoupling, 47µF tantalum low inductance SMT caps should be sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a -3.3V supply, then all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling 3.3V must be changed to -3.3V.

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AC Characteristics

Figure 6: AC Timing Waveforms

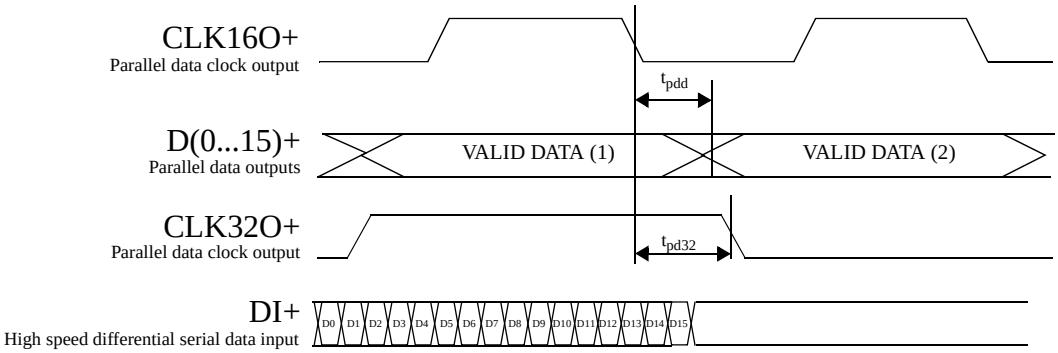
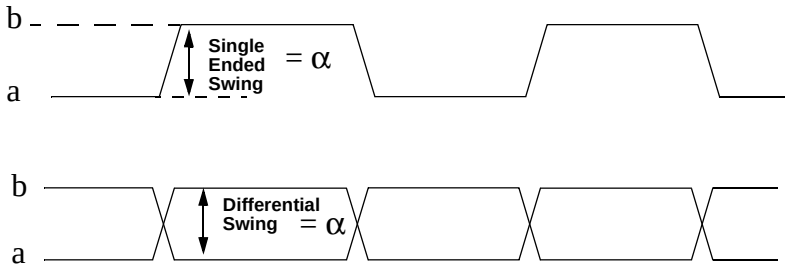


Figure 7: Differential and Single Ended Input and Output Voltage Measurement



* Differential swing (α) is specified as | b - a | (or | a - b |), as is the single ended swing. Differential swing is specified as equal in magnitude to single ended swing.

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Table 1: AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
t_{pdd}	Data valid from falling edge of CLK16O+	0	1.0	ns	
t_{pd32}	CLK32O transition from falling edge of CLK16O+	0	1.0	ns	
t_{DR}, t_{DF}	D[15:0]+/- rise and fall times		400	ps	20% to 80% into 50 Ohm load See Figure 7
t_{CLKR}, t_{CLKF}	CLK16O+/- rise and fall times		400	ps	20% to 80% into 50 Ohm load See Figure 7
t_{CLKR32}, t_{CLKF32}	CLK32O+/- rise and fall times		400	ps	20% to 80% into 50 Ohm load See Figure 7
$CLK16O_D$	CLK16O+/- duty cycle distortion	45	55	% of clock cycle	

Table 2: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	PECL output high voltage	V_{CC}-1.02		V_{CC}-0.70	V	50Ω Termination to V_{CC} - 2.0V, See Figure 7
V_{OL}	PECL output low voltage	V_{CC}-2.00		V_{CC}-1.62	V	50Ω Termination to V_{CC} - 2.0V, See Figure 7
$\Delta V_{OLVPECL}$	Low speed output voltage differential peak-to-peak swing.	400		1200	mV	50Ω Termination to V_{CC} - 2.0V, See Figure 7
ΔV_{IHS}	Serial input differential (DI+/-)	400		1200	mV	AC Coupled, internally biased to $(V_{CC}+V_{EE})/2$
ΔV_{CMI}	Serial input common mode voltage	V_{CC}-1.5		V_{CC}-0.5	V	
V_{CC}	Supply voltage	3.14	—	3.47	V	3.3V± 5%
P_D	Power dissipation	—	1.7	2.3	W	Outputs open, V_{CC} = 3.45V
I_{DD}	Supply Current	—	525	660	mA	Outputs open, V_{CC} = 3.45V

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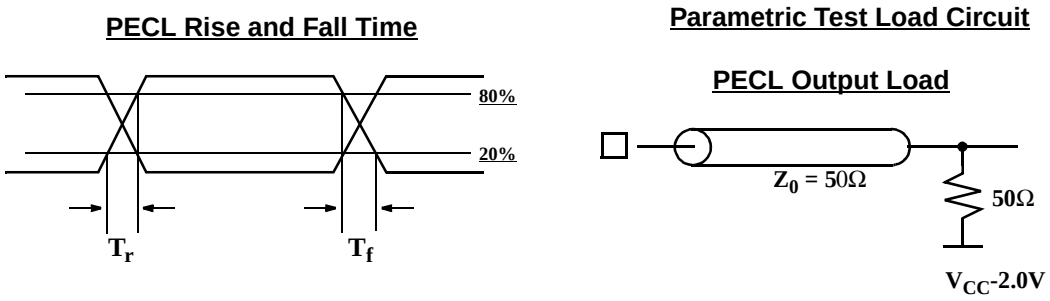
Figure 8: Parametric Measurement Information



Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{cc}+0.5V
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^o to +125^{o}C
Storage Temperature ..... -65^{o}C to +150^{o}C
Maximum Input ESD (Human Body Model) 1500V

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +3.3V±5%
Operating Temperature Range ..... 0^{o}C Ambient to +85^{o}C Case Temperature

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8166 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Table 3: Package Pin Identification

Pin #	*Name*	*I/O*	*Level*	*Description*
1	NC	—	—	No connect, leave unconnected
2	NC	—	—	No connect, leave unconnected
3	CLKREF	I/O	0V or 1.3V	Reference clock input termination voltage. 1.3V for DC coupling, otherwise 0V.
4	VCC	—	3.3V typ.	Positive power supply pin
5	VEE_CMU	—	GND typ.	Negative power supply for CMU
6	VEE_CMU	—	GND typ.	Negative power supply for CMU
7	VEE_CMU	—	GND typ.	Negative power supply for CMU
8	VCC_CMU	—	3.3V typ.	Positive power supply for CMU
9	REFCLK+	I	LVPECL	Reference clock input, true.
10	REFCLK-	I	LVPECL	Reference clock input, complement.
11	VCC_CMU	—	3.3V typ.	Positive power supply for CMU
12	VCC	—	3.3V typ.	Positive power supply pin
13	DI+	I	LVPECL	High speed data input, true
14	DI-	I	LVPECL	High speed data input, complement
15	VEE	—	GND typ.	Negative power supply pin
16	VEE	—	GND typ.	Negative power supply pin
17	VEE	—	GND typ.	Negative power supply pin
18	VCC	—	3.3V typ.	Positive power supply pin
19	HSDREF	I	0V or 1.3V	High speed data input termination voltage reference. 1.3V for DC coupling, otherwise 0V.
20	NC	—	—	No connect, leave unconnected
21	VCC	—	3.3V typ.	Positive power supply pin
22	NC	—	—	No connect, leave unconnected
23	VCC	—	3.3V typ.	Positive power supply pin
24	VCC	—	3.3V typ.	Positive power supply pin
25	VCC	—	3.3V typ.	Positive power supply pin
26	VEE	—	GND typ.	Negative power supply pin
27	VEE	—	GND typ.	Negative power supply pin
28	VEE	—	GND typ.	Negative power supply pin
29	VEE	—	GND typ.	Negative power supply pin
30	VEE	—	GND typ.	Negative power supply pin
31	NC	—	—	No connect, leave unconnected
32	NC	—	—	No connect, leave unconnected
33	NC	—	—	No connect, leave unconnected
34	NC	—	—	No connect, leave unconnected

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Table 3: Package Pin Identification

Pin #	*Name*	*I/O*	*Level*	*Description*
35	NC	—	—	No connect, leave unconnected
36	NC	—	—	No connect, leave unconnected
37	NC	—	—	No connect, leave unconnected
38	NC	—	—	No connect, leave unconnected
39	VCCT	—	+3.3V typ.	TTL V_{CC} Power Supply
40	VEET	—	GND typ.	TTL V_{EE} Power Supply
41	NC	—	—	No connect, leave unconnected
42	VEE	—	GND typ.	Negative power supply pin
43	VCC	—	3.3V typ.	Positive power supply pin
44	LOLEN	I	TTL	Loss of Lock enable. LOLEN= “1”: LOL asserts high when loss of data OR 3.3µS of zeroes, LOLEN=“0”: LOL assets high when 3.3µS of zeroes
45	NC	—	—	No connect, leave unconnected
46	NC	—	—	No connect, leave unconnected
47	NC	—	—	No connect, leave unconnected
48	NC	—	—	No connect, leave unconnected
49	NC	—	—	No connect, leave unconnected
50	VCC	—	3.3V typ.	Positive power supply pin
51	VEE	—	GND typ.	Negative power supply pin
52	REFCK_TEST	—	GND typ.	Test input signal used for production test. Active high. Connect to ground for normal operation.
53	NC	—	—	No connect, leave unconnected
54	VCC	—	3.3V typ.	Positive power supply pin
55	LOS	I	TTL	Loss of Signal control
56	POL	I	TTL	Polarity Signal Control
57	VEE	—	GND typ.	Negative power supply pin
58	D15+	O	LVPECL	Low speed differential parallel data, true
59	D15-	O	LVPECL	Low speed differential parallel data, compliment
60	VCC	—	3.3V typ.	Positive power supply pin
61	D14+	O	LVPECL	Low speed differential parallel data, true
62	D14-	O	LVPECL	Low speed differential parallel data, compliment
63	NC	—	—	No connect, leave unconnected
64	VCC	—	3.3V typ.	Positive power supply pin
65	NC	—	—	No connect, leave unconnected
66	VCC	—	3.3V typ.	Positive power supply pin
67	D13+	O	LVPECL	Low speed differential parallel data, true
68	D13-	O	LVPECL	Low speed differential parallel data, compliment
69	VEE	—	GND typ.	Negative power supply pin

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Table 3: Package Pin Identification

Pin #	*Name*	*I/O*	*Level*	*Description*
70	D12+	O	LVPECL	Low speed differential parallel data, true
71	D12-	O	LVPECL	Low speed differential parallel data, compliment
72	VCC	—	3.3V typ.	Positive power supply pin
73	D11+	O	LVPECL	Low speed differential parallel data, true
74	D11-	O	LVPECL	Low speed differential parallel data, compliment
75	VCC	—	3.3V typ.	Positive power supply pin
76	D10+	O	LVPECL	Low speed differential parallel data, true
77	D10-	O	LVPECL	Low speed differential parallel data, compliment
78	VEE	—	GND typ.	Negative power supply pin
79	D9+	O	LVPECL	Low speed differential parallel data, true
80	D9-	O	LVPECL	Low speed differential parallel data, compliment
81	VCC	—	3.3V typ.	Positive power supply pin
82	D8+	O	LVPECL	Low speed differential parallel data, true
83	D8-	O	LVPECL	Low speed differential parallel data, compliment
84	VCC	—	3.3V typ.	Positive power supply pin
85	D7+	O	LVPECL	Low speed differential parallel data, true
86	D7-	O	LVPECL	Low speed differential parallel data, compliment
87	VEE	—	GND typ.	Negative power supply pin
88	D6+	O	LVPECL	Low speed differential parallel data, true
89	D6-	O	LVPECL	Low speed differential parallel data, compliment
90	VCC	—	3.3V typ.	Positive power supply pin
91	D5+	O	LVPECL	Low speed differential parallel data, true
92	D5-	O	LVPECL	Low speed differential parallel data, compliment
93	VCC	—	3.3V typ.	Positive power supply pin
94	D4+	O	LVPECL	Low speed differential parallel data, true
95	D4-	O	LVPECL	Low speed differential parallel data, compliment
96	VEE	—	GND typ.	Negative power supply pin
97	D3+	O	LVPECL	Low speed differential parallel data, true
98	D3-	O	LVPECL	Low speed differential parallel data, compliment
99	VCC	—	3.3V typ.	Positive power supply pin
100	D2+	O	LVPECL	Low speed differential parallel data, true
101	D2-	O	LVPECL	Low speed differential parallel data, compliment
102	VCC	—	3.3V typ.	Positive power supply pin
103	VCC	—	3.3V typ.	Positive power supply pin
104	NC	—	—	No connect, leave unconnected
105	D1+	O	LVPECL	Low speed differential parallel data, true
106	D1-	O	LVPECL	Low speed differential parallel data, compliment

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Table 3: Package Pin Identification

Pin #	*Name*	*I/O*	*Level*	*Description*
107	VCC	—	3.3V typ.	Positive power supply pin
108	D0+	O	LVPECL	Low speed differential parallel data, true
109	D0-	O	LVPECL	Low speed differential parallel data, compliment
110	VEE	—	GND typ.	Negative power supply pin
111	CLK16O-	O	LVPECL	Parallel clock output, complement
112	CLK16O+	O	LVPECL	Parallel clock output, true
113	VCC	—	3.3V typ.	Positive power supply pin
114	CLK32O-	O	LVPECL	Divided Parallel clock output, complement
115	CLK32O+	O	LVPECL	Divided Parallel clock output, true
116	NC	—	—	No connect, leave unconnected
117	NOREF	O	TTL	No reference clock output. Active high for REFCLK missing or severely out of tolerance.
118	VCCT	—	3.3V typ.	Positive power supply pin (TTL)
119	VEEY	—	GND typ.	Negative power supply pin (TTL)
120	LOL	O	TTL	Loss of lock indicator.
121	NC	—	—	No connect, leave unconnected
122	VEE	—	GND typ.	Negative power supply pin
123	VCC	—	3.3V typ.	Positive power supply pin
124	NC	—	—	No connect, leave unconnected
125	NC	—	—	No connect, leave unconnected
126	VEE	—	GND typ.	Negative power supply pin
127	VEE	—	GND typ.	Negative power supply pin
128	VCC	—	3.3V typ.	Positive power supply pin

Note: No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative power supply rails may cause improper operation or failure of the device; or in extreme cases, cause permanent damage to the device.

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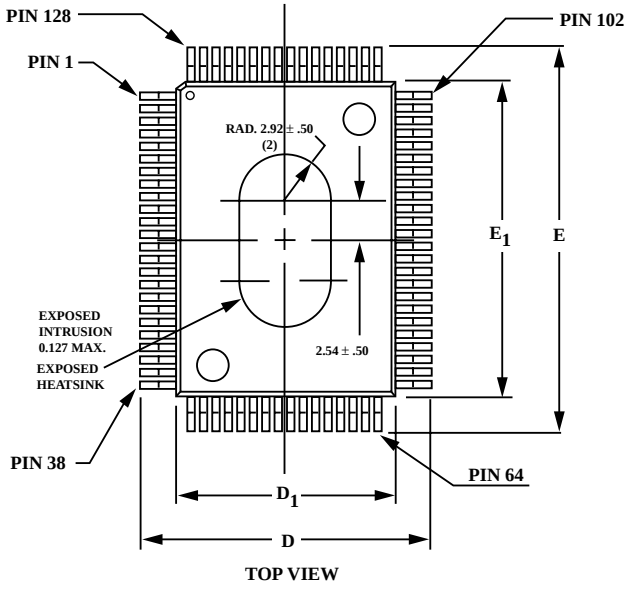
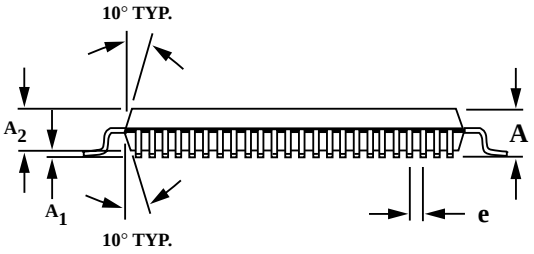
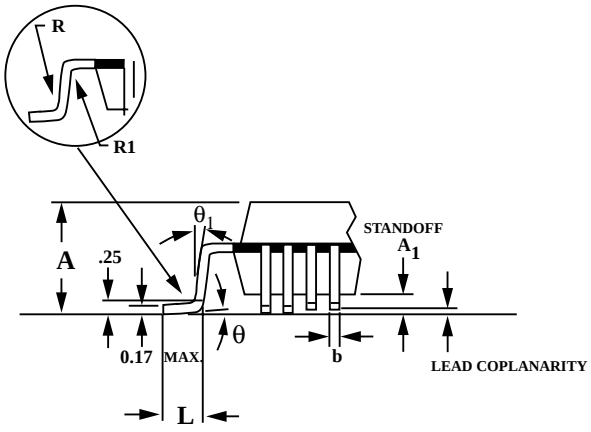
Package Information

128 PQFP Package Drawings



Key	mm	Tolerance
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

NOTES:

Package #: 101-322-5
Issue #: 2

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Package hermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table

Table 4: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{jc}	Thermal resistance from junction to case.	2.2
θ_{ja}	Thermal resistance from junction to ambient with no airflow, including conduction through the leads.	23.9

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 5: Thermal Resistance with Airflow

Airflow	θ_{ca} *(°C/W)*
100 lfpm	19.8
200 lfpm	16.7
400 lfpm	14.6
600 lfpm	13.0

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

$T_{A(MAX)}$ Ambient Air temperature
$T_{C(MAX)}$ Case temperature (85°C for VSC8166)
$P_{(MAX)}$ Power (2.3W for VSC8166)
θ_{CA} Theta case to ambient at appropriate airflow

The results of this calculation are listed below:

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Table 6: Maximum Ambient Air Temperature without Heatsink

Airflow	Max Ambient Temp ^{0}C
none	29.6
100 lfpm	39.5
200 lfpm	46.6
400 lfpm	51.4
600 lfpm	55.1

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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