VITESSE

VSC8117
Data Sheet

ATM/SONET/SDH 622Mb/s or 155Mb/s Transceiver Mux/Demux with Integrated Clock Generation and Clock Recovery

FEATURES

- Operates at either STS-3/STM-1 (155.52Mb/s) or STS-12/STM-4 (622.08Mb/s) data rates
- Compatible with industry ATM UNI devices
- On-chip clock generation of the 155.52MHz or 622.08MHz high-speed clock (Mux)
- On-chip clock recovery of the 155.52MHz or 622.08MHz high-speed clock (Demux)
- 8-bit parallel TTL interface
- SONET/SDH frame recovery
- Loss of Signal (LOS) input and LOS detection
- 3.3V/5V programmable PECL serial interface
- Provides Equipment, Facilities, Split Loopback, and Loop Timing modes
- Provides TTL and PECL reference clock inputs
- Low power: 1W typical
- 64-pin PQFP package

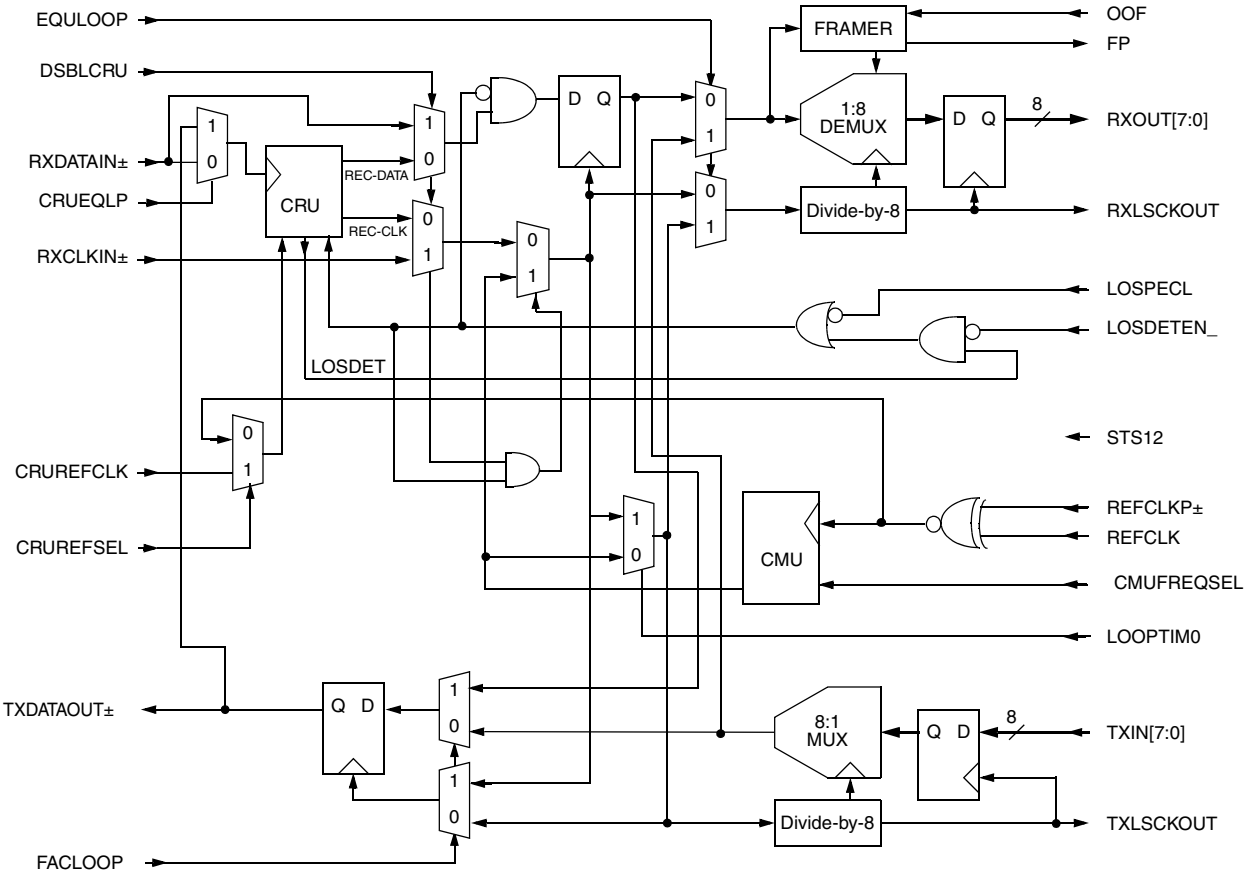
GENERAL DESCRIPTION

The VSC8117 is an ATM/SONET/SDH-compatible transceiver that integrates an on-chip clock multiplication unit (CMU) for the high-speed clock, as well as a clock and data recovery (CDR) unit with 8-bit serial-to-parallel and parallel-to-serial data conversion. The phase-locked loop (PLL) clock is used for serialization in the transmit direction (Mux). The recovered clock is used for deserialization in the receive direction (Demux). The demultiplexer contains SONET/SDH frame detection and recovery. The VSC8117 provides facility, equipment, and loopback modes.

The VSC8117 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

The VSC8117 is packaged in a 64-pin, plastic quad flat pack (PQFP) with an integrated heat spreader for optimum thermal performance and reduced cost. The device is also available in lead(Pb)-free packages, VSC8117XQP, VSC8117XQP1, and VSC8117XQP2.

VSC8117 Block Diagram



REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.7

Revision 4.7 of this data sheet was published on September 25, 2007. In revision 4.7 of the document, the moisture sensitivity level ratings for the VSC8117QP, VSC8117QP1, and VSC8117QP2 devices were changed to level 4. For more information, see "Moisture Sensitivity Level" on page 21.

Revision 4.6

Revision 4.6 of this data sheet was published on March 20, 2007. In revision 4.6 of the document, the maximum value for the power supply current from V_{DD} and power dissipation parameters were updated.

Revision 4.5

Revision 4.5 of this data sheet was published in September 2006. The following is a summary of the changes implemented in the data sheet:

- Thermal specifications were added.
- The lead(Pb)-free packages VSC8117XQP, VSC8117XQP1, and VSC8117XQP2 were added.

FUNCTIONAL DESCRIPTION

The VSC8117 is designed to provide a SONET/SDH-compliant interface between the high-speed optical networks and the lower speed User Network Interface (UNI) devices, such as the PM5355 S/UNI-622. The VSC8117 converts 8-bit parallel data at 77.76Mb/s or 19.44Mb/s to a serial bit stream at 622.08Mb/s or 155.52Mb/s, respectively. The VSC8117 also provides a facility loopback function that loops the received high-speed data and clock (optionally recovered on-chip) directly to the high-speed transmit outputs. A CMU is integrated into the transmit circuit to generate the high-speed clock for the serial output data stream from input reference frequencies of 19.44MHz or 77.76 MHz. The CMU can be bypassed with the recovered clock in the loop timing mode, thus synchronizing the entire device to a single clock. See "VSC8117 Block Diagram" on page 2 for major functional blocks associated with the VSC8117.

The receive section provides the serial-to-parallel conversion, converting the 622Mb/s or 155.52Mb/s bit stream to an 8-bit parallel output at 19.44Mb/s or 77.76Mb/s, respectively. A CRU is integrated into the receive circuit to recover the high-speed clock from the received serial data stream. The receive section provides an equipment loopback function that will loop the low-speed transmit data and clock back through the receive section to the 8-bit parallel data bus and clock outputs. The VSC8117 also provides the option of selecting between either its internal CRU's recovered clock and data signals or optics containing a CRU clock and data signals. (In this mode the VSC8117 operates the same as the VSC8111 and VSC8116.) The receive section also contains a SONET/SDH frame detector circuit that is used to provide frame pulses during the A1, A2 boundary in the serial-to-parallel converter, which only occurs when OOF is HIGH. Both internal and external Loss of Signal (LOS) functions are supported. The high-speed serial signals can be made PECL or LVPECL compatible by setting the proper voltage on the V_{DDP} supply pins.

Transmit Section

Byte-wide data is presented to TXIN[7:0] and is clocked into the device on the rising edge of TXLSCKOUT. TXLSCKOUT also latches TXIN[7:0] into the VSC8117 as shown in Figure 1. The data is then serialized (MSB-first) and presented at the TXDATAOUT± pins. The serial output stream is synchronized to the CMU-generated clock, which is a phase-locked and frequency-scaled version of the input reference clock. External control inputs, CMUFREQSEL and STS-12, select the multiply ratio of the CMU for either STS-12 (622Mb/s) or STS-3 (155Mb/s) transmission (see Table 10 on page 14). A divide-by-8 version of the CMU clock (TXLSCKOUT) should be used to synchronize the transmit interface of the UNI device to the transmit input registers on the VSC8117.

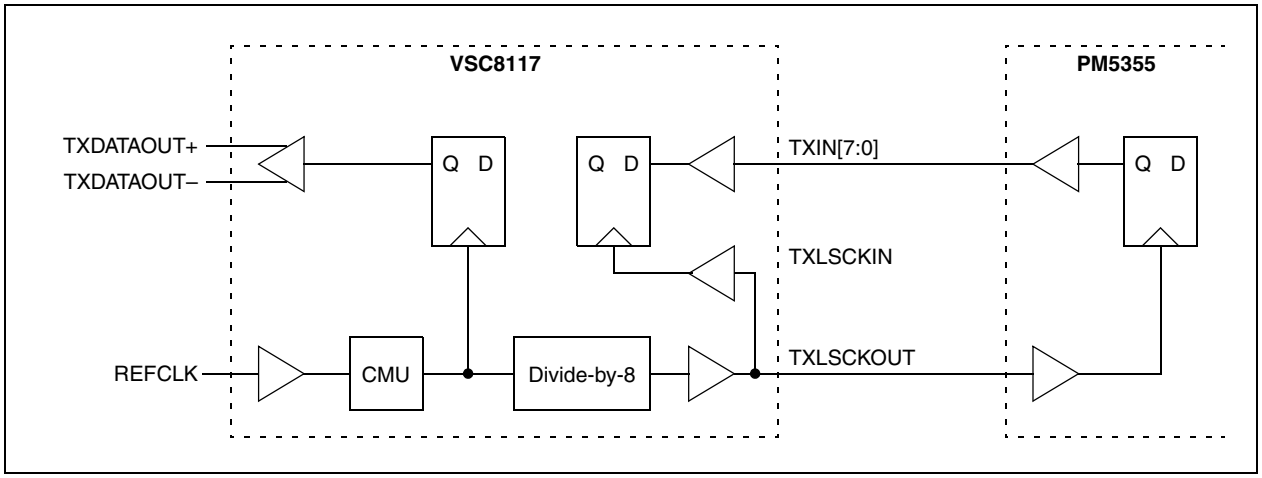


Figure 1. Data and Clock Transmit Block Diagram

Receive Section

High-speed Non-Return to Zero (NRZ) serial data at 155Mb/s or 622Mb/s is received by the RXDATAIN inputs. The CRU recovers the high-speed clock from the serial data input. The serial data is converted to byte-wide parallel data and presented on RXOUT[7:0] pins. A divide-by-8 version of the high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT[7:0] data with the receive portion of the UNI device. The on-chip CRU is bypassed by setting the DSBLCRU input HIGH. In this mode, the serial input data and corresponding clock are received by the RXDATAIN and RXCLKIN inputs, respectively. RXDATAIN is clocked in on the rising edge of RXCLKIN+. See Figure 2.

The receive section also includes frame detection and recovery circuitry that detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP, coincident with the byte-aligned data. The frame recovery is initiated when OOF is held HIGH, which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8117 will continually perform frame detection and recovery as long as this pin is held HIGH, even if one or more frames have been detected. Frame detection and recovery occurs when a series of three A1 bytes, followed by three A2 bytes, have been detected. The parallel output data on RXOUT[7:0] will be byte-aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP, which is synchronized with the byte-aligned third A2 byte on RXOUT[7:0]. The frame detector sends a FP pulse only if OOF is HIGH.

Loss of Signal

The VSC8117 features Loss of Signal (LOS) detection. LOS is declared if the incoming serial data stream has no transition continuously for more than 128 bits. During an LOS condition, the VSC8117 forces the receive data LOW, which is an indication for any downstream equipment that an optical interface failure has occurred. The receive section continues to be clocked by the CRU as it is now locked to the CRUREFCLK, unless DSBLCRU is active or CRUREFSEL is inactive, in which case, it will be clocked by the CMU. This LOS condition will be removed when the device detects more than 16 transitions in a 128-bit time window. This LOS detection feature can be disabled by applying a high level to LOSDETEN_ input. The VSC8117 also has a PECL input (LOSPECL) to force the device into a LOS state. Most optics have a PECL output, usually called SD or FLAG, indicating a lack of or presence of optical power. Depending on the optics manufacturer, this signal is either active HIGH or active LOW. The LOSPECL input on the VSC8117 is active LOW.

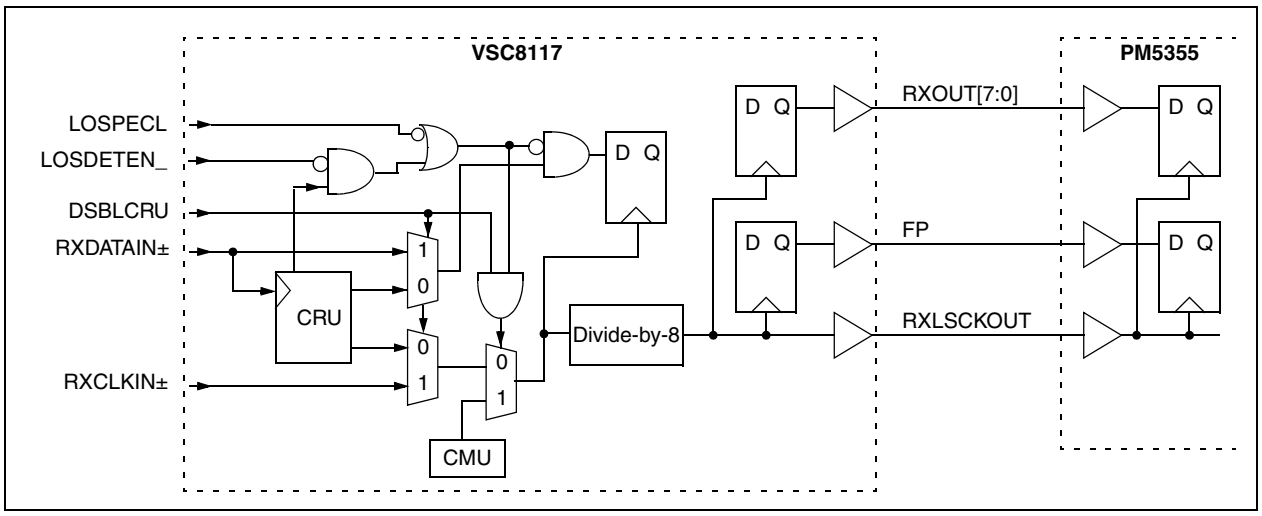


Figure 2. Data and Clock Receive Block Diagram

Facility Loopback

The Facility Loopback mode is controlled by the FACLOOP signal. When the FACLOOP signal is set HIGH, the Facility Loopback mode is activated, and the high-speed serial receive data (RXDATAIN) is presented at the high-speed transmit output (TXDATAOUT). See Figure 3. In Facility Loopback mode the high-speed receive data (RXDATAIN) is also converted to parallel data and presented at the low-speed receive data output pins (RXOUT[7:0]). The receive clock (RXCLKIN) or the recovered clock is also divided down and presented at the low-speed clock output (RXLSCKOUT).

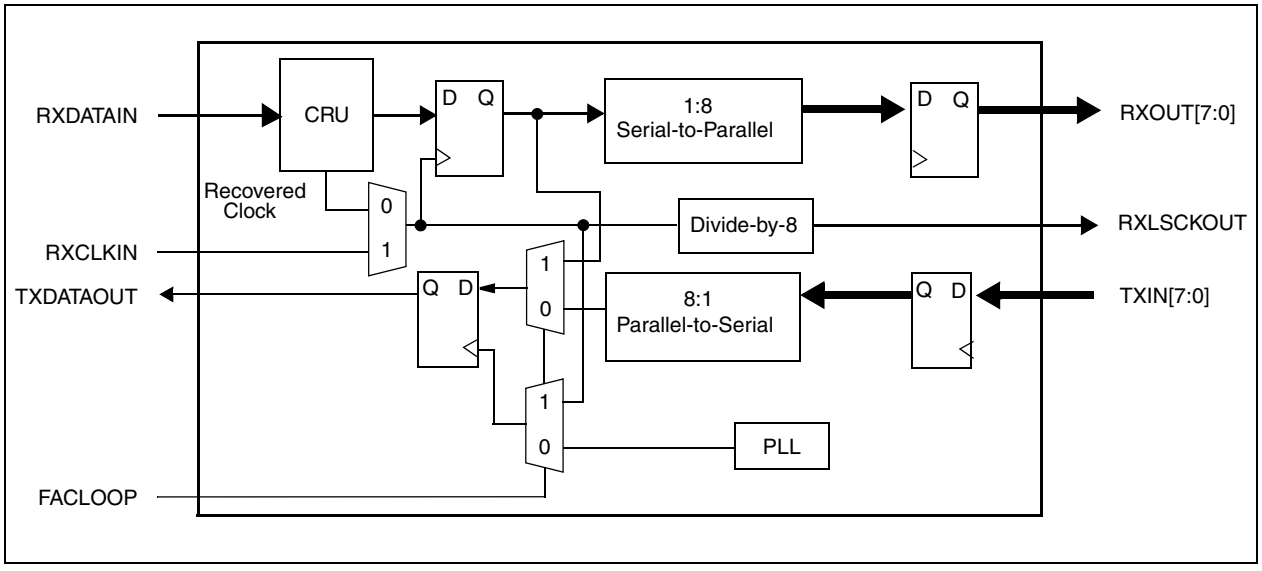


Figure 3. Facility Loopback Data Path

Equipment Loopback

The Equipment Loopback mode is controlled by the EQULOOP signal. When the EQULOOP signal is set HIGH, the Equipment Loopback mode is activated, and the high-speed transmit data generated from the parallel-to-serial conversion of the low-speed data (TXIN[7:0]) is selected and converted back to parallel data in the receiver section and presented at the low-speed parallel outputs (RXOUT[7:0]). See Figure 4 on page 7. The internally-generated 155MHz/622MHz clock is used to generate the low-speed receive clock output (RXLSCKOUT). In Equipment Loopback mode, the transmit data (TXIN[7:0]) is serialized and presented at the high-speed output (TXDATAOUT).

CRU Equipment Loopback

In the CRU Equipment Loopback mode, the parallel transmit data is serialized, presented at the high-speed output (TXDATOUT), and internally routed to the CRU. When the CRUEQLP signal is set HIGH, the CRU Equipment Loopback mode is activated.

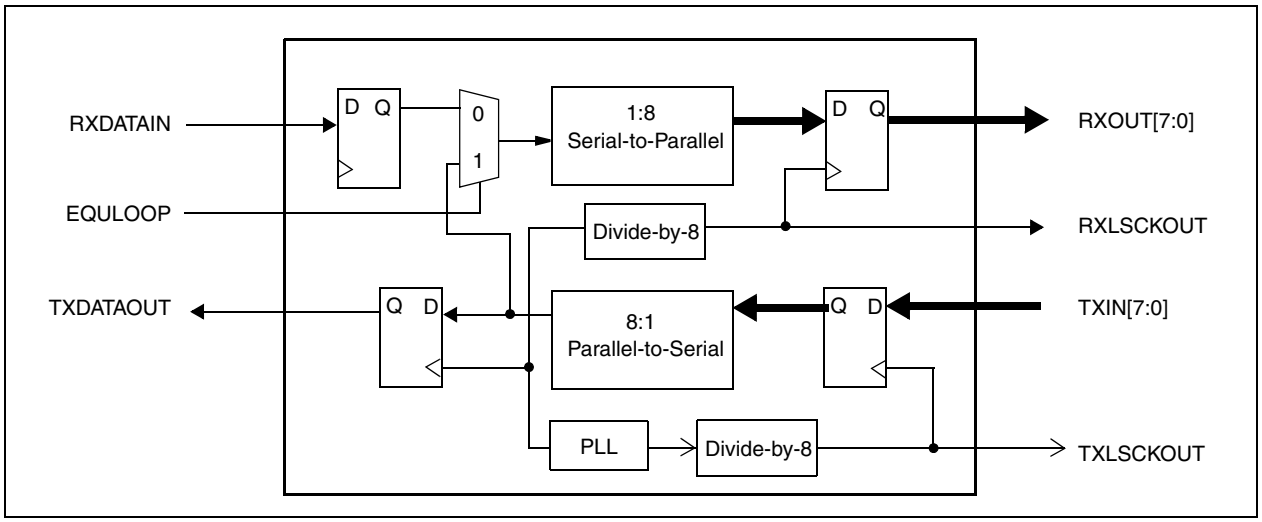


Figure 4. Equipment Loopback Data Path

Split Loopback

The Equipment and Facility Loopback modes can be enabled simultaneously. To enable both modes, high-speed serial data received (RXDATAIN) is muxed through to the high-speed serial output (TXDATAOUT). The low-speed transmit byte-wide bus (TXIN[7:0]) and (TXLSCKIN) are muxed into the low-speed byte-wide receive output bus (RXOUT[7:0]) and (RXLSCKOUT). See Figure 5.

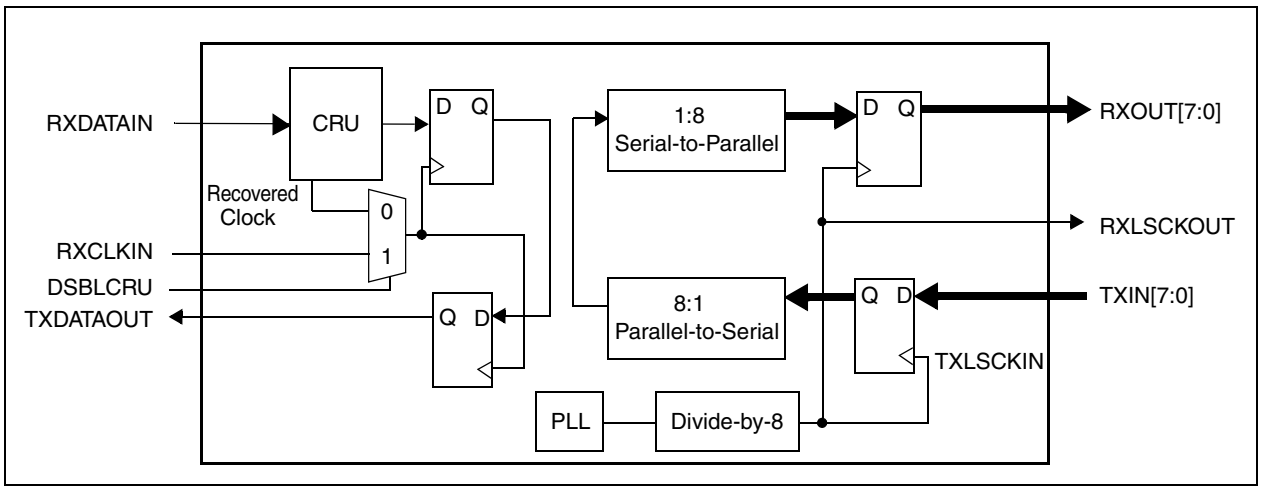


Figure 5. Split Loopback Data Path

Loop Timing

The LOOPTIM0 mode bypasses the CMU when the LOOPTIM0 input is asserted HIGH. In this mode, the CMU is bypassed by using the receive clock (RXCLKIN) and the entire part is synchronously clocked from a single external source.

Clock Synthesis

The VSC8117 uses an integrated PLL for clock synthesis of the 622MHz high-speed clock, which is used for serialization in the transmitter section. The PLL is comprised of a phase-frequency detector (PFD), an integrating operational amplifier, and a voltage-controlled oscillator (VCO) configured in classic feedback system. The PFD compares the selected divided-down version of the 622MHz VCO (CMUFREQSEL selects the divide-by ratios of 8 or 32—see Table 10 on page 14) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage-controlled ring-oscillator with a center frequency of 622MHz.

The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the CP1, CP2, CN1, and CN2 pins. The configuration of these external surface-mounted capacitors is shown in Figure 6.

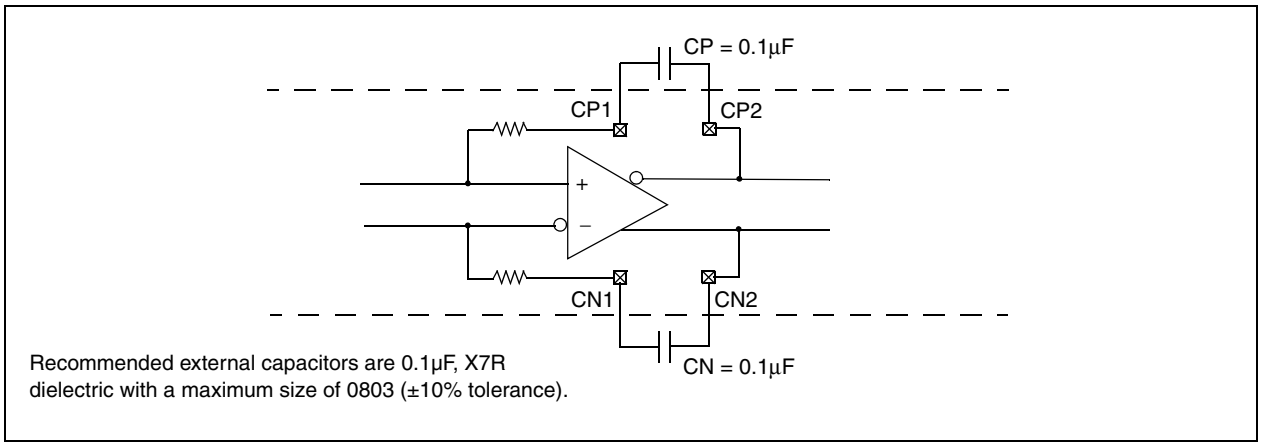


Figure 6. External Integrator Capacitor

Good analog design practices should be applied to the board design for these external components. Tightly-controlled analog ground and power planes should be provided for the PLL portion of the circuitry. The dedicated PLL power (VDDA) and ground (VSSA) pins should have quiet supply planes to minimize jitter generation within the clock synthesis unit and can be accomplished by using either a ferrite bead or a C-L-C choke (π filter) on the (VDDA) power pins. All ground planes should be tied together using multiple vias.

Reference Clocks

To improve jitter performance and to provide flexibility, an additional differential PECL reference clock input is provided. This reference clock is internally XNORed with a TTL reference clock input to generate the reference for the CMU. Vitesse recommends using the differential PECL input and tying the unused TTL reference clock LOW. If the TTL reference clock is used, the positive side of the differential PECL reference clock, REFCLKP+, should be tied to ground. REFCLKP± is internally biased with on-chip resistors to 1.65V.

The CRU has the option of either using the CMU's reference clock or its own independent reference clock, CRUREFCLK, and is selected with the control signal CRUREFSEL. The CRUREFCLK should be used if the system is being operated in either a regeneration or loop timing mode. In either of these modes, the quality of the CRUREFCLK is not a concern, therefore, it can be driven by a simple 77.76MHz crystal—the key is its independence of the CMU's reference clock.

Clock Recovery

The fully monolithic CRU consists of a phase detector, a frequency detector, a loop filter, and a VCO. The phase detector compares the phase information of the incoming data with the recovered clock. The frequency detector compares the frequency component of the data input with the recovered clock to provide the pull-in energy during lock acquisition. The loop filter integrates the phase information from the phase and frequency detectors and provides the control voltage to the VCO.

Jitter Tolerance

Jitter tolerance is the ability of the CRU to track timing variation in the received data stream. The Bellcore and ITU specifications allow the received optical data to contain jitter. The amount that must be tolerated is a function of the frequency of the jitter. At high frequencies, the specifications do not require the CRU to tolerate large amounts, whereas at low frequencies, many unit intervals (bit times) of jitter have to be tolerated. The CRU is designed to tolerate this jitter with margin over the specification limits. See Figure 7. Based on the data transition information, the CRU obtains and maintains lock. When there is no transition on the data stream, the recovered clock frequency can drift. The VSC8117 can maintain lock over 100 bits of no switching on data stream.

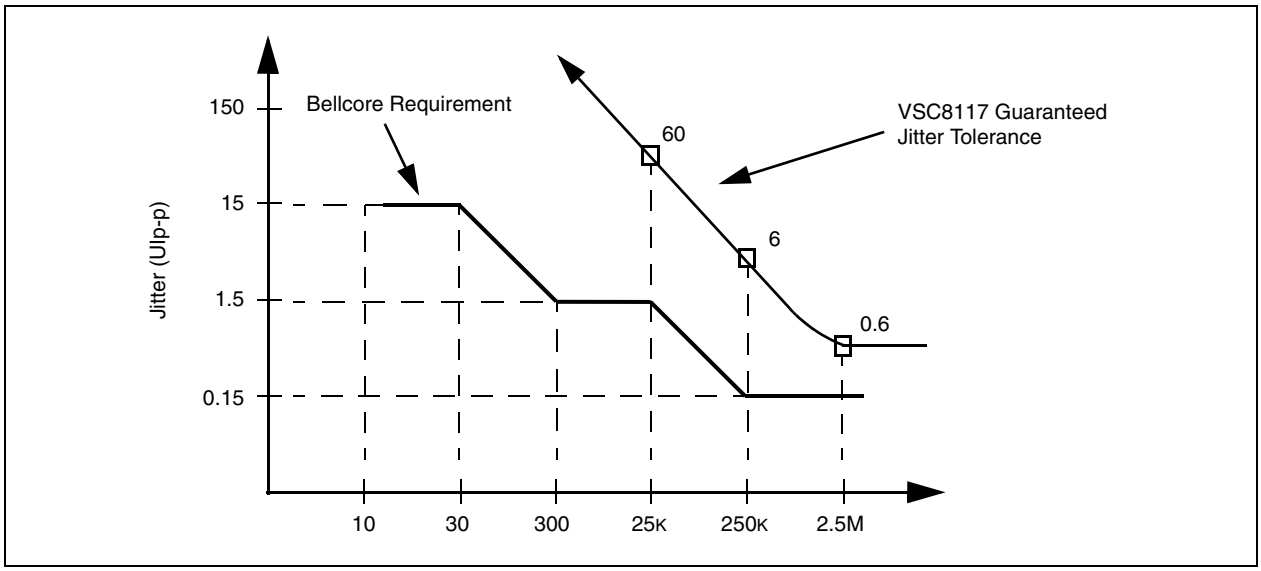


Figure 7. Jitter Tolerance

ELECTRICAL SPECIFICATIONS

AC Characteristics

Over recommended operating conditions.

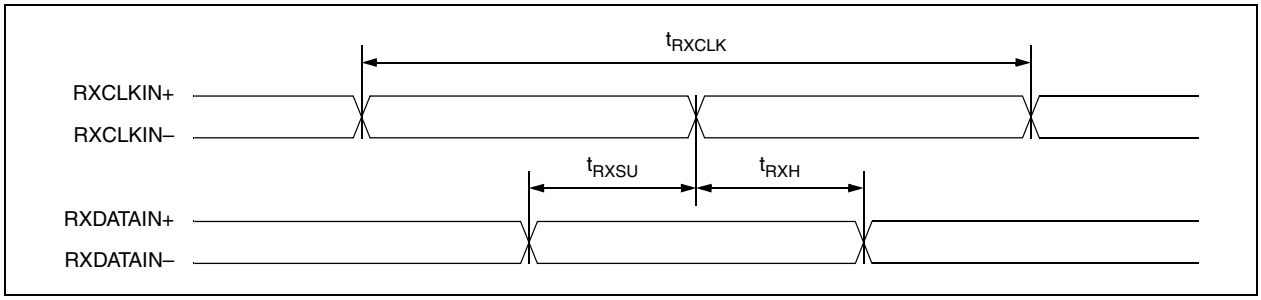


Figure 8. Receive High-Speed Data Input Timing Diagram

Table 1. Receive High-Speed Data Input Timing (STS-12 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{RXCLK}	Receive clock period		1.608		ns	
t_{RXSU}	Serial data setup time with respect to RXCLKIN	400			ps	
t_{RXH}	Serial data hold time with respect to RXCLKIN	100			ps	

Table 2. Receive High-Speed Data Input Timing (STS-3 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{RXCLK}	Receive clock period		6.43		ns	
t_{RXSU}	Serial data setup time with respect to RXCLKIN	1.5			ps	
t_{RXH}	Serial data hold time with respect to RXCLKIN	1.5			ps	

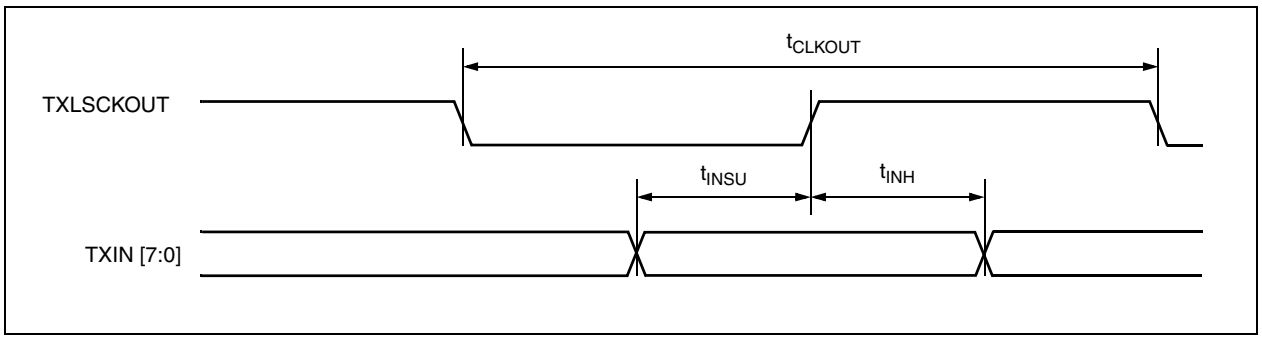


Figure 9. Transmit Data Input Timing Diagram

Table 3. Transmit Data Input Timing (STS-12 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{CLKOUT}	Transmit data output byte clock period		12.86		ns	
t_{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0			ns	
t_{INH}	Transmit data hold time with respect to TXLSCKOUT(1)	1.0			ns	
t_{TDT}	Clock falling edge to data transition Keep-Out Zone	–0.4		2.0	ns	

1. Worst-case duty cycle for TXLSCKOUT is 50% ±10%.

Table 4. Transmit Data Input Timing (STS-3 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{CLKOUT}	Transmit data output byte clock period		51.44		ns	
t_{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0			ns	
t_{INH}	Transmit data hold time with respect to TXLSCKOUT(1)	1.0			ns	

1. Worst-case duty cycle for TXLSCKOUT is 50% ±10%.

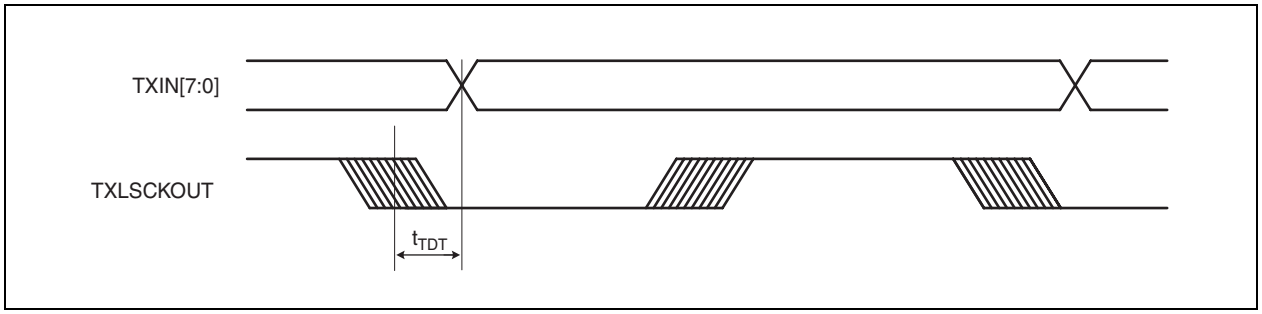


Figure 10. TXLSCKOUT Falling Edge Keep-Out Zone

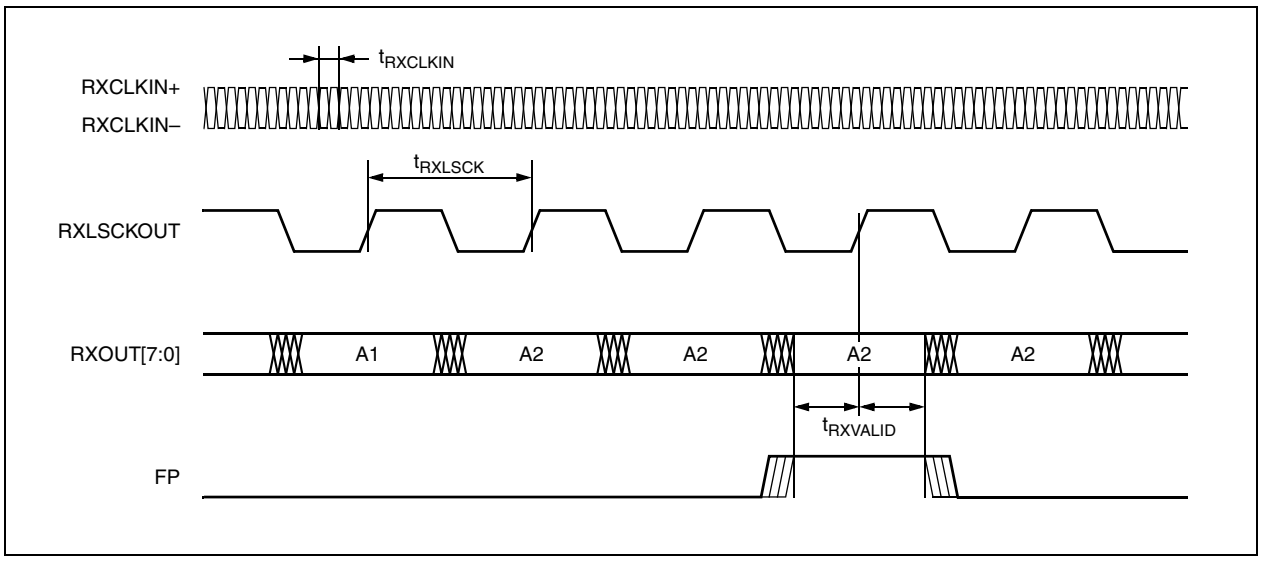


Figure 11. Receive Data Output Timing

Table 5. Receive Data Output Timing (STS-12 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
$t_{RXCLKIN}$	Receive clock period		1.608		ns	
t_{RXLSCK}	Receive data output byte clock period		12.86		ns	
$t_{RXVALID}$	Time the data is valid on RXOUT[7:0] and FP before and after the rising edge of RXLSCKOUT	4.0			ns	
t_{PW}	Pulse width of frame detection pulse on FP		12.86		ns	

Table 6. Receive Data Output Timing (STS-3 Operation)

Symbol	Parameter	Min	Typ	Max	Units	Condition
$t_{RXCLKIN}$	Receive clock period		6.43		ns	
t_{RXLSCK}	Receive data output byte clock period		51.44		ns	
$t_{RXVALID}$	Time the data is valid on RXOUT[7:0] and FP before and after the rising edge of RXLSCKOUT	22			ns	
t_{PW}	Pulse width of frame detection pulse on FP		51.44		ns	

Table 7. PECL and TTL Receive Outputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{R_TTL}	TTL output rise time		2		ns	10% to 90%.
t_{F_TTL}	TTL output fall time		1.5		ns	10% to 90%.
t_{R_PECL}	PECL output rise time		350		ps	20% to 80%.
t_{F_PECL}	PECL output fall time		350		ps	20% to 80%.

Data Latency

The VSC8117 contains several operating modes, each of which exercises different logic paths through the device. Table 8 bounds the data latency through each path with an associated clock signal.

Table 8. Data Latency

Circuit Mode	Description	Clock Reference	Range of Clock Cycles
Receive	MSB at RXDATAIN to data on RXOUT[7:0]	RXCLKIN	25 to 35
Facilities Loopback	MSB at RXDATAIN to MSB at TXDATAOUT	RXCLKIN	2 to 4

Clock Recovery Unit

Table 9. Reference Frequency for the CRU

CRUREFSEL	STS12	CRUREFCLK Frequency (MHz)	Output Frequency (MHz)
1	1	77.76 ±500ppm	622.08
1	0	77.76 ±500ppm	155.52
0	Uses CMU's Reference Clock (see Table 10 on page 14)		

Clock Multiplier Unit

Table 10. Reference Frequency Selection and Output Frequency Control

STS12	CMUFREQSEL	Reference Frequency (MHz)	Output Frequency (MHz)
1	1	19.44	622.08
1	0	77.76	622.08
0	1	19.44	155.52
0	0	77.76	155.52

Table 11. Clock Multiplier Unit Performance

Name	Parameter	Min	Typ	Max	Units
RC_D	Reference clock duty cycle	40		60	%
RC_J	Reference clock jitter (rms) at 77.76MHz reference(1)			13	ps
RC_J	Reference clock jitter (rms) at 19.44MHz reference(1)			5	ps
RC_F	Reference clock frequency tolerance(2)	–20		20	ppm
OC_J	Output clock jitter (rms) at 77.76MHz reference(3)			8	ps
OC_J	Output clock jitter (rms) at 51.84MHz reference(3)			10	ps
OC_J	Output clock jitter (rms) at 38.88MHz reference(3)			13	ps
OC_J	Output clock jitter (rms) at 19.44MHz reference(3)			15	ps
OCf_{RANGE}	Output frequency	620		624	MHz
OC_D	Output clock duty cycle	40		60	%
RC_D	Reference clock duty cycle	40		60	%

Jitter specification is defined using a 12kHz to 5MHz LP-HP single-pole filter.

1. *These reference clock jitter limits are required for the outputs to meet SONET system level jitter requirements (<10 mUIrms).*
2. *Required to meet SONET output frequency stability requirements.*
3. *Transmit and receive data must be synchronous with each other.*

DC Characteristics

Over Recommended Operating Conditions.

Table 12. PECL and TTL Inputs/Outputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{OH}	Output HIGH voltage (PECL)			V_{DDP} – 0.9V	V	
V_{OL}	Output LOW voltage (PECL)	0.7			V	
V_{OCM}	Output common-mode range (PECL)	1.1		V_{DDP} – 1.3V	V	
ΔV_{OUT75}	Differential output voltage (PECL)	600		1300	mV	75Ω to V_{DDP} – 2.0V.
ΔV_{OUT50}	Differential output voltage (PECL)	600		1300	mV	50Ω to V_{DDP} – 2.0V.
V_{IH}	Input HIGH voltage (PECL)	V_{DDP} – 0.9V		V_{DDP} – 0.3V	V	For single-ended.
V_{IL}	Input LOW voltage (PECL)	0		V_{DDP} – 1.72V	V	For single-ended.
ΔV_{IN}	Differential input voltage (PECL)	400		1600	mV	
V_{ICM}	Input common-mode range (PECL)	1.5 – $\Delta V_{IN}/2$		V_{DDP} – 1.0 – $\Delta V_{IN}/2$	V	
V_{OH}	Output HIGH voltage (TTL)	2.4			V	I_{OH} = –1.0mA.
V_{OL}	Output LOW voltage (TTL)			0.5	V	I_{OL} = 1.0mA.
V_{IH}	Input HIGH voltage (TTL)	2.0		5.5	V	
V_{IL}	Input LOW voltage (TTL)	0		0.8	V	
I_{IH}	Input HIGH current (TTL)		50	500	µA	2.0V< V_{IN} < 5.5V, typical at 2.4V.
I_{IL}	Input LOW current (TTL)			–500	µA	–0.5V < V_{IN} < 0.8V.

Table 13. Power Supply Currents

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{DD}	Power supply current from V_{DD}			500	mA	
P_D	Power dissipation			1.7	W	

Recommended Operating Conditions

Table 14. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{DD}	Power supply voltage	3.135	3.3	3.465	V	
V_{DDP}	PECL I/O power supply voltage for 3V operation	3.135	3.3	3.465	V	
V_{DDP}	PECL I/O power supply voltage for 5V operation	4.75	5.0	5.25	V	
T	Operating temperature range under bias(1)					
	VSC8117QP and VSC8117XQP	0		70	°C	
	VSC8117QP1 and VSC8117XQP1	0		115	°C	
	VSC8117QP2 and VSC8117XQP2	–40		85	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Power supply voltage, potential to GND	–0.5	4.0	V
V_{DDP}	PECL I/O power supply voltage, potential to GND	–0.5	6.0	V
	DC input voltage (PECL inputs)	–0.5	V_{DDP} + 0.5	V
	DC input voltage (TTL inputs)	–0.5	5.5	V
	DC output voltage (TTL outputs)	–0.5	V_{DD} + 0.5	V
	Output current (TTL outputs)	–50	50	mA
	Output current (PECL outputs)	–50	50	mA
T_C	Case temperature under bias	–55	125	°C
T_S	Storage temperature	–65	150	°C
V_{ESD}	ESD (Human Body Model)	–250	250	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

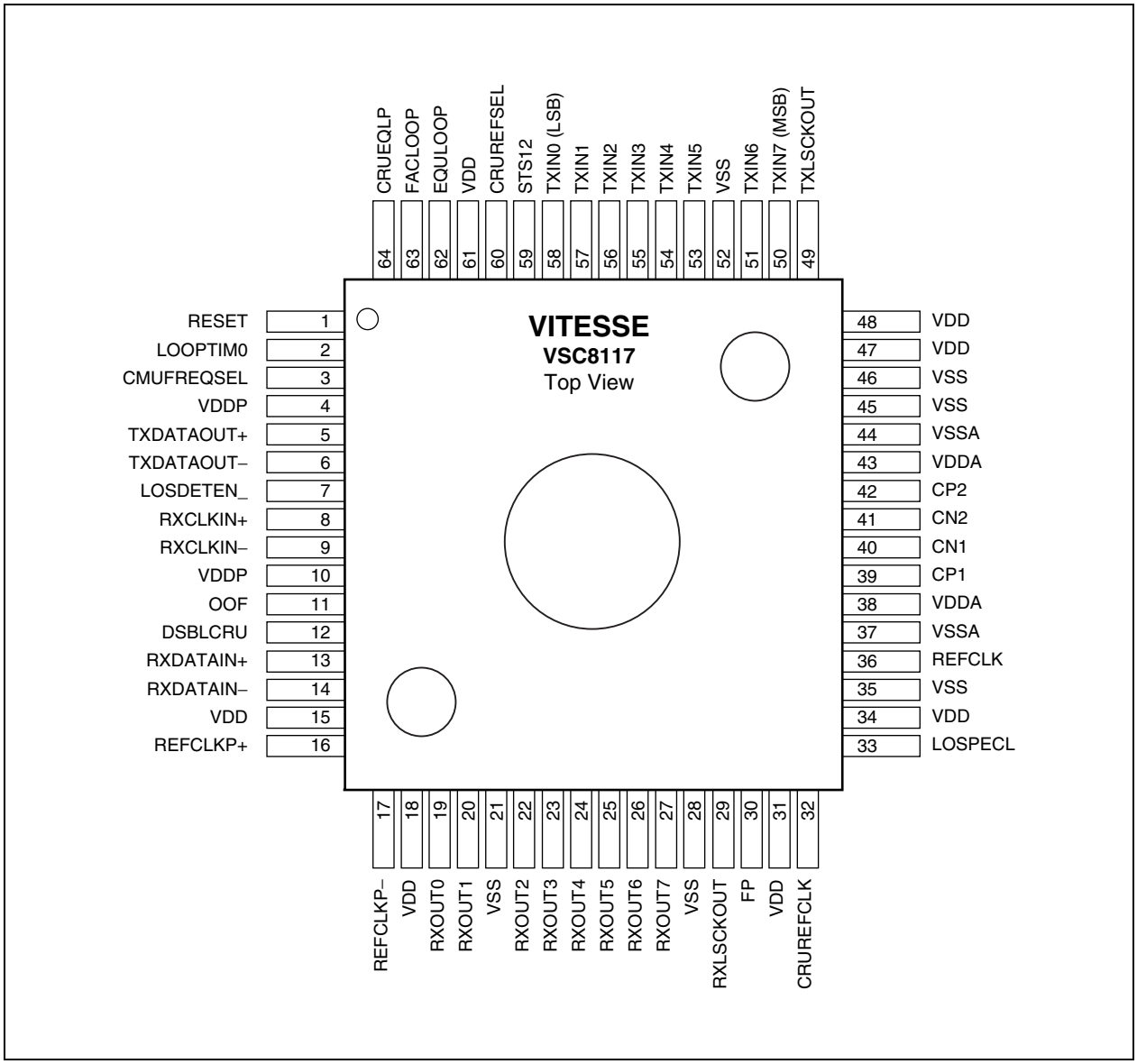


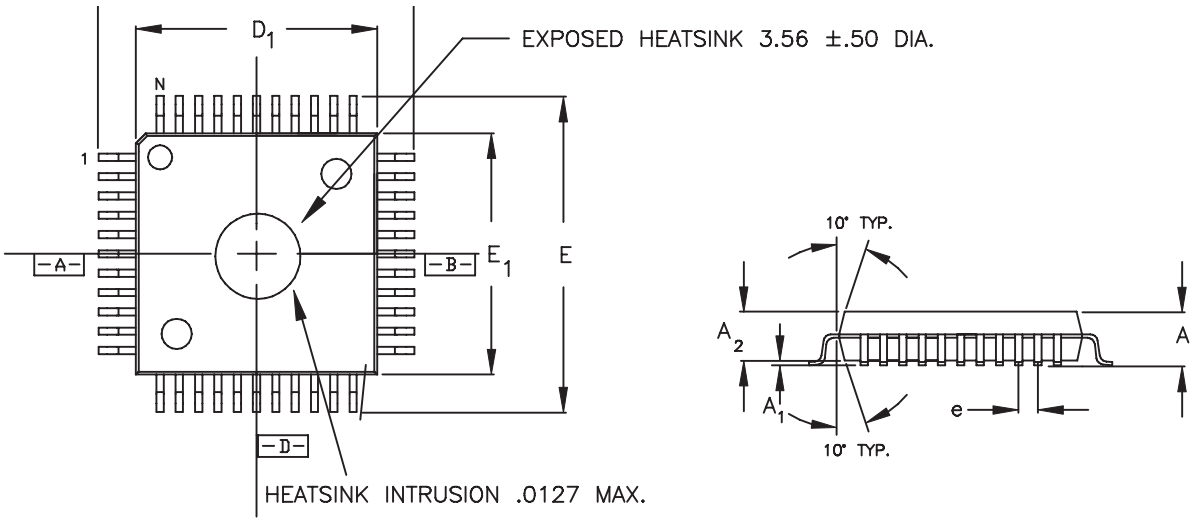
Figure 12. Pin Diagram

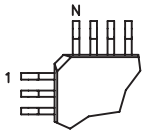
Table 16. Pin Identifications

Pin Number	Signal	I/O	Level	Description
1	RESET	I	TTL	Resets frame detection, dividers, and controls. Active HIGH.
2	LOOPTIM0	I	TTL	Enables loop timing operation. Active HIGH.
3	CMUFREQSEL	I	TTL	Reference clock frequency select. See Table 10 on page 14.
4	VDDP		Power	3.3V or 5V power supply for PECL I/Os.
5	TXDATAOUT+	O	PECL	Transmit output, high-speed differential data, true.
6	TXDATAOUT–	O	PECL	Transmit output, high-speed differential data, complement.
7	LOSDETEN_	I	TTL	Enables internal LOS detection. Active LOW.
8	RXCLKIN+	I	PECL	Receive high-speed differential clock input, true.
9	RXCLKIN–	I	PECL	Receive high-speed differential clock input, complement.
10	VDDP		Power	3.3V or 5V power supply for PECL I/Os.
11	OOF	I	TTL	Out Of Frame; frame detection initiated with high level.
12	DSBLCRU	I	TTL	Disables on-chip CRU. Active HIGH.
13	RXDATAIN+	I	PECL	Receive high-speed differential data input, true.
14	RXDATAIN–	I	PECL	Receive high-speed differential data input, complement.
15	VDD		Power	3.3V power supply.
16	REFCLKP+	I	PECL	PECL reference clock input, true.
17	REFCLKP–	I	PECL	PECL reference clock input, complement.
18	VDD		Power	3.3V power supply.
19	RXOUT0	O	TTL	Receive output data, bit 0.
20	RXOUT1	O	TTL	Receive output data, bit 1.
21	VSS		GND	Ground.
22	RXOUT2	O	TTL	Receive output data, bit 2.
23	RXOUT3	O	TTL	Receive output data, bit 3.
24	RXOUT4	O	TTL	Receive output data, bit 4.
25	RXOUT5	O	TTL	Receive output data, bit 5.
26	RXOUT6	O	TTL	Receive output data, bit 6.
27	RXOUT7	O	TTL	Receive output data, bit 7.
28	VSS		GND	Ground.
29	RXLSCKOUT	O	TTL	Receive byte clock output.
30	FP	O	TTL	Frame detection pulse.
31	VDD		Power	3.3V power supply.
32	CRUREFCLK	I	TTL	Optional external CRU reference clock at 77.76MHz.
33	LOSPECL	I	PECL	Loss of Signal Control. Single-ended PECL input, active LOW.
34	VDD		Power	3.3V power supply.
35	VSS		Power	Ground.
36	REFCLK	I	TTL	Reference clock input. See Table 10 on page 14.
37	VSSA		Power	Analog ground (CMU).
38	VDDA		Power	3.3V analog power supply (CMU).
39	CP1		Analog	CMU external capacitor (see Figure 6).
40	CN1		Analog	CMU external capacitor (see Figure 6).

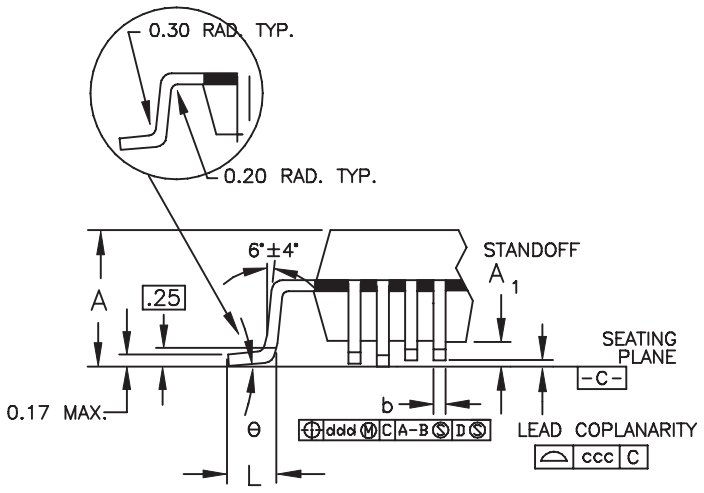
Table 16. Pin Identifications (continued)

Pin Number	Signal	I/O	Level	Description
41	CN2		Analog	CMU external capacitor (see Figure 6).
42	CP2		Analog	CMU external capacitor (see Figure 6).
43	VDDA		Power	3.3V analog power supply (CRU).
44	VSSA		Power	Analog ground (CRU).
45	VSS		Power	Ground.
46	VSS		Power	Ground.
47	VDD		Power	3.3V power supply.
48	VDD		Power	3.3V power supply.
49	TXLSCKOUT	O	TTL	Transmit byte clock out.
50	TXIN7	I	TTL	Transmit input data, bit 7, MSB.
51	TXIN6	I	TTL	Transmit input data, bit 6.
52	VSS		Power	Ground.
53	TXIN5	I	TTL	Transmit input data, bit 5.
54	TXIN4	I	TTL	Transmit input data, bit 4.
55	TXIN3	I	TTL	Transmit input data, bit 3.
56	TXIN2	I	TTL	Transmit input data, bit 2.
57	TXIN1	I	TTL	Transmit input data, bit 1.
58	TXIN0	I	TTL	Transmit input data, bit 0, LSB.
59	STS12	I	TTL	155Mb/s or 622Mb/s mode select. See Table 10 on page 14.
60	CRUREFSEL	I	TTL	Selects between CMU's or CRU's REFCLK.
61	VDD		Power	3.3V power supply.
62	EQULOOP	I	TTL	Equipment Loopback. Loops low-speed byte wide transmit input data to the receive output bus.
63	FACLOOP	I	TTL	Facility Loopback. Loops high-speed receive data and clock directly to the transmit outputs.
64	CRUEQLP	I	TTL	Loops TXDATAOUT to the CRU replacing RXDATAIN±.





ANOTHER VARIATION OF PIN 1 VISUAL AID



Dimensional References
64-pin PQFP, thermally-enhanced package
10mm x 10mm x 2.0mm body

Dimension	Min	Typ	Max
A			2.45
A_1	0.25		0.50
A_2	1.95	2.00	2.10
D	12.95	13.20	13.45
D_1	9.90	10.00	10.10
E	12.95	13.20	13.45
E_1	9.90	10.00	10.10
L	0.78	0.88	1.03
e		0.50 BSC	
b	0.17	0.22	0.27
θ		0° – 7°	
ddd			0.08
ccc			0.08

NOTES:
1. All dimensions are in millimeters.
2. Foot length "L" is measured at gage plane, at 0.25 above the seating plane.

Figure 13. Package Drawing

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 17. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC8117QP	6.2	46	41	37.8
VSC8117XQP	6.2	46	41	37.8
VSC8117QP1	6.2	46	41	37.8
VSC8117XQP1	6.2	46	41	37.8
VSC8117QP2	6.2	46	41	37.8
VSC8117XQP2	6.2	46	41	37.8

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity Level

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

VSC8117 622Mb/s or 155Mb/s Transceiver Mux/Demux with CMU and CRU

Part Number	Description
VSC8117QP	64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: 0°C ambient to 70°C case
VSC8117XQP	Lead(Pb)-free, 64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: 0°C ambient to 70°C case
VSC8117QP1	64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: 0°C ambient to 115°C case
VSC8117XQP1	Lead(Pb)-free, 64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: 0°C ambient to 115°C case
VSC8117QP2	64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: –40°C ambient to 85°C case
VSC8117XQP2	Lead(Pb)-free, 64-pin PQFP, thermally enhanced, 10mm x 10mm x 2.0mm body Operating temperature range under bias: –40°C ambient to 85°C case

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