VITESSE

VSC7983
Datasheet

11.2 Gbps Electroabsorption Modulator Driver

FEATURES

- 5 V or –5.2 V power supply operation
- Selectable data retiming
- AC-coupled inputs
- Internally-stabilized modulation and bias outputs
- Excellent output return loss
- 300 mV differential data input sensitivity
- Programmable output data eye crossing point

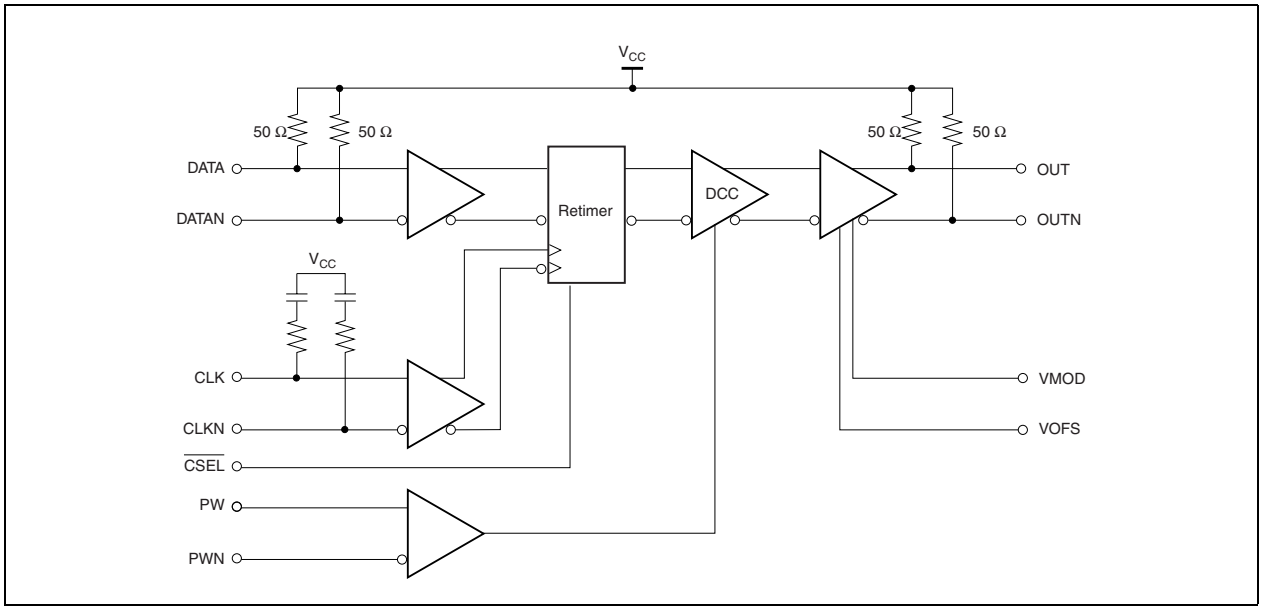
APPLICATIONS

- SONET OC-192 and SDH STM-64 transmission systems up to 11.2 Gbps
- 10 GbE modules
- VSR modules
- Fiber optic transponder and transceiver modules
- SONET/SDH test equipment

GENERAL DESCRIPTION

The VSC7983 device is a 11.2 Gbps electroabsorption modulator driver for SONET/SDH and 10 GbE applications. The device provides selectable data retiming to improve jitter performance and controls for output bias voltage, modulation voltage, and duty cycle. Internal operational amplifiers preclude the need for additional off-chip circuitry. The unique architecture of the VSC7983 device provides excellent output impedance which improves the match between the driver and load, further reducing output jitter. The VSC7983 device is available in a 32-pin *Micro*LeadFrame™ (MLF) package, a high performance 32-pin metal-glass QFP package, or in die form.

Block Diagram



Revision History

This section describes the changes that have been implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.2

Revision 4.2 of this datasheet was published on April 26, 2005. In revision 4.2 of the document, the package drawing for VSC7983CD was updated to include pre-dipped and solder-dipped specifications. For more information, see "Package Drawing for VSC7983CD," page 20.

Functional Description

The advantages of the VSC7983 device are its excellent output match, data retiming, internal stabilization of offset and modulation, and small package size. The VSC7983 device provides up to 3 V of output modulation swing and 1 V of voltage offset (or bias). The output compliance (the lowest achievable level of output swing) is better than 3.4 V for $V_{CC} - V_{EE} > 4.9$ V power supply.

The VSC7983 device has been characterized at 4.75 V to verify operation over power supply variations in 5 V systems. This reduction in power supply only affects the output voltage compliance and modulation limits. The reduced output voltage compliance (V_{OC}) is 3.3 V for modulation voltages (V_{OM}) of up to 2.8 V. The VSC7983 device is capable of moving the crossing point from the top to the bottom of the output eye. Specifications are guaranteed over all conditions for crossing points from 25% to 80%. For a crossing point from 25% to 85% the modulation voltage (V_{OM}) limit is reduced to 2.8 V. See Table 2 for these limitations.

The VSC7983 device inputs are to be AC-coupled and the outputs are to be DC-coupled. Information on AC-coupling the outputs is available. For assistance with this and other configurations, please contact your local Vitesse sales representative. Evaluation boards for all configurations and detailed supplemental information are also available.

Power Consumption

The VSC7983 device consumes 277 mA typical from a –5.2 V power supply and 300 mA maximum with a 2.5 V output swing and 1 V offset voltage. The following equation provides an estimation of worst-case power dissipation:

$$P_D = 5.5\ V \bullet (180\ mA + V_{OM}/25) \quad \textbf{(EQ 1)}$$

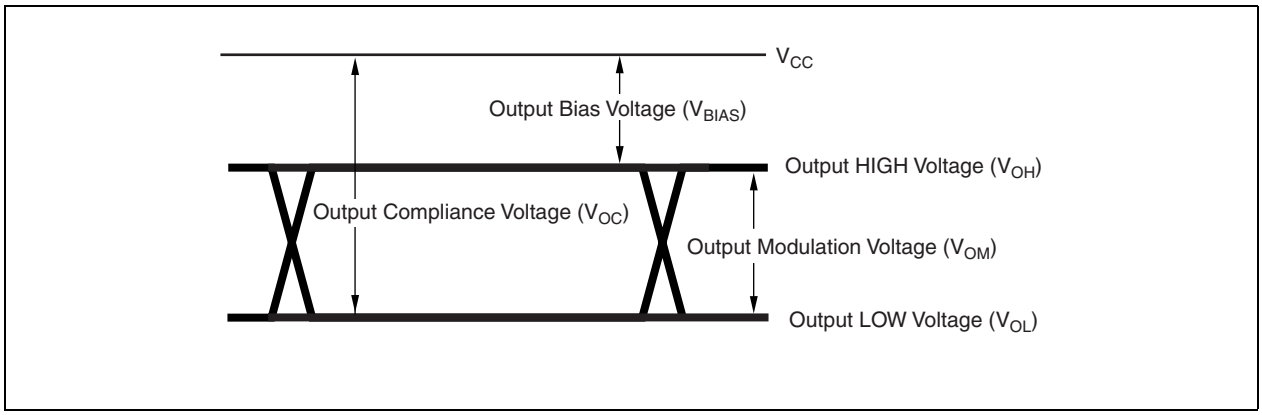


Figure 1. Output Voltage Range Specifications

Modulation, Bias, and Data Eye Crossing Point

Internal feedback stabilizes the VSC7983 device modulation and offset voltages. Therefore, no external operational amplifiers are required to stabilize modulation and bias currents. For optimal stability, it is recommended that a reference voltage relative to the most negative rail be used to set the VMOD and VOFS control voltages. The graphs below depict modulation, bias voltage and data eye crossing point range versus their control voltage. Figure 2, Figure 3, and Figure 4 show typical part-to-part variation as well as stability over temperature and power supply variation.

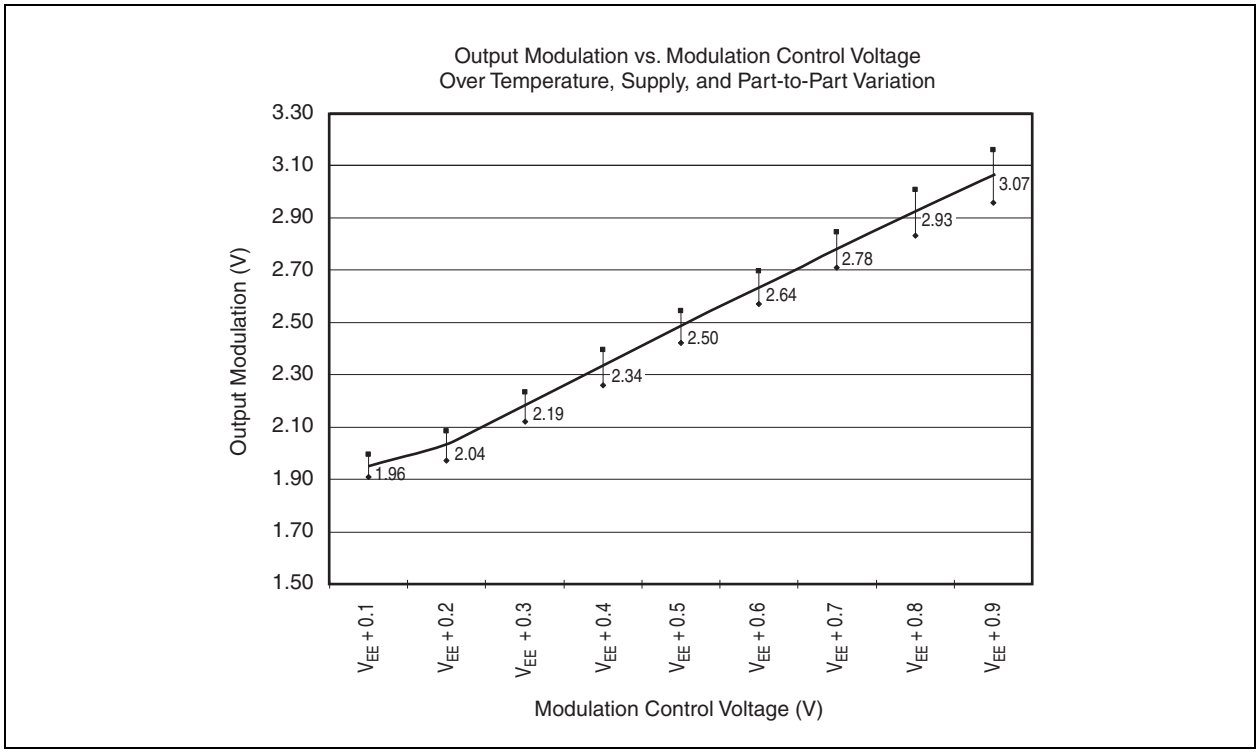


Figure 2. Modulation Range and Stability

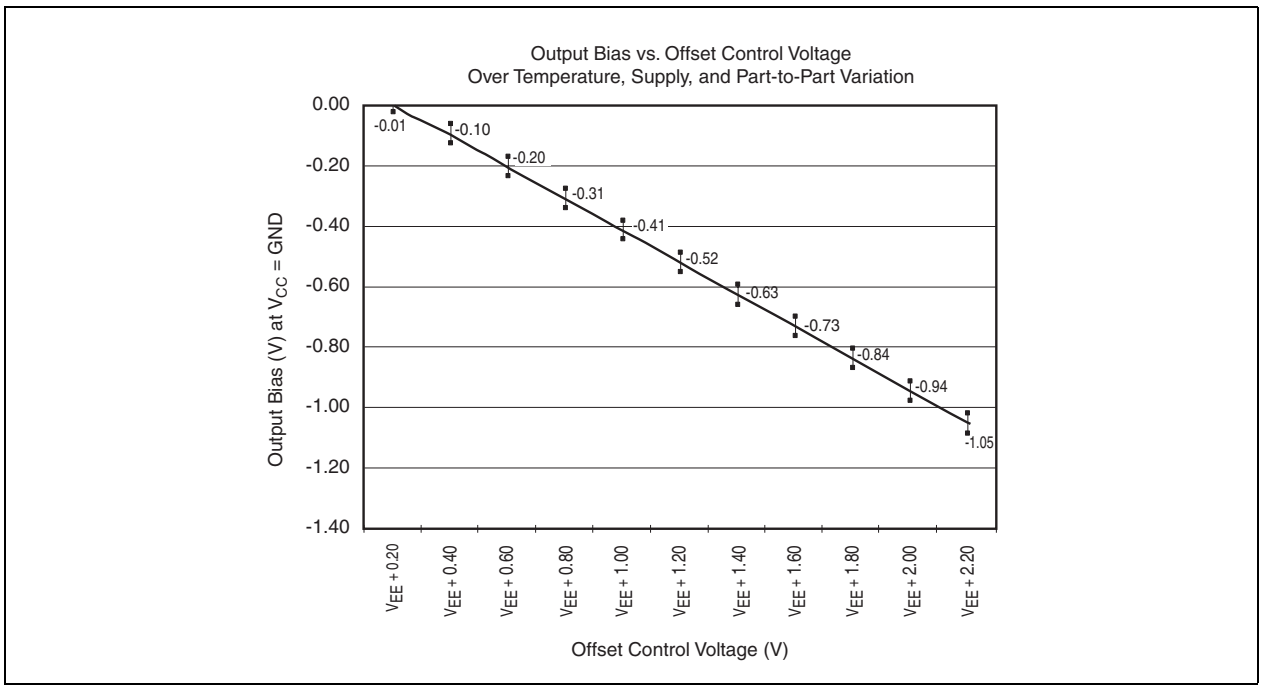


Figure 3. Bias Range and Stability

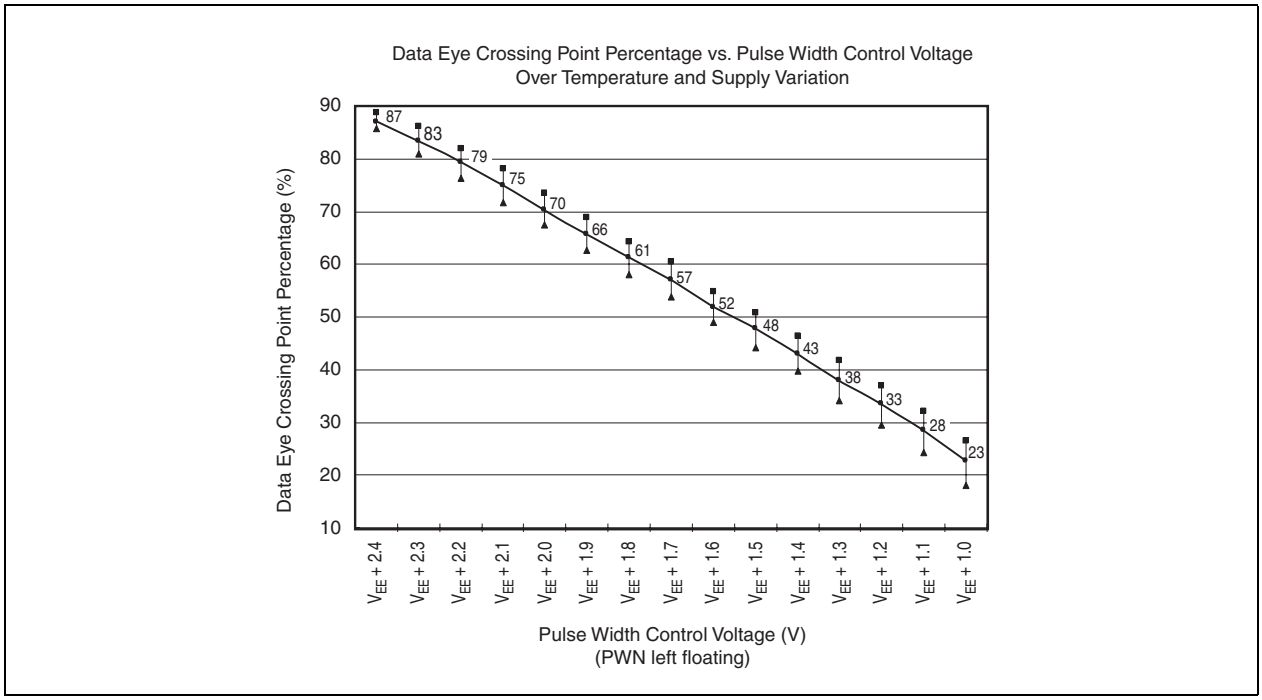


Figure 4. Data Eye Crossing Point Range and Stability

ELECTRICAL SPECIFICATIONS

This section contains the DC characteristics, AC characteristics, operating conditions, and maximum ratings for the VSC7983 device.

DC Characteristics

All parameters are guaranteed over temperature and supply with 11.2 Gbps PRBS $2^{31}-1$ pattern unless otherwise noted.

Table 1. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
$V_{CC} - V_{EE}$	Power supply voltage	4.75	5.0	5.5	V	
I_{EE}	Power supply current (nominal bias and modulation current)		277	300	mA	$V_{MOD} = V_{EE} + 0.5$ V. $V_{OFS} = V_{EE} + 2.0$ V. $V_{OM} = 2.5$ V, $V_{BIAS} = 1$ V.
$P_{DNOMINAL}$	Power dissipation (nominal bias and modulation current)		1440	1650	mW	$V_{MOD} = V_{EE} + 0.5$ V. $V_{OFS} = V_{EE} + 2.0$ V. $V_{OM} = 2.5$ V, $V_{BIAS} = 1$ V.
I_Q	Quiescent power supply current		237	260	mA	$V_{MOD} = V_{EE}$, $V_{OFS} = V_{EE}$. $V_{OM} = 2$ V, $V_{BIAS} = 0$ V.
P_{DQ}	Quiescent power dissipation		1240	1430	mW	$V_{MOD} = V_{EE}$, $V_{OFS} = V_{EE}$. $V_{OM} = 2$ V, $V_{BIAS} = 0$ V.
V_{MOD}	Output modulation control voltage	V_{EE}		$V_{EE} + 1.0$	V	Output amplitude maximum at $V_{EE} + 1.0$ V, minimum at V_{EE}. See Figure 2.
V_{OFS}	Output offset control voltage for output bias	V_{EE}		$V_{EE} + 2.2$	V	No offset at V_{EE}; maximum offset at $V_{EE} + 2.2$ V. See Figure 3.
V_{BIAS}	Output bias voltage	$V_{CC} - 1.0$		$V_{CC} - 0.1$	V	$R_L = 50\ \Omega$. See Figure 3.

AC Characteristics

This section contains the AC characteristics for the VSC7983 device.

Table 2. AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
f_{DATA}	Data rate		10.7	11.2	Gbps	NRZ.
f_{CLK}	Clock rate	1	10.7	11.2	GHz	
V_{IN}	Single-ended data input voltage amplitude	0.3		1.0	V	AC-coupled, peak-to-peak. See Figure 7.
	Differential data input voltage amplitude	0.3		1.0	V	AC-coupled, peak-to-peak (150 mV per side). See Figure 7.
V_{CLK}	Single-ended clock input voltage amplitude	0.4		1.0	V	AC-coupled, peak-to-peak. See Figure 7.
	Differential clock input voltage amplitude	0.4		1.0	V	AC-coupled, peak-to-peak (200 mV per side). See Figure 7.
V_{OC}	Output compliance voltage	–3.4			V	$V_{CC} - V_{EE} \geq 4.9$ V. $R_L = 50\ \Omega$ See Figure 1.
		–3.5			V	$V_{CC} - V_{EE} \geq 4.9$ V, $V_{OM} \leq 2.8$ V. $R_L = 50\ \Omega$. See Figure 1.
		–3.3			V	$V_{CC} - V_{EE} \geq 4.75$ V, $V_{OM} \leq 2.8$ V. $R_L = 50\ \Omega$. See Figure 1.
V_{OM}	Output voltage modulation	2		3	V	$R_L = 50\ \Omega$, $V_{CC} - V_{EE} \geq 4.9$ V. See Figure 2.
		2		2.8	V	$R_L = 50\ \Omega$, $V_{CC} - V_{EE} \geq 4.75$ V. See Figure 2.
t_R, t_F	Output rise time and fall time		28	35	ps	20% to 80%, $R_L = 50\ \Omega$.
DCC	Data eye crossing point range[1]	25		80	%	f_{DATA} = 10.7 Gbps data. See Figure 5 and Figure 4.
		25		85	%	f_{DATA} = 10.7 Gbps data, $V_{OM} \leq 2.8$ V. See Figure 5 and Figure 4. VSC7983CD only.
DCC_{STAB}	Data eye crossing point stability	–4		4	%	
V_{PW}	Pulse width control voltage[2]	V_{EE} + 0.7	V_{EE} + 1.5	V_{EE} + 2.4	V	See Figure 4.
–OVS, +OVS	Output under and overshoot	–10		10	%	$V_{OM} > 2$ V.
$\overline{CSEL}$	Clock select		Floating		V	Unclocked mode.
		V_{EE}		V_{EE} + 0.3	V	Clocked mode.
	Phase margin	270			degrees	
t_S	Set up time	–11			ps	See Figure 6. Differential clock input.
t_H	Hold time	25			ps	See Figure 6. Differential clock input.
J_{TOT_rms}	Total jitter, rms		1.6	3	ps	Clocked mode.
			2.1	5	ps	Unclocked mode.
$J_{TOT\_p\text{-}p}$	Total jitter, peak-to-peak		10	15	ps	Clocked mode.
			12	15	ps	Unclocked mode.

Table 2. AC Characteristics *(continued)*

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
S_{11}	Clock input return loss:					
	VSC7983-W		–22	–12	dB	1 GHz to 15 GHz.
	VSC7983CD		–9		dB	1 GHz to 15 GHz.
	VSC7983YE-02		–7		dB	1 GHz to 15 GHz.
S_{11}	Data input return loss:					
	VSC7983-W		–25	–15	dB	50 MHz to 10 GHz.
			–20	–12	dB	10 GHz to 15 GHz.
	VSC7983CD		–9		dB	50 MHz to 10 GHz.
			–9		dB	10 GHz to 15 GHz.
	VSC7983YE-02		–11		dB	50 MHz to 10 GHz.
			–7		dB	10 GHz to 15 GHz.
S_{22}	Data output return loss:					
	VSC7983-W		–16	–10	dB	50 MHz to 15 GHz, output = OFF.
			–10	–8	dB	50 MHz to 15 GHz, output = ON.
	VSC7983CD		–14		dB	50 MHz to 15 GHz, output = OFF.
			–9		dB	50 MHz to 15 GHz, output = ON.
	VSC7983YE-02		–7		dB	50 MHz to 15 GHz, output = OFF.
			–5		dB	50 MHz to 15 GHz, output = ON.

1. *VSC7983YE-02 output compliance V_{OC} is reduced to 3.1 V at DCC = 80%.*
2. *The VSC7983 device is capable of moving the data eye crossing point to the very top and bottom of the eye diagram.*

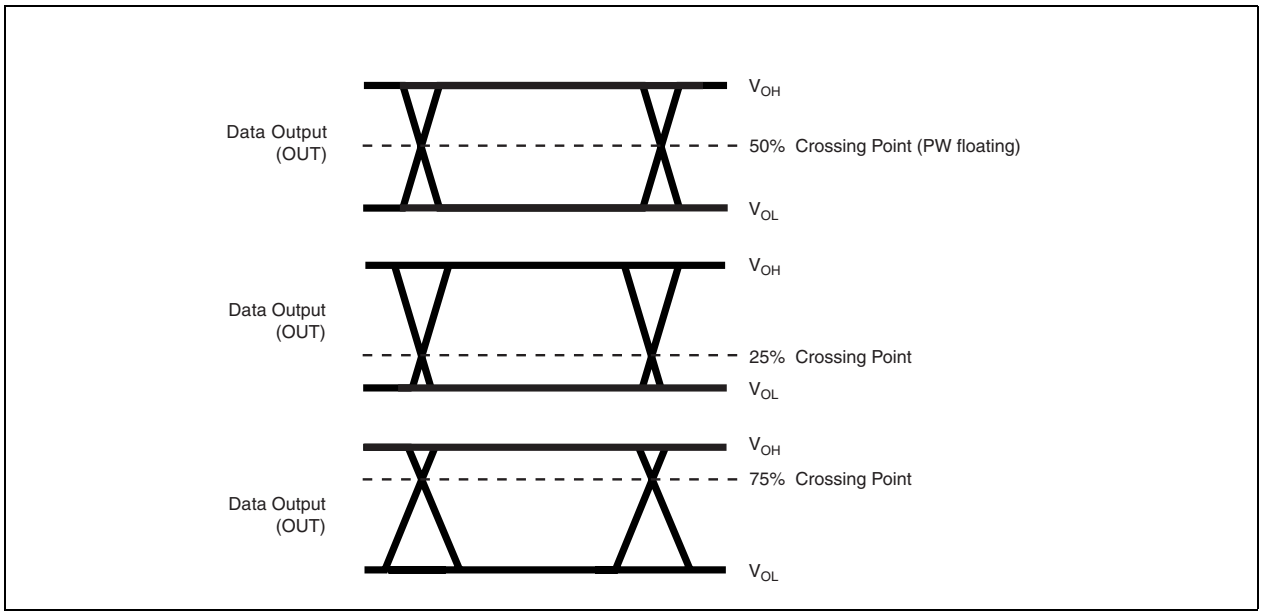


Figure 5. Data Eye Crossing Point Control Diagram

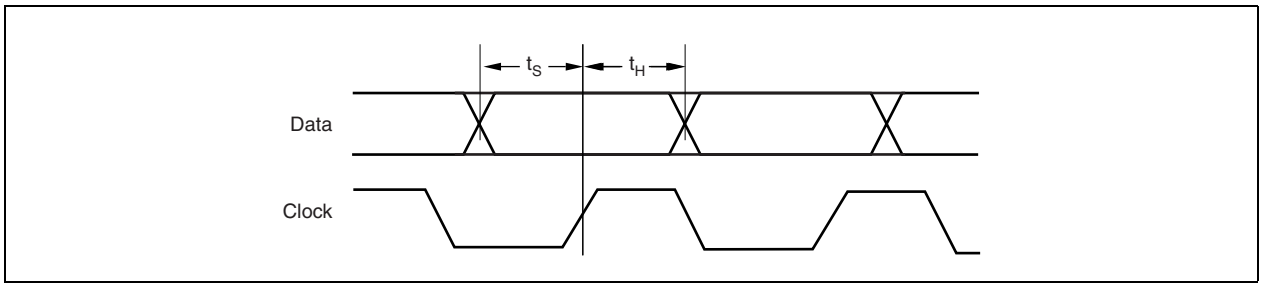


Figure 6. Set Up and Hold Timing Diagrams

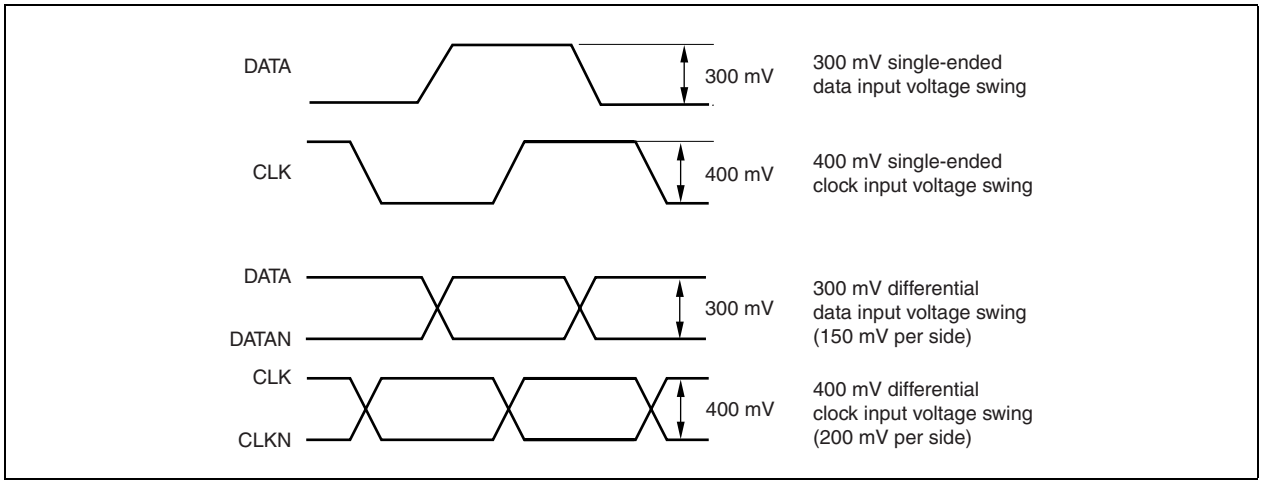


Figure 7. Input Voltage Swing Diagram

Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{CC}	Power supply voltage for positive supply operation		5.0		V	V_{EE} = GND
V_{EE}	Power supply voltage for negative supply operation		–5.2		V	V_{CC} = GND
T_B	Die backside temperature	0		100	°C	
T_J	Junction temperature	–10		125	°C	
T	Operating temperature(1)	–10		95	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Maximum Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
$V_{CC} - V_{EE}$	Power supply voltage	0	6	V
	All pins	V_{EE}	V_{CC} + 0.5	V
I_{EE}	Supply current		500	mA
V_{IN}, V_{CLK}	Input voltage	V_{CC} – 2	V_{CC} + 1	V
V_{OUT}	Output voltage		V_{CC} – 4	V
V_{MOD}	Output voltage modulation control voltage	V_{EE} – 0.5	V_{CC}	V
V_{OFS}	Output voltage offset control voltage	V_{EE} – 0.5	V_{CC}	V
V_{PW}	Pulse width control voltage	V_{EE}	V_{CC}	V
T_J	Junction temperature range	–40	140	°C
T_S	Storage temperature range	–55	140	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–400	400	V

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

TYPICAL OPERATING CHARACTERISTICS

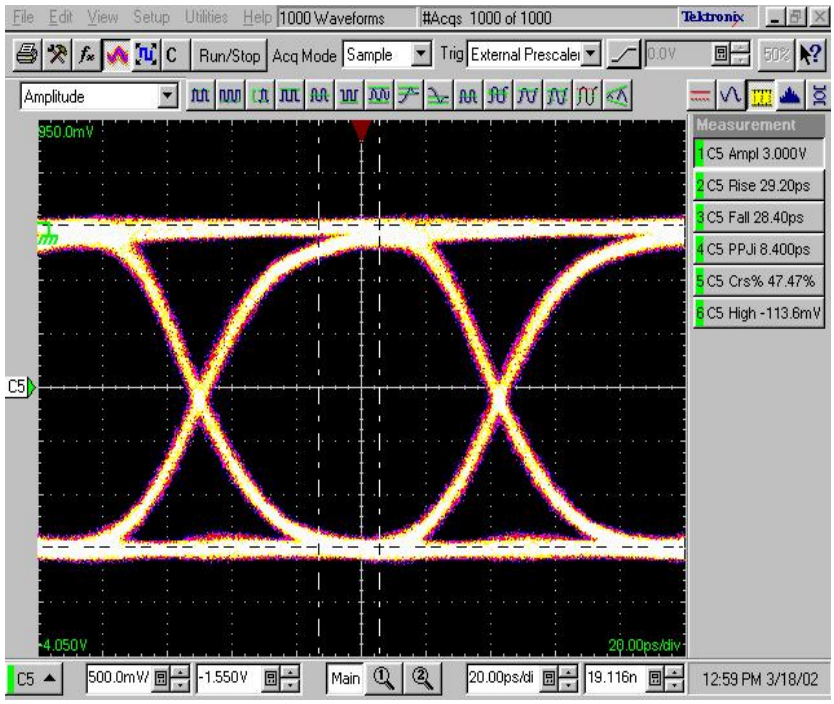


Figure 8. VSC7983-W: 3 V Swing Without Bias, Clocked

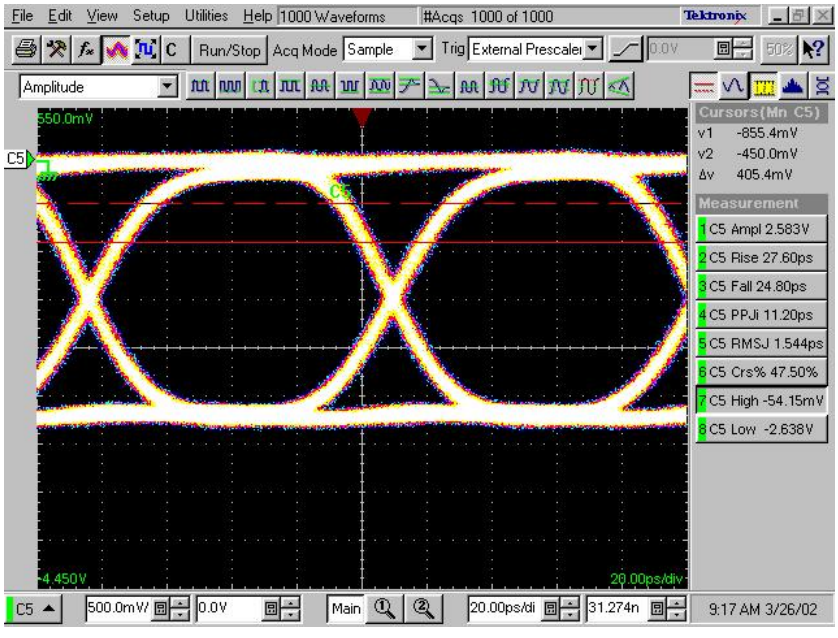


Figure 9. VSC7983CD: 2.5 V Swing Without Bias, Clocked

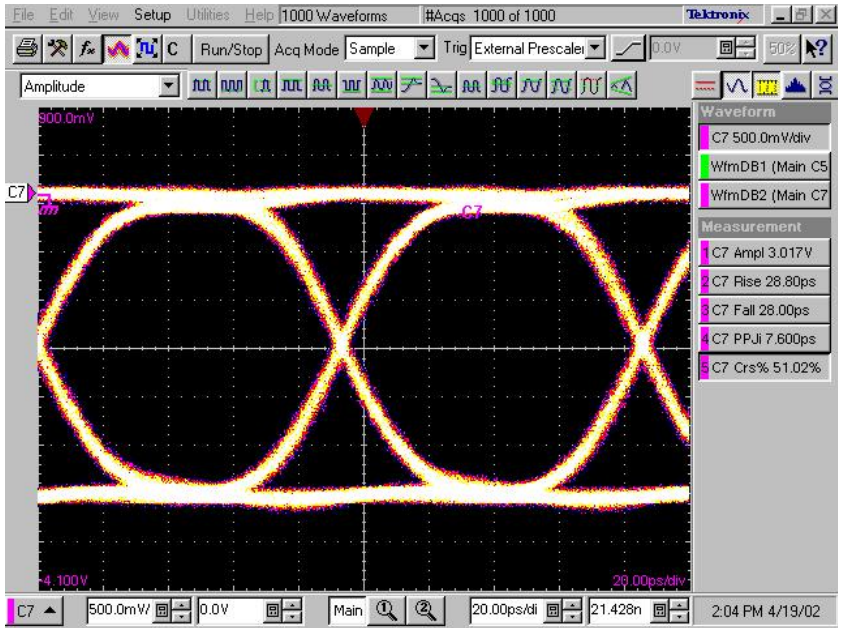


Figure 10. VSC7983CD: 3 V Swing Without Bias, Clocked

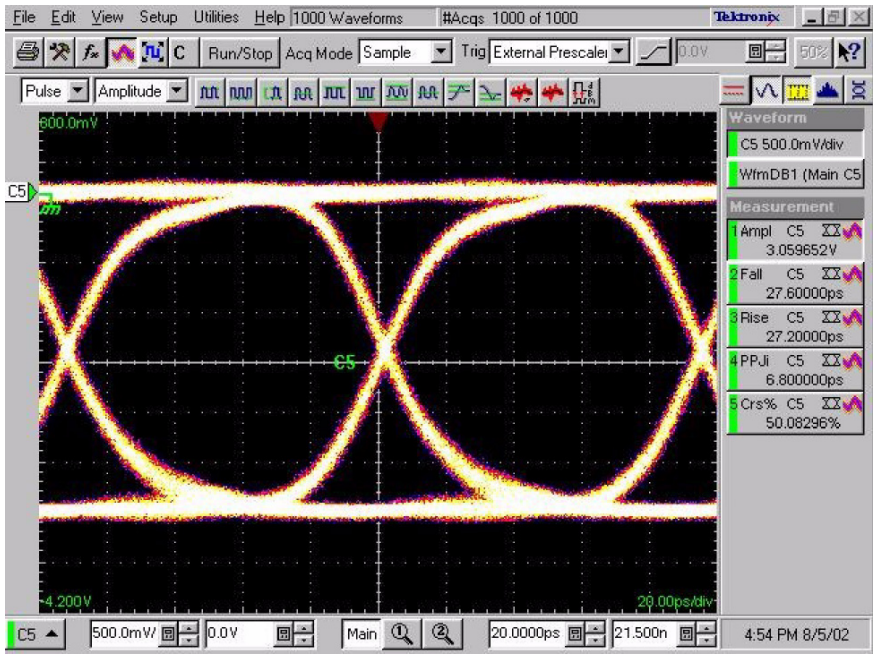
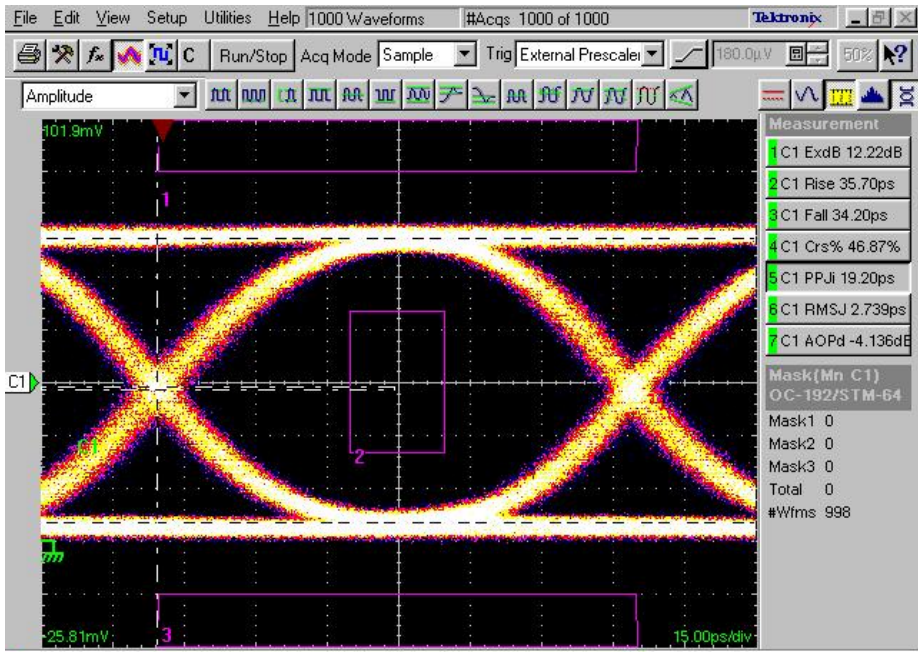


Figure 11. VSC7983YE-02: 3 V Swing Without Bias, Clocked

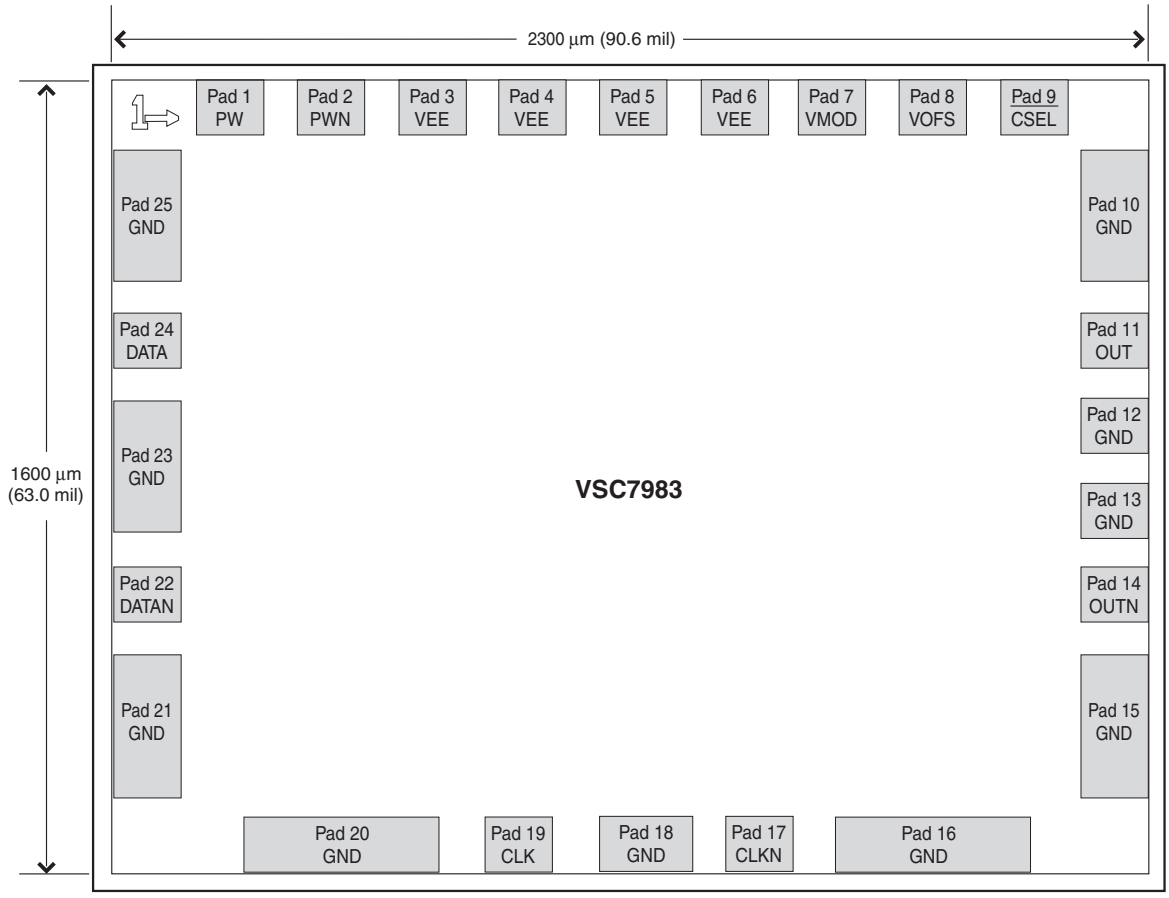


V_{EE} = –5.2 V, f = 10.7 GHz, NEL NLK3581SSI EML, 12.5 G Filter, 1000 Waveforms, PRBS 2^{23}–1
t_R = 36 ps, t_F = 34 ps, $J_{TOT\_p\text{-}p\text{-}}$ = 20 ps, Extinction Ratio = 12 dB

Figure 12. VSC7983CD: Optical, Nonclocked

BARE DIE AND PACKAGE INFORMATION

Pad Diagram for VSC7983-W



Die Size:	1600 µm x 2300 µm (63.0 mil x 90.6 mil)
Die Size Including Scribe:	1757 µm x 2457 µm (69.2 mil x 96.7 mil)
Die Thickness:	279 µm (11.0 mil)
Pad Passivation Opening:	85 µm x 85 µm (3.3 mil x 3.3 mil)
Pad Pitch:	125 µm (4.9 mil)

Die backside must be left floating or connected to most negative supply.

Figure 13. Pad Diagram for VSC7983-W

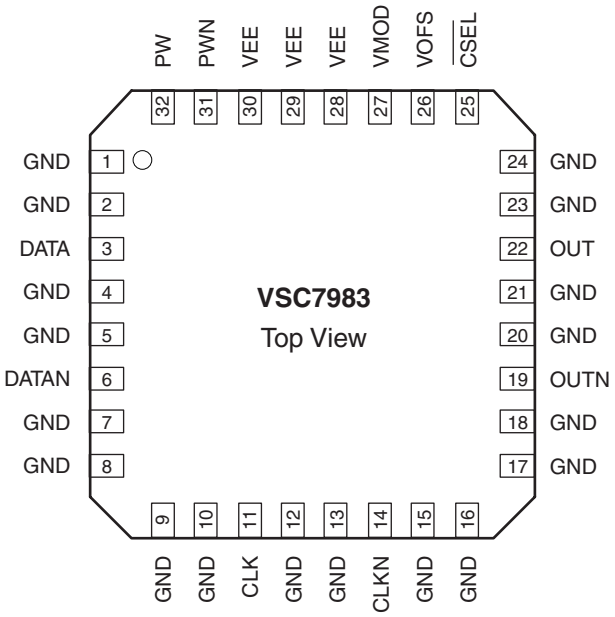
Pad Coordinates for VSC7983-W

Table 5. Pad Coordinates for VSC7983-W

Signal Name	Pad Number	Input/Output	Coordinates (µm)		Description
			X	Y	
PW	1	Input	350	1525	Pulse width control for data eye crossing point, true.
PWN	2	Input	550	1525	Pulse width control for data eye crossing point, complement.
VEE	3	Power	750	1525	Negative power supply.
VEE	4	Power	950	1525	Negative power supply.
VEE	5	Power	1150	1525	Negative power supply.
VEE	6	Power	1350	1525	Negative power supply.
VMOD	7	Input	1550	1525	Output modulation control. See Figure 2.
VOFS	8	Input	1750	1525	Output bias control. See Figure 3.
$\overline{\text{CSEL}}$	9	Input	1950	1525	Clock enable. For clock mode, connect to V_{EE}; for unclocked mode, leave floating.
GND	10	Power	2225	1300	Ground.
OUT	11	Output	2225	1050	Data output, true[1].
GND	12	Power	2225	875	Ground.
GND	13	Power	2225	725	Ground.
OUTN	14	Output	2225	550	Data output, complement.
GND	15	Power	2225	250	Ground.
GND	16	Power	1750	75	Ground.
CLKN	17	Input	1400	75	Clock input, complement.
GND	18	Power	1150	75	Ground.
CLK	19	Input	900	75	Clock input, true.
GND	20	Power	550	75	Ground.
GND	21	Power	75	250	Ground.
DATAN	22	Input	75	550	Data input, complement.
GND	23	Power	75	800	Ground.
DATA	24	Input	75	1050	Data input, true[1].
GND	25	Power	75	1350	Ground.

1. *A voltage HIGH on the data input (pad 24) corresponds to a voltage HIGH on the data output (pad 11).*

Pin Diagram for VSC7983YE-02



Exposed paddle must be connected to most negative rail or left floating. Heat must be removed through the printed circuit board (PCB).

Figure 14. Pin Diagram for VSC7983YE-02

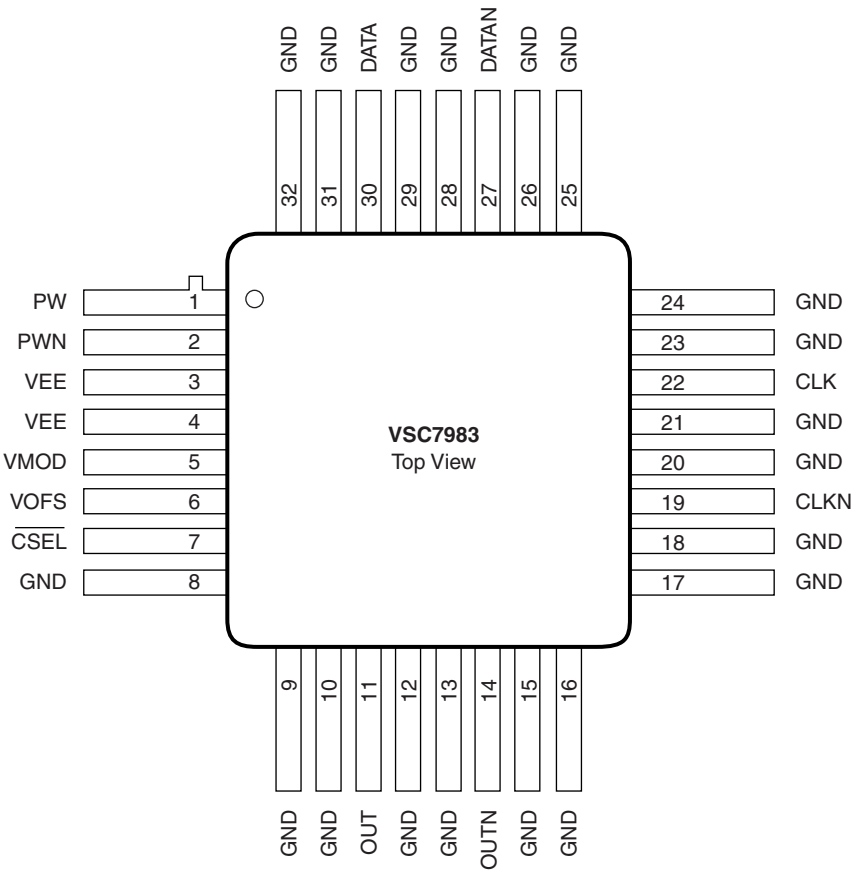
Pin Identifications for VSC7983YE-02

Table 6. Pin Identifications for VSC7983YE-02

Pin	Signal Name	Input/Output	Description
1	GND	Power	Ground.
2	GND	Power	Ground.
3	DATA	Input	Data input, true.
4	GND	Power	Ground.
5	GND	Power	Ground.
6	DATAN	Input	Data input, complement.
7	GND	Power	Ground.
8	GND	Power	Ground.
9	GND	Power	Ground.
10	GND	Power	Ground.
11	CLK	Input	Clock input, true.
12	GND	Power	Ground.
13	GND	Power	Ground.
14	CLKN	Input	Clock input, complement.
15	GND	Power	Ground.
16	GND	Power	Ground.
17	GND	Power	Ground.
18	GND	Power	Ground.
19	OUTN	Output	Data output, complement.
20	GND	Power	Ground.
21	GND	Power	Ground.
22	OUT	Output	Data output, true.
23	GND	Power	Ground.
24	GND	Power	Ground.
25	$\overline{\text{CSEL}}$	Input	Clock enable. For clock mode, connect to V_{EE}; for unclocked mode, leave floating.
26	VOFS	Input	Output bias control. See Figure 3.
27	VMOD	Input	Output modulation control. See Figure 2.
28	VEE	Power	Negative power supply.
29	VEE	Power	Negative power supply.
30	VEE	Power	Negative power supply.
31	PWN	Input	Pulse width control for data eye crossing point, complement.
32	PW	Input	Pulse width control for data eye crossing point, true.

1. *A voltage HIGH on the data input (pin 3) corresponds to a voltage HIGH on the data output (pin 22).*

Pin Diagram for VSC7983CD



NOTE: Heat should be removed through the top of the package. The top of the package should be connected to VEE or isolated. Connecting the package to GND will not damage but will degrade performance of the device.

Figure 15. Pin Diagram for VSC7983CD

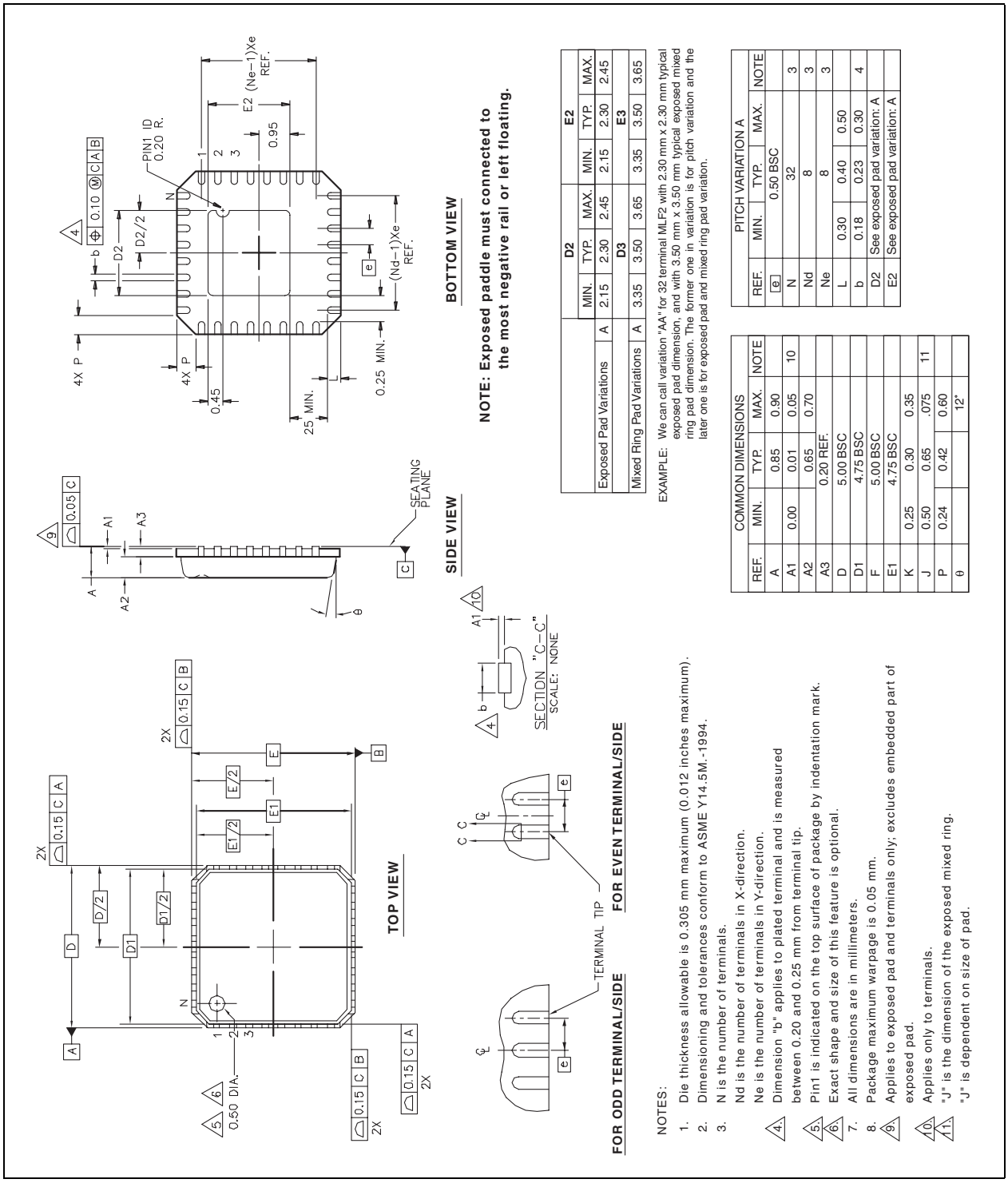
Pin Identifications for VSC7983CD

Table 7. Pin Identifications for VSC7983CD

Pin	Signal Name	Input/Output	Description
1	PW	Input	Pulse width control for data eye crossing point, true.
2	PWN	Input	Pulse width control for data eye crossing point, complement.
3	VEE	Power	Negative power supply.
4	VEE	Power	Negative power supply.
5	VMOD	Input	Output modulation control. See Figure 2.
6	VOFS	Input	Output bias control. See Figure 3.
7	$\overline{\text{CSEL}}$	Input	Clock enable. For clock mode, connect to V_{EE}; for unclocked mode, leave floating.
8	GND	Power	Ground.
9	GND	Power	Ground.
10	GND	Power	Ground.
11	OUT	Output	Data output, true.
12	GND	Power	Ground.
13	GND	Power	Ground.
14	OUTN	Output	Data output, complement.
15	GND	Power	Ground.
16	GND	Power	Ground.
17	GND	Power	Ground.
18	GND	Power	Ground.
19	CLKN	Input	Clock input, complement.
20	GND	Power	Ground.
21	GND	Power	Ground.
22	CLK	Input	Clock input, true.
23	GND	Power	Ground.
24	GND	Power	Ground.
25	GND	Power	Ground.
26	GND	Power	Ground.
27	DATAN	Input	Data input, complement.
28	GND	Power	Ground.
29	GND	Power	Ground.
30	DATA	Input	Data input, true.
31	GND	Power	Ground.
32	GND	Power	Ground.

1. *A voltage HIGH on the data input (pin 30) corresponds to a voltage HIGH on the data output (pin 11).*

Package Drawing for VSC7983YE-02



	D2			E2		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Exposed Pad Variations A	2.15	2.30	2.45	2.15	2.30	2.45
	D3			E3		
Mixed Ring Pad Variations A	3.35	3.50	3.65	3.35	3.50	3.65

EXAMPLE: We can call variation "AA" for 32 terminal MLF2 with 2.30 mm x 2.30 mm typical exposed pad dimension, and with 3.50 mm x 3.50 mm typical exposed mixed ring pad dimension. The former one in variation is for pitch variation and the later one is for exposed pad and mixed ring pad variation.

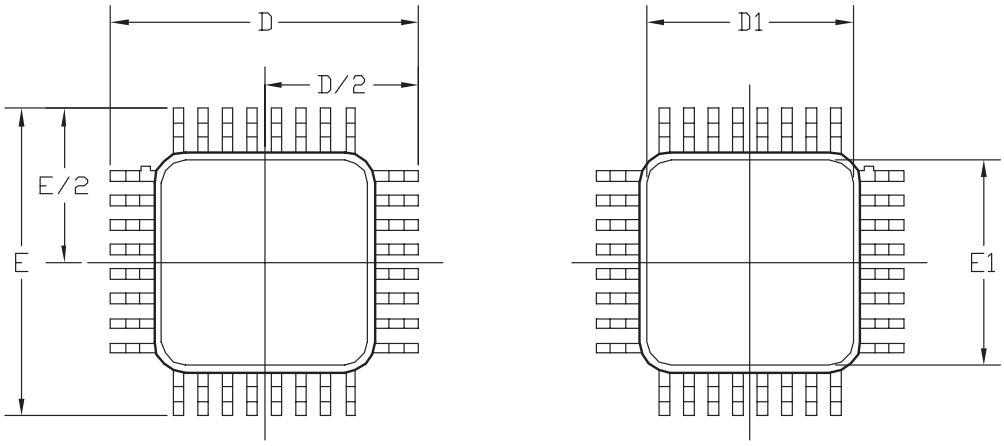
COMMON DIMENSIONS				
REF.	MIN.	TYP.	MAX.	NOTE
A		0.85	0.90	
A1	0.00	0.01	0.05	10
A2		0.65	0.70	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
F		5.00 BSC		
E1		4.75 BSC		
K	0.25	0.30	0.35	
J	0.50	0.65	.075	11
P	0.24	0.42	0.60	
θ			12°	

PITCH VARIATION A				
REF.	MIN.	TYP.	MAX.	NOTE
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	See exposed pad variation: A			
E2	See exposed pad variation: A			

NOTES:
1. Die thickness allowable is 0.305 mm maximum (0.012 inches maximum).
2. Dimensioning and tolerances conform to ASME Y14.5M.-1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction.
   Ne is the number of terminals in Y-direction.
4. Dimension "b" applies to plated terminal and is measured between 0.20 and 0.25 mm from terminal tip.
5. Pin1 is indicated on the top surface of package by indentation mark.
6. Exact shape and size of this feature is optional.
7. All dimensions are in millimeters.
8. Package maximum warpage is 0.05 mm.
9. Applies to exposed pad and terminals only; excludes embedded part of exposed pad.
10. Applies only to terminals.
11. "J" is the dimension of the exposed mixed ring.
    "J" is dependent on size of pad.

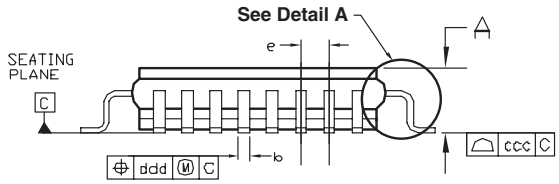
Figure 16. Package Drawing for VSC7983YE-02

Package Drawing for VSC7983CD

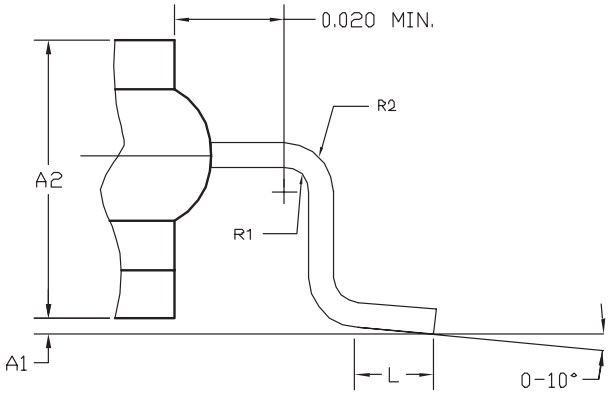


TOP VIEW

BOTTOM VIEW



SIDE VIEW



DETAIL A

Symbol	Tolerance	Dimension	
A	±0.011	0.054	
A1	+0.005 −0.003	0.003	
A2	Reference	0.051	
D	±0.010	0.321	
D1	±0.005	0.215	
E	±0.010	0.321	
E1	±0.005	0.215	
L	±0.005	0.0155	
e	Reference	0.0256	
b	±0.003	0.012	
ddd	Maximum	0.004	
ccc	Maximum	0.004 0.0045	Pre-dipped Solder-dipped
R1	±0.002	0.005	
R2	±0.002	0.005	

NOTES:
1. All dimensions in inches
2. Lead thickness : 0.006 ±0.003 (solder dipped)

Figure 17. Package Drawing for VSC7983CD

Package Thermal Considerations

A significant advantage of the VSC7983YE-02 is its small leadless package. The die is attached just above the package heat slug, therefore, the heat must be removed through the PCB. (Please contact your local Vitesse sale representative for detailed information on PCB design and thermal simulation.) The package heat slug must have a good thermal path to the PCB, meaning that either the package must be reflowed or epoxy must be carefully applied. For improved thermal performance, conductive epoxy is used to attach the heat slug, therefore, the heat slug is connected to the most negative rail (typically –5.2 V). It is recommended to connect the heat slug thermally and electrically to the PCB and to use as many vias as possible to connect to the backside of the PCB. If necessary, a thermally conductive and electrically insulating tape may be applied to the backside of the PCB to prevent shorts to ground. It is also recommended that the module case or heat sink be connected to this thermal tape. Thermal simulations indicate that the PCB backside be kept at 80°C to maintain quality operation and to guarantee recommended junction temperature. The VSC7983YE-02 is smaller and is lower cost than the VSC7983CD, but does not have the same caliber of performance. However, the VSC7983YE-02 produces a good quality optical data eye. See "Typical Operating Characteristics," page 10 for eye diagrams.

The VSC7983CD requires heat to be removed through the top of the package; the top of the package should not be connected to GND. Although this will not damage the device or reduce performance, it will unnecessarily draw higher power. It is recommended that thermally conductive, electrically insulating tape be used to connect the package to the heat sink or module case. The bottom of the package (the part that comes in contact with the board) is electrically insulated.

ORDERING INFORMATION

VSC7983 11.2 Gbps Electroabsorption Modulator Driver

Part Number	Description
VSC7983-W	Bare die, waffle pack
VSC7983YE-02	32-pin MLF package, 5 mm x 5 mm
VSC7983CD	32-pin metal-glass QFP package, 8.1 mm x 8.1 mm

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