VSC7177 Data Sheet

Enhanced 2:1 Port Selector for Serial ATA and Serial Attached SCSI

FEATURES

- 2:1 port selector for both Serial ATA (SATA) and Serial Attached SCSI (SAS) links
- Serial ATA 1.0 compliant at 1.5 Gbps (3.0 Gbps capable)
- Sideband port selection
- Complies with Serial ATA II: Port Selector specification 1.0, including failover control
- Passes Serial ATA patterns transparently
- Programmable receiver sensitivity
- High output swing mode with pre-emphasis
- Compatible with legacy designs (VSC7173 and VSC7175); provides enhanced connectivity and signal pre-emphasis
- 0.6 W to 0.8 W power dissipation (depending on operating mode)
- 3.3 V power supply
- 32-pin, 7 mm x 7 mm QFP-N package

APPLICATIONS

- Active-passive redundant failover systems
- Dual-port Serial ATA and Serial Attached SCSI disk arrays (JBODs)
- NAS servers
- RAID subsystems
- Disk-based backup systems
- Serial ATA and Serial Attached SCSI routing applications
- Buffers for externally connected links

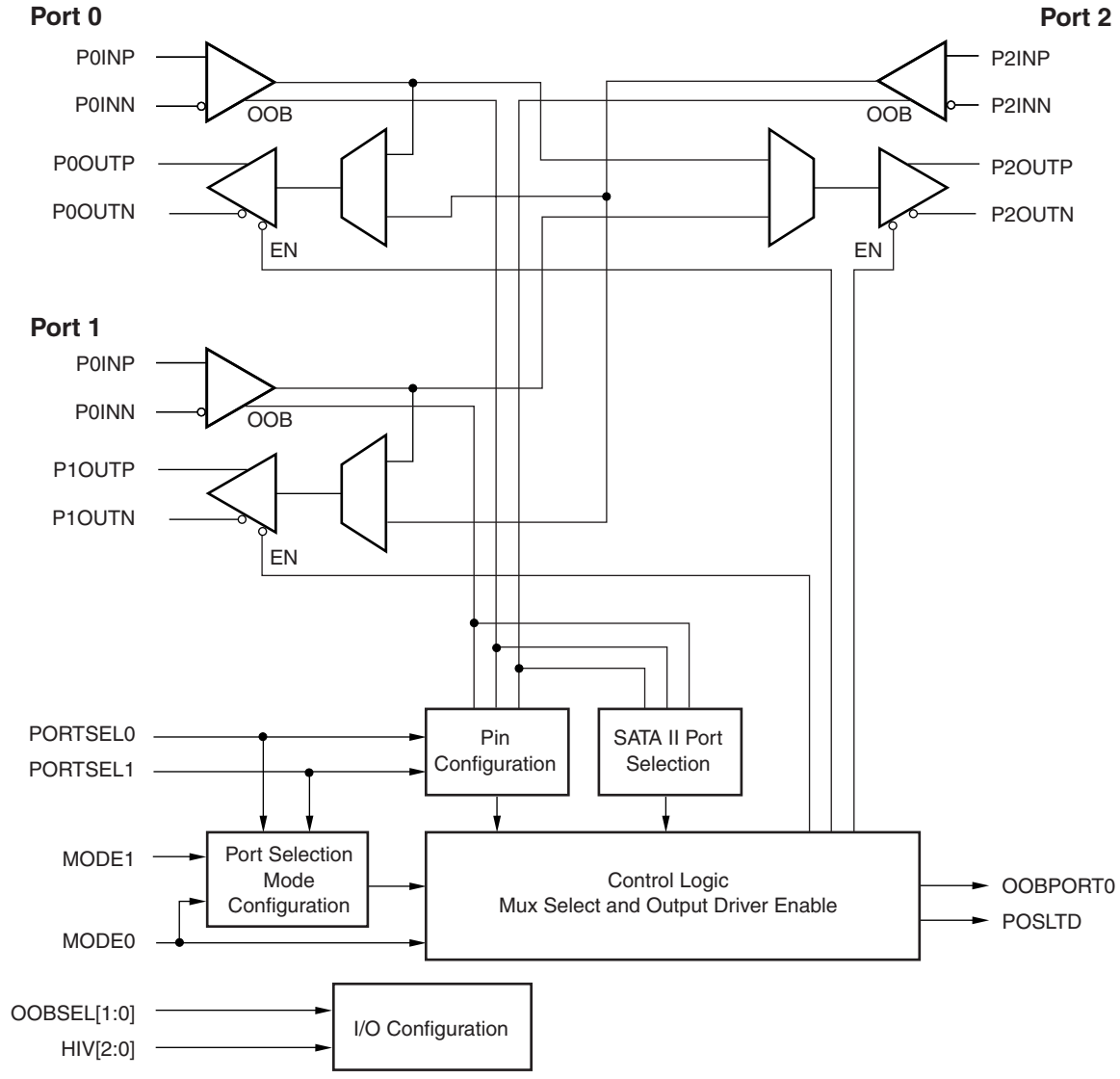
To order the VSC7177 device, see "Ordering Information," page 24.

GENERAL DESCRIPTION

The VSC7177 is a Serial ATA and Serial Attached SCSI multiplexer/buffer that implements a 2:1 port selector function for 1.5 Gbps and 3.0 Gbps links. This function is used when dual hosts, such as I/O controllers, must access single-port disk drives in high availability storage subsystems where redundancy and load sharing are important. The outputs from the I/O controllers are multiplexed to a Serial ATA or Serial Attached SCSI drive. The output from the Serial ATA drive is buffered and replicated to the I/O controllers. When switching from one I/O controller to the other, a Serial ATA link must be re-initialized with out-of-band (OOB) signals, which are transferred through the VSC7177 transparently. The VSC7177 provides high output swings, pre-emphasis, and programmable receiver sensitivity that are needed to drive long backplanes and external cables.

Port connectivity for the device can be configured using driving external I/O pins or through protocol-based port. See the block diagram on page 2.

VSC7177 Block Diagram



Application Example

The VSC7177 allows two Serial ATA hosts to access one Serial ATA drive. Figure 1 shows a common application where redundant I/O controllers in disk arrays have multiplexed access to single-port Serial ATA disk drives.

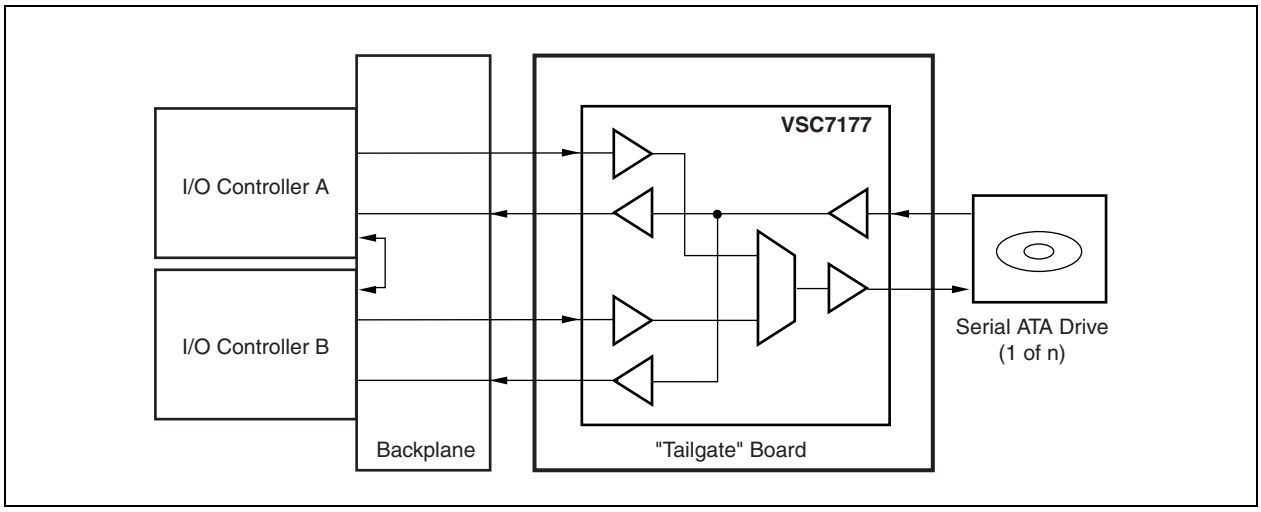


Figure 1. Serial ATA Backplane Application

REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.2

Revision 4.2 of this data sheet was published on July 29, 2005. In revision 4.2 of the document, information about the VSC7177XYI lead(Pb)-free device was added. For more information, see "Thermal Specifications," page 23 and "Ordering Information," page 24.

Revision 4.1

Revision 4.1 of this data sheet was published on November 16, 2004. In revision 4.1 of the document, differences for pin 9 between VSC7177, VSC7175, and VSC7173 were added. For VSC7177, pin 9 reports the OOB status for the unselected host port. For VSC7175, pin 9 reports the OOB status for Host A. For VSC7173, pin 9 reports the OOB status for Port 0.

Revision 4.0

Revision 4.0 of this data sheet was published on June 25, 2004. This was the first production-level publication of the document.

FUNCTIONAL DESCRIPTIONS

Modes of Operation

The VSC7177 has two modes of operation: sideband port selection and protocol port selection. Each mode corresponds to a different method of configuring port connectivity. Only one of the operating modes is active at any time in the VSC7177. Sideband-based port connectivity is controlled externally using the I/O pins of the device itself. Protocol-based connectivity is implemented as defined in the Serial ATA II: Port Selector 1.0 specification.

Selecting Operating Modes

There are two types of sideband-based port selections: Edge-sensitive and level-sensitive. Rising-edge transitions on the PORTSEL0 and PORTSEL1 inputs cause the corresponding port to become active when in edge-sensitive sideband-based selection mode. Edge-sensitive sideband port selection is enabled when MODE1 is HIGH.

PORTSEL0 determines the active port in level-sensitive sideband-based mode. Level-sensitive sideband port selection is enabled when MODE1 is LOW and PORTSEL1 is LOW.

Setting MODE1 LOW and PORTSEL1 HIGH in the VSC7177 allows the protocol-based Serial ATA II port selection and test modes to be enabled. PORTSEL0 and MODE0 are used to select these operating modes shown in Table 1. The functionality of the various operating modes is described in the following sections.

The setting of PORTSEL1 constitutes one of the primary differences between the VSC7177 and the VSC7173 and the VSC7175. In the VSC7177, PORTSEL1 must be set LOW in level-sensitive sideband mode. The setting of PORTSEL1 has no effect on the operation of the VSC7173 and the VSC7175 in level-sensitive mode (it is a “don’t care”). For a complete list of differences between the VSC7177 and the VSC7173 and the VSC7175, see “Pinout Differences Between VSC7177 and VSC7173/VSC7175,” page 13.

Table 1 shows how to configure the VSC7177 to operate in any of the various available modes.

Table 1. Operating Modes

Modes of Operation	Configuration Pins			
	MODE1	MODE0	PORTSEL0	PORTSEL1
Edge-sensitive sideband port selection	1	Select output mode of unconnected port	↑ edge makes port 0 active	↑ edge makes port 1 active
Level-sensitive sideband port selection	0	Select output mode of unconnected port	Selects connected port	0 (1)
Reserved	0	0	0	1
Test modes	0	0	1	1
Protocol-based Serial ATA II port selection	0	1	0	1
Test modes	0	1	1	1

X = don’t care; ↑ = rising.

1. *PORTSEL1* ***must*** *equal V_{SS} in level-sensitive sideband-based port selection mode. (The VSC7173 and the VSC7175 allow PORTSEL1 = X.)*

Sideband-Based Port Selection

External I/O pins are used to configure port connectivity when the sideband-based port selection modes are active. The protocol-based port selection mode is disabled when sideband-based port selection modes are enabled.

There are two sideband-based port selection operating modes. One mode selects the active port connected to port 2 based on the logical value of the PORTSEL0 input. Port 0 is the active port connected to port 2 when PORTSEL0 is LOW. Port 1 is the active port connected to port 2 when PORTSEL0 is HIGH. This level-sensitive sideband mode is enabled when MODE1 is LOW and PORTSEL1 is LOW. Note that the requirement to have PORTSEL1 LOW in level-sensitive sideband mode does not exist in the VSC7173 and VSC7175. For a complete list of differences between the VSC7177 and the VSC7173 and the VSC7175, see "Pinout Differences Between VSC7177 and VSC7173/VSC7175," page 13.

The other sideband-based mode chooses the active port connected to port 2 when rising edge transitions are detected on the PORTSEL0 and PORTSEL1 input pins. This edge-sensitive sideband-based mode is enabled when MODE1 is HIGH. Port 0 is selected as the active port connected to port 2 when a rising edge transition is detected on PORTSEL0. PORTSEL1 can be in a HIGH or LOW state during a transition of PORTSEL0. Port 1 is selected as the active port when a rising edge transition is detected on PORTSEL1. PORTSEL0 can be in a HIGH or LOW state during a transition of PORTSEL1. The VSC7177 grants access to the last PORTSELx signal that transitions from LOW to HIGH.

To allow redundant hosts to access single-port drives in edge-sensitive sideband port selection mode, two inputs, PORTSEL0 and PORTSEL1, control the multiplexer to the drive port and the enable signal to their output port. Because of this, each host needs to gain control of the VSC7177 if the other host fails. It is assumed that if a host fails, it will drive PORTSELx HIGH, LOW, or open, but that it will not be transitioning the signal. It is also assumed that the two hosts have a host-to-host communication path that allows them to agree which host should access the drive at any time. If the host at port 1 fails, the host at port 0 can regain access to the drive by first driving PORTSEL0 LOW, then driving it HIGH. Essentially, the last host to transition its PORTSELx signal from LOW to HIGH is granted access. This simple scheme ensures that a healthy host can always recover access to the drive at port 2 if the other host fails.

Status Signals—Sideband Mode

The P0SLTD output reports the OOB status of port 1 (OOBPORT1) when the device is in level-sensitive sideband-based port selection mode. The P0SLTD output indicates the active port when the device is in edge-sensitive sideband-based port selection mode. P0SLTD is LOW when port 1 is active and HIGH when port 0 is active.

The OOBPORT0 output reports the state of the OOB detector from port 0's input receiver. Table 2 contains a summary of this information. For more information about the OOBPORT0 and OOBPORT1 signals, see "OOB Transfer," page 12.

Table 2. Output Status in Sideband Port Selection Mode

Sideband Port Selection Mode	Port Connected (to Port 2)	Output Pins	
		P0SLTD	OOBPORT0
Level-sensitive	Port 0 or 1	OOBPORT1	OOBPORT0
Edge-sensitive	Port 0	1	OOBPORT0
Edge-sensitive	Port 1	0	OOBPORT0

Inactive Port Functionality

The MODE0 pin controls the functionality of the output driver for the unconnected port.

In both edge-sensitive and level-sensitive sideband modes, the output of the unconnected port (P0OUTP/N or P1OUTP/N) transmits port 2 input data when MODE0 is HIGH. The output driver transmits the data received by that unconnected port when MODE0 is LOW. Note that this loopback functionality differs from the VSC7173 and the VSC7175 in edge-sensitive sideband mode.

Table 3 summarizes the sideband-based port selection functionality.

Table 3. Sideband-based Port Selection Operating Modes

Input Pins				Output Pins			
MODE1	MODE0	PORTSEL0	PORTSEL1	P0OUT	P1OUT	P2OUT	P0SLTD
0 (level)	0	0	0 (1)	P2IN	P1IN	P0IN	OOBPORT1
0 (level)	0	1	0 (1)	P0IN	P2IN	P1IN	OOBPORT1
0 (level)	1	0	0 (1)	P2IN	P2IN	P0IN	OOBPORT1
0 (level)	1	1	0 (1)	P2IN	P2IN	P1IN	OOBPORT1
1 (edge)	0	X	↑	P0IN	P2IN	P1IN	0
1 (edge)	0	↑	X	P2IN	P1IN	P0IN	1
1 (edge)	1	X	↑	P2IN	P2IN	P1IN	0
1 (edge)	1	↑	X	P2IN	P2IN	P0IN	1

X = don't care; ↑ = rising.

1. *PORTSEL1* ***must*** *equal V_{SS} in level-sensitive sideband-based port selection mode. See Table 1, page 5.*

Reset State

The power-up state of the VSC7177 while in sideband-based port selection mode is based upon the PORTSEL0 and PORTSEL1 input signals. When in level-sensitive sideband mode, the active port connected to port 2 is controlled directly by the PORTSEL0 input. This is the same behavior as the normal operating condition described above. When in edge-sensitive sideband mode, the active port connected to port 2 is defined in Table 4. The state diagram in Figure 2 indicates the same result in a different format.

Table 4. Power-Up State (Edge-Sensitive Sideband Mode)

PORTSEL0	PORTSEL1	Active Port	P0SLTD Output
0	0	Port 0 selected	1
1	0	Port 0 selected	1
0	1	Port 1 selected	0
1	1	Port 0 selected	1

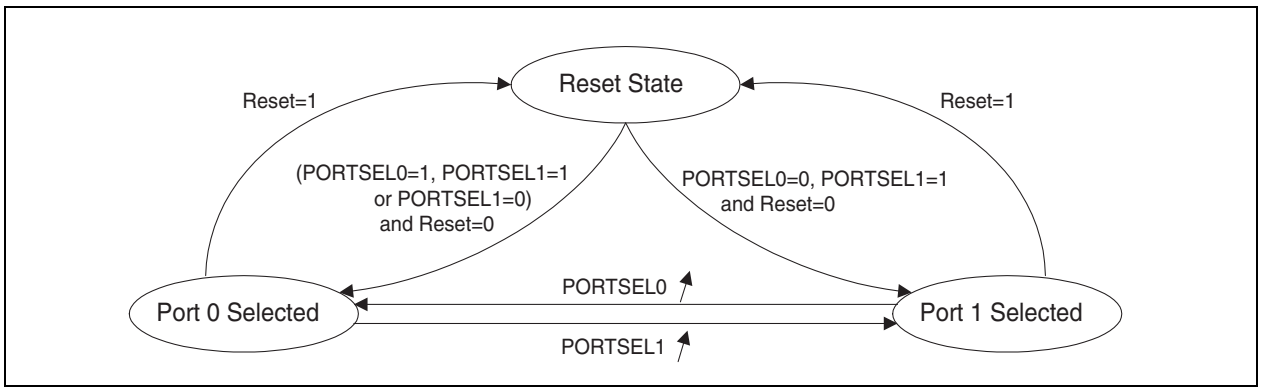


Figure 2. Reset State Machine (Edge-Sensitive Sideband Mode)

Serial ATA II Protocol-Based Port Selection

Protocol-based port selection allows two hosts to negotiate for connection to a single device using OOB signaling. The active host port in the VSC7177 may be selected using the protocol-based method defined in the Serial ATA II: Port Selector 1.0 specification. Protocol-based port selection determines whether port 0 or port 1 is the active host port connected to port 2 in this operating mode.

The Serial ATA II protocol-based port selection mode is enabled when MODE1 is LOW, MODE0 is HIGH, PORTSEL1 is HIGH, and PORTSEL0 is LOW. Sideband-based port selection is disabled when Serial ATA II protocol-based port selection mode is enabled.

Table 1, page 5 shows all modes of operation. This section describes how the Serial ATA II: Port Selector standard was implemented in the VSC7177.

Neither host port (port 0 or port 1) is active following power up and reset of the VSC7177. The output buffer in the device port (port 2) is disabled (output is at DC-bias point) when there is no active host port. Data received by the device port is transmitted to both host ports.

The VSC7177 supports presence detection per Serial ATA II: Port Selector 1.0 specification. A six-burst COMWAKE signal is transmitted from each host port immediately after power up. A six-burst COMWAKE signal is transmitted from a host port each time a valid COMRESET signal is received by that host port. The VSC7177 starts transmitting the COMWAKE signal after it has detected the COMRESET signal is no longer being received from the host. The COMWAKE signal is transmitted in response to receiving a COMRESET signal, regardless of that port's being active or inactive.

When there is no active host port, the first COMWAKE or COMRESET signal received by a host port selects that port as the active host port. A COMRESET signal is transmitted out of the device port to the device, and the now active host port is connected to the device port. If a COMWAKE or COMRESET signal is received by both host ports simultaneously, port 0 is given priority and is selected as the active host port.

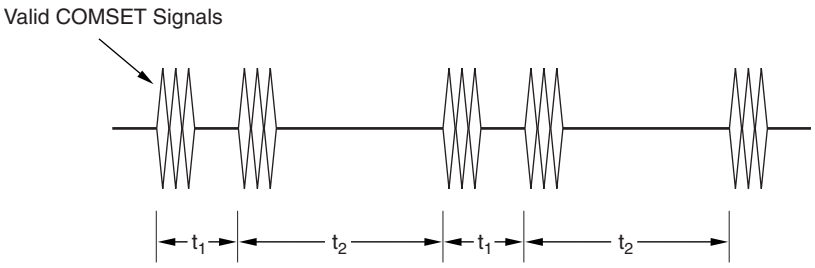
The VSC7177 detects a port selection signal received by an inactive host port. The port selection signal is a series of five, valid COMRESET signals. The duration between the first and second COMRESET series and the third and fourth COMRESET series is nominally 2.0 ms. The duration between the second and third COMRESET series and the fourth and fifth COMRESET series is nominally 8.0 ms. After the entire fifth COMRESET series has been deasserted, the inactive port that received the port selection signal is immediately switched to be the active host port. Figure 3 shows the port selection signal. Maintaining primitive alignment is not guaranteed. Reception of

COMRESET signals by an active host port are transmitted out of the device port even if the COMRESET signals are a valid port selection signal. Refer to the Serial ATA II: Port Selector Revision 1.0 specification for a complete definition of the port selection signals.

In the situation where a port selection signal is received when neither port is active (following a reset condition, for example), the port receiving the signal becomes the active host port based on the first COMRESET series. All five series of COMRESET signals are transmitted from the device port. A COMRESET signal is sent to the device in response to the first COMRESET series and makes that port active. The remaining four series of COMRESET signals are transmitted to the device because OOB signals are always transmitted once a host port has been connected to the device port.

A COMRESET signal transmitted to a device causes the device to respond with a COMINIT signal. To prevent this COMINIT signal from being squelched by the presence detection circuit's COMWAKE transmission, the VSC7177 continuously transmits a COMRESET pattern to the device until the COMWAKE transmission is completed. This guarantees the COMINIT signal from the device is propagated to the host.

Only OOB signals from an active host port are propagated to the device port. OOB signals from an inactive host port are not propagated to the device port. If no active host port is selected, OOB signals received by the device port are propagated to both host ports. When an active host port exists, OOB signals received by the device port are propagated only to the active host port.



Inter-reset Assertion Delay	Minimum	Typical	Maximum	Unit
t_1	1.6	2.0	2.4	ms
t_2	7.6	8.0	8.4	ms

Figure 3. Port Selection Signal

Data is transferred between the host and device ports without the use of PHYs. Power management, speed negotiation, and spread spectrum clocking is indirectly supported by VSC7177 because data is merely passed through the device.

Status Signals—Serial ATA II Protocol-based Port Selection

The P0SLTD output indicates the active host port. P0SLTD is LOW when port 1 is active and HIGH when port 0 is active. P0SLTD is a logic HIGH when neither host port is active.

OOBPORT0 reports the state of the inactive host port's OOB detector. OOBPORT0 reports the state of the OOB detector from port 0's input receiver when there is no active host.

There is no active host following a reset of the VSC7177.

Table 5 contains a summary of the protocol-based port selection operating mode.

Table 5. Operating Modes for Serial ATA II Protocol-based Port Selection

Active Host Port	Output Pins				
	P0OUT	P1OUT	P2OUT	P0SLTD	OOBPORT0
Port 0	P2IN	OFF(1)	P0IN	1	OOBPORT1
Port 1	OFF(1)	P2IN	P1IN	0	OOBPORT0
No active host	P2IN	P2IN	OFF(1)	1	OOBPORT0

1. OFF indicates the output driver is transmitting a common-mode state.

High-Speed Outputs

Each port has a high-speed output buffer that transmits the differential serial ATA data at rates up to 3.0 Gbps. The output pins for the ports are P0OUTP/N, P1OUTP/N, and P2OUTP/N. Each output buffer has an input to indicate when OOB signals are being transmitted and a single input to control the output voltage amplitude and to enable pre-emphasis.

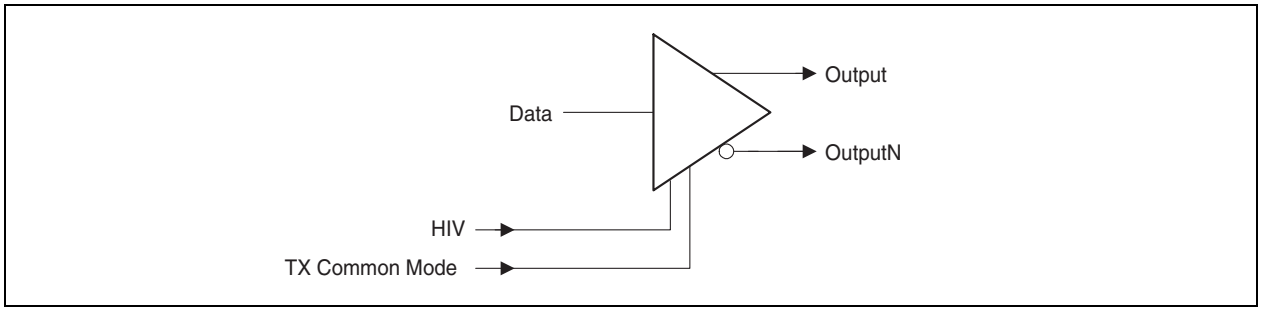


Figure 4. High-Speed Output Buffer

Transmitting OOB Signals

Both differential output signals are at the DC-bias voltage when the output buffer is disabled. The output buffer is disabled when OOB signals are transmitted and when an output port is turned "off" as described in "Modes of Operation," page 5.

Output Amplitude and Pre-Emphasis

The output buffers each have an amplitude control input pin (HIV0, HIV1, and HIV2 corresponding to port 0, port 1, and port 2, respectively) that sets the differential output voltage to normal Serial ATA levels. See Table 6. Recommended output AC-coupling capacitor values are 0.01 µF. When the amplitude control pin is HIGH, the output is configured for high voltage swing mode, which is useful for driving extended length media such as backplanes or external cables. Setting the output to high swing mode should be done only in controlled environments because the output voltage exceeds the Serial ATA 1.0 differential mode specifications.

The output buffers have a pre-emphasis circuit that is enabled when HIVx is HIGH. Pre-emphasis accentuates higher frequency signals in a transmitted data stream. This feature takes into consideration that a signal loses amplitude and affects the data eye opening as it goes through long trace length runs. Figure 5 shows the effects of the pre-emphasis feature. The amplitude increase is between 20% and 30%, and the duration of the amplitude increase is between 150 ps and 300 ps.

Table 6. Output Amplitude and Pre-Emphasis

HIVx	Output Swing Level	Pre-Emphasis
0	Normal	None
1	HIGH	Enabled

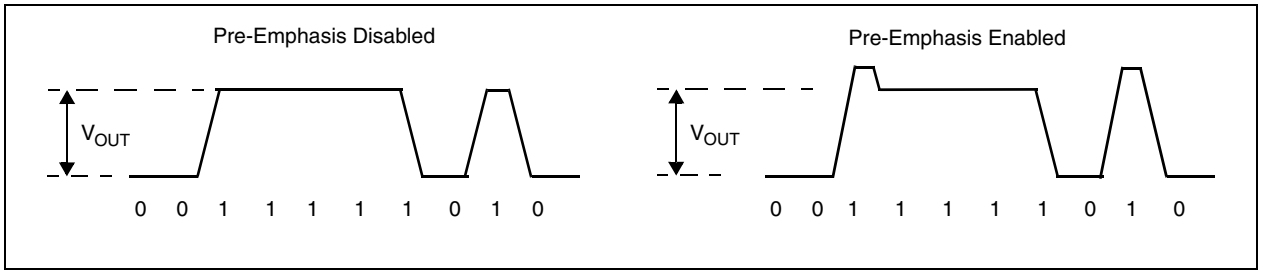


Figure 5. Pre-Emphasis Diagram

High-Speed Inputs

The high-speed input receivers are designed to achieve Serial ATA 1.0 compliance using AC-coupling as described in the Serial ATA 1.0 specification. Recommended input AC-coupling capacitor values are 0.01 µF. The high-speed input receiver contains an OOB signal detector, as shown in Figure 6.

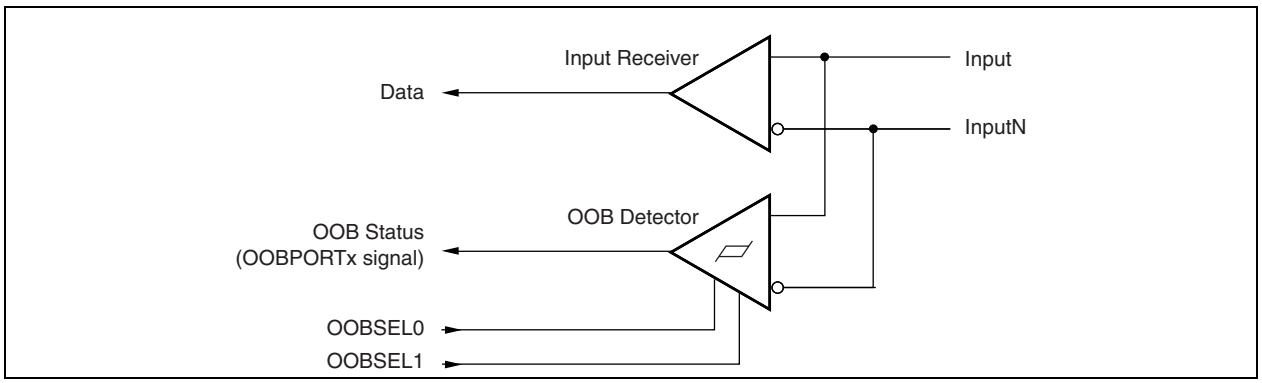


Figure 6. High-Speed Input Receiver

OOB Transfer

The VSC7177 cleanly transfers OOB signals from high-speed inputs to outputs. Two status outputs, OOBPORT0 and OOBPORT1, indicate whether the input signal is data or a common-mode state. OOBPORT1 and OOBPORT1 correspond to port 0 and port 1, respectively. An OOB detector monitors the amplitude of an incoming signal in parallel with each high-speed input. When the amplitude is less than the OOB threshold, the OOB status output is driven HIGH. When the incoming amplitude is greater than the OOB threshold, the OOB status output is driven LOW.

Setting the OOBSEL1/OOBSEL0 inputs as shown in Table 7 configures the OOB threshold level for all three ports.

Table 7. Setting the OOB Threshold Level

OOBSEL1	OOBSEL0	OOB THRESHOLD LEVEL
1	0	Nominal setting (150 mV to 250 mV)
0	0	Decrease by ~40 mV
0	1	Decrease by ~80 mV
1	1	Increase by ~40 mV

NOTE: *All values are differential peak-to-peak voltages.*

Voltage Regulator

The digital logic in the VSC7177 operates on an internally generated 1.8 V supply voltage. The regulated voltage must be connected to an external capacitor. VDDN (pin 25) is the regulated voltage pin. The recommended capacitor to use is 4.7 µF with equivalent series resistance between 0.5 Ω and 5.0 Ω

DESIGN GUIDELINES

Pinout Differences Between VSC7177 and VSC7173/VSC7175

The VSC7177 device is an upgrade to the VSC7173 and the VSC7175 devices. The VSC7177 package is the same as the VSC7173 and the VSC7175; however, there are two pin requirement changes to be aware of when using a VSC7177 device on a board designed for the VSC7173 or the VSC7175.

- Pin 25 (VDDN) in the VSC7177 is an internally-generated 1.8 V supply voltage. This pin must be connected to a capacitor as described in "Voltage Regulator," page 12. Pin 25 (Reserved) is not used in the VSC7173 or in the VSC7175.
- Pin 18 (PORTSEL1) and pin 21 (MODE1) in the VSC7177 must both be set LOW to enable level-sensitive sideband mode. Setting PORTSEL1 HIGH enables the protocol-based port selection mode listed in Table 1, page 5. In the VSC7173 and the VSC7175, setting only pin 21 (MODE1) to LOW is required to enable level-sensitive sideband mode. Pin 18 (HSTSELB) in the VSC7173 and the VSC7175 is not used in the this mode and is a "don't care" (connect to any value). The logical value of PORTSEL0/HSTSELA (pin 19 in the VSC7177, the VSC7173, and the VSC7175) selects the connected port in level-sensitive mode.
- Pin 9 in the VSC7175 (OOBDTA) reports the OOB status for Host A. For the VSC7177 device, pin 9 (OOBPORT0) reports the OOB status for the unselected host port.

Table 8 provides a summary of the pinout differences.

Table 8. VSC7177 and VSC7173/VSC7175 Pinout Differences

Pin Number	Operating Mode	Pin Function / Connectivity		
		VSC7173	VSC7175	VSC7177
18	Level-sensitive sideband mode	X (don't care)	X (don't care)	VSS (ground)
25	All modes	Not used	Not used	Connect to external capacitor
9	All modes	OOB status for Port 0	OOB status for Host A	OOB status for unselected host port

Sideband Loopback Function

A sideband loopback feature has been added to the VSC7177 in sideband mode. Consequently, the VSC7177 has different functionality than either the VSC7173 or the VSC7175 in this mode. Port 2 can be connected to port 0 or port 1 in sideband mode. The data transmitted from the output driver of the unconnected port can be data from port 2 (the downstream device) or data from the unconnected port's input receiver (loopback data). The data transmitted is selected with the MODE0 input. The ability to loopback the data from the unconnected port is a new feature for sideband mode. Both the VSC7173 and the VSC7175 transmit the downstream device data or a common-mode signal from the unconnected port's output driver. The VSC7177 cannot directly force transmission of common mode from the unconnected port. Transmission of common mode is achieved indirectly by enabling the loopback mode and having the host send a common mode signal to the VSC7177.

ELECTRICAL SPECIFICATIONS

DC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 15, page 18.

Table 9. LVTTL Inputs and Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OH}	Output HIGH voltage	2.0	2.2	V_{DD}	V	I_{OH} = –4 mA
V_{OL}	Output LOW voltage	0.0	0.2	0.4	V	I_{OL} = 4 mA
V_{IH}	Input HIGH voltage	2.0		V_{DD}	V	
V_{IL}	Input LOW voltage	0.0		0.8	V	
I_I	Input current (includes a weak pull-up resistor)	–200		+50	µA	0 V < V_{IL} < 2.4 V

Table 10. High-Speed Inputs and Outputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{TH}	Input threshold voltage for OOB detection		200		mV	See Table 7.
V_{OCM}	High-speed output common-mode voltage		2.0		V	Normal Swing mode. 100 Ω termination between true and complement outputs.
			1.7		V	High Swing mode. 100 Ω termination between true and complement outputs.
V_{ICM}	High-speed input common-mode voltage		1.5		V	
Z_{IN}	Differential input impedance	85	100	115	Ω	

Table 11. Power Supply Requirements for Sideband Operating Mode

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Power supply voltage	3.0	3.3	3.6	V	±10% on all supplies
I_{DD}	Power supply current (total on all supply pins)		150	170	mA	Normal Swing mode
			200	235	mA	High Swing mode
P_D	Total power dissipation		540	625	mW	Normal Swing mode
			720	850	mW	High Swing mode

Table 12. Power Supply Requirements for Serial ATA II Protocol Port Selection Mode

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Power supply voltage	3.0	3.3	3.6	V	±10% on all supplies
I_{DD}	Power supply current (total on all supply pins)		175	238	mA	Normal Swing mode
			225	295	mA	High Swing mode
P_D	Total power dissipation		635	860	mW	Normal Swing mode
			817	1065	mW	High Swing mode

AC Characteristics

Specifications are guaranteed over the recommended operating conditions listed in Table 15, page 18.

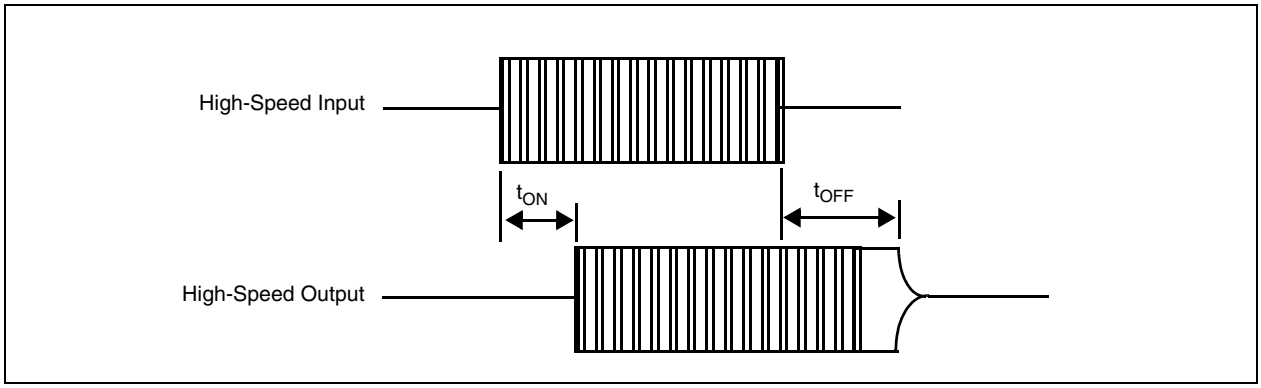
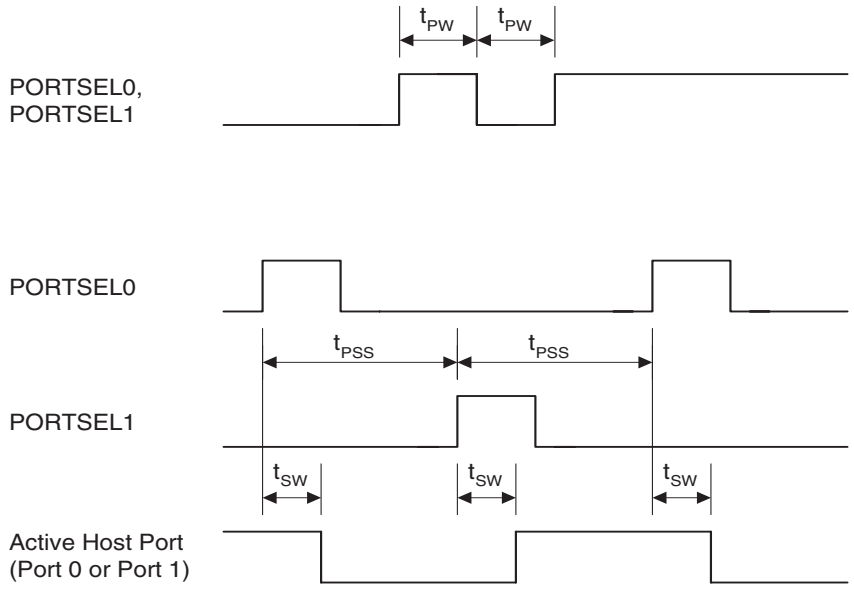


Figure 7. Timing Waveform

Table 13. High-Speed Inputs and Outputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_P	Propagation delay from any high-speed input to high-speed output	0.4	2.0	ns	
t_{ON}	Propagation delay from signal present at input to output buffer turned on	3.0	12.0	ns	
t_{OFF}	Propagation delay from no signal at input to output buffer turned off	3.0	12.0	ns	
t_R, t_F	Rise and fall times	67	260	ps	1.5 Gbps operation, 20% to 80%.
V_{OUT}(1)	OUTx output differential peak-to-peak voltage swing in normal swing mode (HIVx is LOW)	500	700	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3. 100 Ω termination between true and complement outputs.
V_{OUT}(1, 2)	OUTx output differential peak-to-peak voltage swing in high swing mode (HIVx is HIGH)	800	1300	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3. 100 Ω termination between true and complement outputs.
V_{IN}	INx input differential peak-to-peak swing with OOBSEL1 = 1 and OOBSEL0 = 0 (OOB nominal)	275	1600	mVp-p	Measured per Serial ATA 1.0 specification.
V_{IN}	INx input differential peak-to-peak swing with OOBSEL1 = 0 and OOBSEL0 = 1 (OOB minimal)	225	1600	mVp-p	Measured per Serial ATA 1.0 specification, section 6.6.3.

1. *Refer to Application Note AN-37 for differential measurement techniques.*
2. *Output swings are higher than the Serial ATA 1.0 specification to compensate for anticipated PCB or connector losses.*



Note: Edge-sensitive side band operation shown.

Figure 8. Timing Waveform—Sideband Switching

Table 14. Sideband Switching

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_{PW}	Pulse width of the port selection pins (PORTSEL0, PORTSEL1)	4.0		ns	
t_{PSS}	Separation between rising edge transitions of the port selection pins	5.0		ns	Applies to edge-sensitive sideband operation.
t_{SW}	Switch time. The time required to make the other host port active following an active edge transition of the port selection pins.		5.0	ns	Applies to both level and edge-sensitive sideband operations.

Operating Conditions

Table 15. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
T	Operating temperature(1)	0		+90	°C

1. Lower limit of specification is ambient temperature and upper limit is case temperature.

Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage	–0.5	+4.0	V
V_{INT}	LVTTL input voltage	–0.5	V_{DD} +0.5	V
V_{OUTT}	LVTTL output voltage	–0.5	V_{DD} +0.5	V
I_{OT}	LVTTL output current	–50	+50	mA
V_{INS}	Serial input voltage	–0.5	V_{DD} +0.5	V
V_{OUTS}	Serial output voltage	–0.5	V_{DD} +0.5	V
I_{OS}	Serial output current	–50	+50	mA
T_S	Storage temperature	–65	+140	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–4000	+4000	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

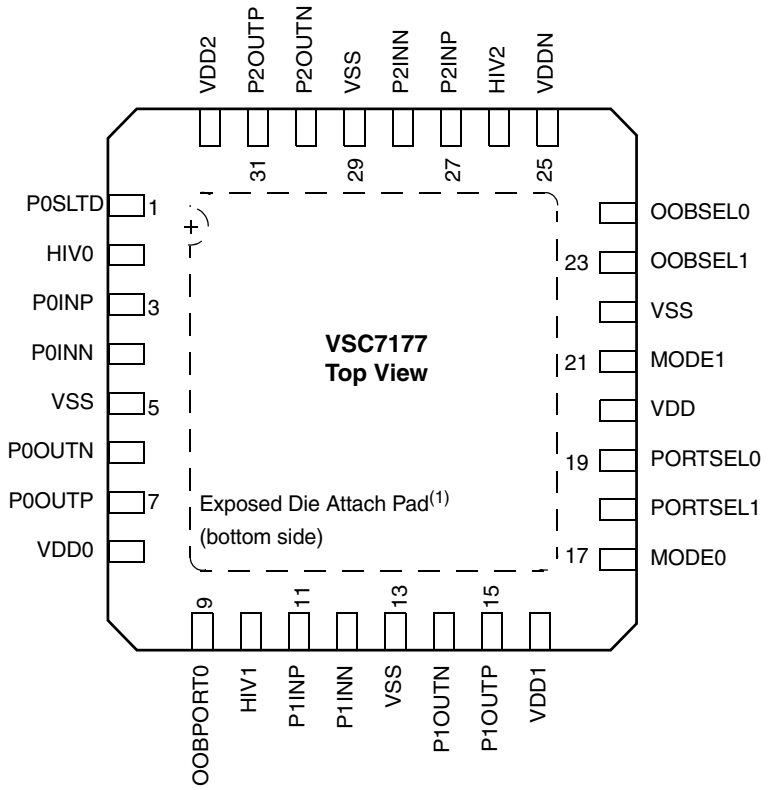
ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Maxim recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

Pin Diagram

The VSC7177 device has 32 pins, which are shown in the following illustration.



1. The exposed Die Attach Pad (DAP) is internally connected to ground and should also be connected to VSS on the board.

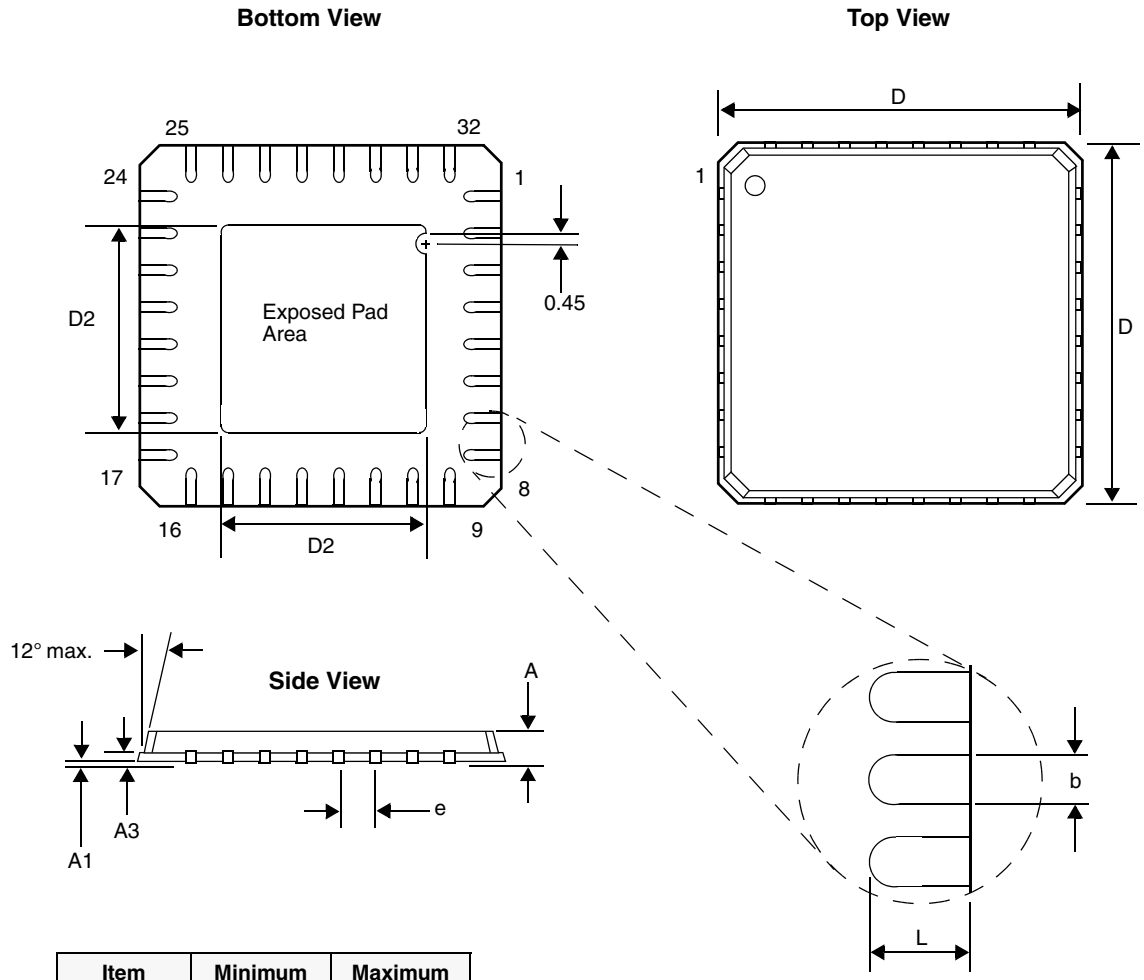
Figure 9. Pin Diagram

Pin Identifications

Table 17. Pin Identifications

Pin Number	Signal	Type	Level	Description
7, 6 15, 14 31, 30	P0OUTP, P0OUTN P1OUTP, P1OUTN P2OUTP, P2OUTN	O	High-Speed	These are the high-speed differential outputs for port 0, port 1, and port 2. These outputs must be AC-coupled.
3, 4 11, 12 27, 28	P0INP, P0INN P1INP, P1INN P2INP, P2INN	I	High-Speed	These are the high-speed differential inputs for port 0, port 1, and port 2. These inputs must be AC-coupled.
19 18	PORTSEL0 PORTSEL1	I	LVTTL	These two inputs select the active port (port 0 or port 1) when the device is in sideband-based port selection mode. PORTSEL1 is used to choose the port selection mode when the VSC7177 is operating in protocol-based port selection mode. For more information on the operating modes, see Table 1, page 5 and "Functional Descriptions" on page 5.
2 10 26	HIV0 HIV1 HIV2	I	LVTTL	When HIGH, selects the high voltage swing output mode for the corresponding output buffer and enables pre-emphasis. See Table 6, page 11.
24 23	OOBSEL0 OOBSEL1	I	LVTTL	These two inputs control the OOB detector threshold voltage for all three input ports. See Table 7, page 12 for threshold levels.
1 9	P0SLTD OOBPORT0	O	LVTTL	These status signals can be monitored by the host for diagnostics. See Table 2, page 6 and Table 5, page 10.
17	MODE0	I	LVTTL	For sideband-based port selection, MODE0 is used as described in Table 3, page 7. For protocol based port selection, MODE0 must be HIGH.
21	MODE1	I	LVTTL	For sideband-based port selection, MODE1 is used as described in Table 3, page 7. For protocol based port selection, MODE1 must be LOW.
20	VDD		Power	3.3 V power supply for all circuits except the high-speed output buffers.
8, 16 32	VDD0, VDD1 VDD2		Power	3.3 V output buffer power supply for P0OUTP/N, P1OUTP/N, and P2OUTP/N, respectively.
25	VDDN		Analog	1.8 V power supply generated by internal voltage regulator. Connect a 4.7 µF capacitor with equivalent series resistance between 0.5 Ω and 5 Ω to this pin.
5, 13, 22, 29 DAP	VSS		GND	Common ground. DAP is the exposed die attach pad on the bottom of the device.

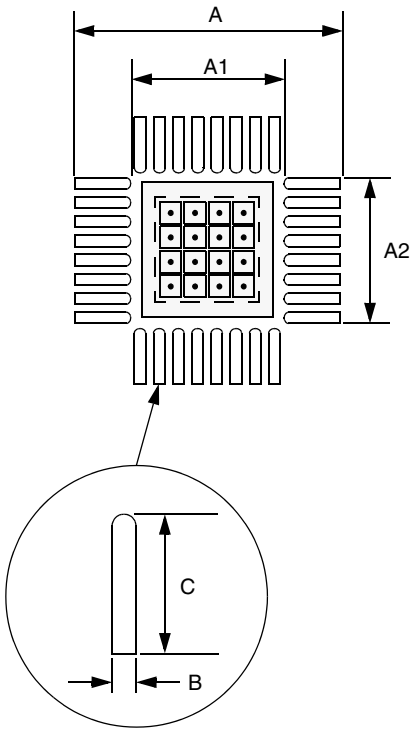
Package Drawing



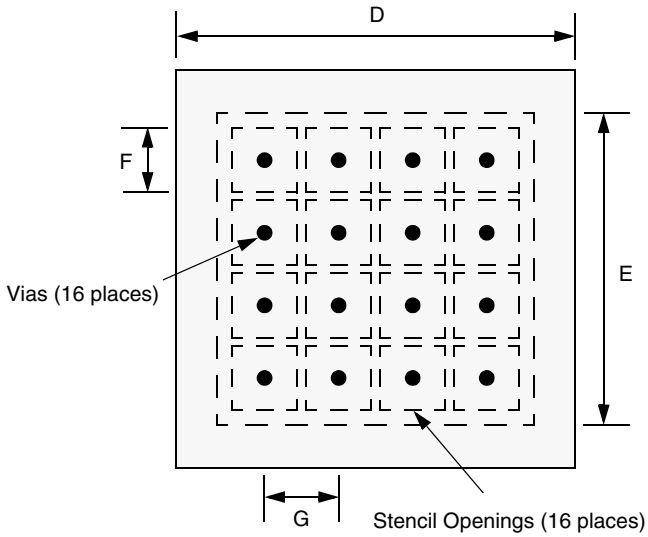
Item	Minimum	Maximum
A	0.85 nom.	0.90
A1	0	0.05
A3	0.20 REF	
b	0.23	0.35
D	7.00 BSC	
D2	4.95	5.25
e	0.65 BSC	
L	0.50	0.75

NOTES: *Drawing not to scale.*
All units in mm unless otherwise noted.
"b" is measured 0.20 to 0.25 from the terminal tip.

Figure 10. Package Drawing



Land Pad Detail



Item	7 mm x 7 mm x 0.9 mm Exposed Pad QFP-N	Comments
A	7.445 maximum	
A1	5.325 minimum	
A2	4.92 maximum	
B	0.37 maximum	
C	1.06	
D	4.95 minimum 5.075 typical 5.20 maximum	Thermal land dimensions
E	5.10	Solder mask opening dimension
F	1.0	Stencil opening dimensions
G	1.2	Stencil opening and via spacing

NOTES: *All vias 0.30 to 0.33 diameter, plugged.*
Drawing not to scale.
All dimensions are in mm unless otherwise noted.

Figure 11. Recommended Land Pattern

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 18. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7177YI	18.2	30	28.7	27
VSC7177XYI	18.2	30	28.7	27

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

The VSC7177 device is available in two package types. VSC7177YI is a 32-pin, quad flat pack with no leads (QFP-N) and an exposed pad. The device is also available in a lead(Pb)-free package, VSC7177XYI.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC7177 device.

VSC7177 Enhanced 2:1 Port Selector for Serial ATA and Serial Attached SCSI

Part Number	Description
VSC7177YI	32-pin QFP-N, 7 mm x 7 mm x 0.9 mm body
VSC7177XYI	Lead(Pb)-free, 32-pin QFP-N, 7 mm × 7 mm × 0.9 mm body

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Sunnyvale, CA 94086
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408-737-7600
www.maxim-ic.com