VITESSE

VSC7147-01 and VSC7147-05 Data Sheet

Hex PBC with Dual Repeater/Retimer for 1.0625Gb/s and 2.125Gb/s FC-AL Disk Arrays

FEATURES

- NCITS T11 Fibre Channel Compliant at 1.0625Gb/s and 2.125Gb/s
- Two FibreTimer® Cells Configured as:
  - Repeaters for Low Latency
  - Retimers for True Fibre Channel Compliance
- Six Port Bypass Circuits (PBCs)
- Two Digital Signal Detect Units (SDUs)
- Cable Equalization on All High-Speed Inputs
- Speed-Independent Tx and Rx Paths to Aid in Auto-Speed Negotiation
- 106.25MHz Reference Clock
- 5V-Tolerant LVTTL Inputs
- VSC7147-0x Adds an Analog Signal Detect (ASD) Function to the VSC7147
- Single 2.5V Supply, 1.6W Typical Power
- 100-Pin, 14mm Exposed Pad TQFP Package

APPLICATIONS

- Disk Arrays
- JBODs

GENERAL DESCRIPTION

The VSC7147-01 and VSC7147-05 contain six Port Bypass Circuits (PBCs), dual FibreTimer repeater/retimer cells, and dual Signal Detect Units (SDUs). These functions are integrated into a single part to minimize part count, cost, high-frequency routing, and jitter.

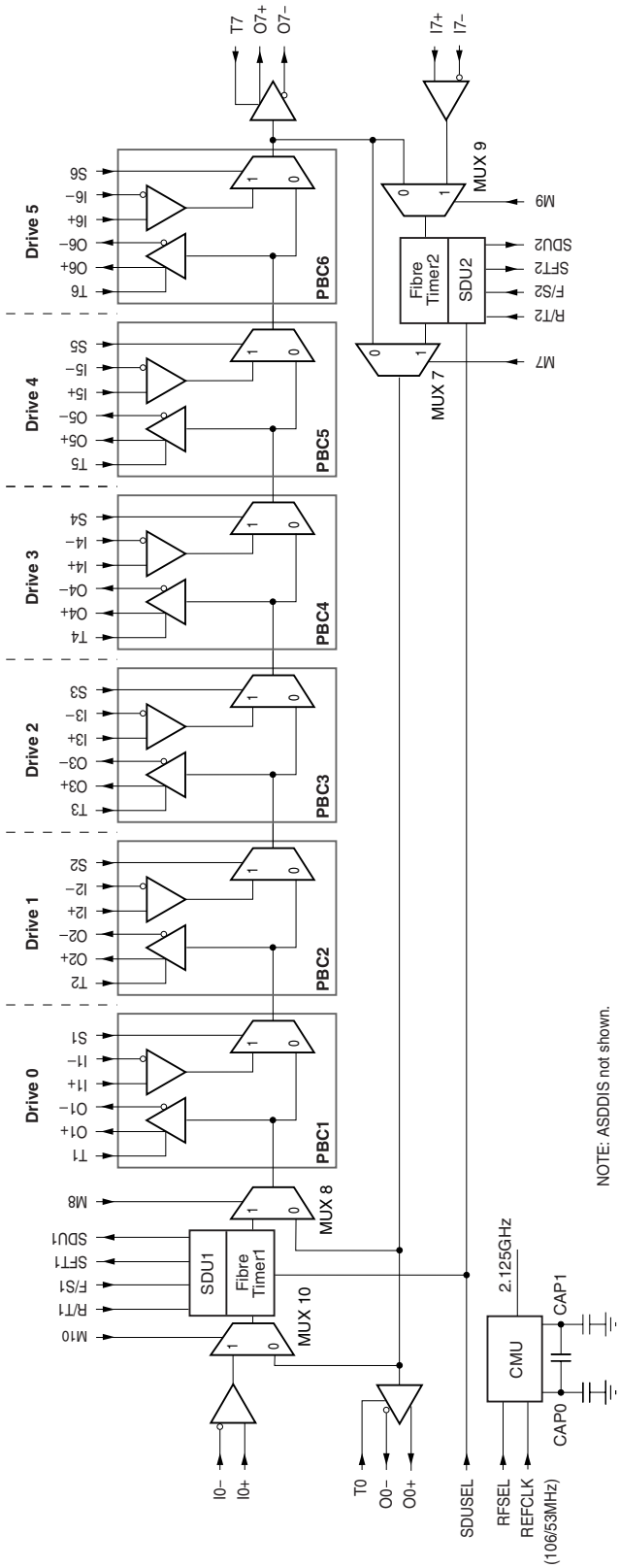
Each FibreTimer cell contains an all-digital Clock Recovery Unit (CRU) that can be configured as either a repeater or a retimer. Repeaters recover the incoming signal and retransmit the data synchronously to the recovered clock in order to attenuate jitter so that downstream devices see high amplitude, low jitter signals. Retimers eliminate jitter transfer by retiming the recovered data to the local reference clock. An add/drop FIFO inserts or deletes 40-bit fill words to match the incoming data rate to the local reference clock, ensuring Fibre Channel compliance at the output of the retimer.

The VSC7147-01 and VSC7147-05 are modifications of the VSC7147 that incorporate an Analog Signal Detect function not found in the VSC7147, as well as a number of other modifications aimed at improving the performance of the part. The -01 and -05 variants were added to the part number to facilitate customer ordering in situations where both the VSC7147 and VSC7147-0x may be used at the same time.The -05 variant is identical to the -01 variant, with the exception that it utilizies a material set that is qualified to withstand a +250°C +0°C/–5°C IR reflow temperature per JEDEC standard IPC/JEDEC J-STD-020B.

This data sheet relates to both the VSC7147-01 and VSC7147-05. “VSC7147-0x” will be used in the text to represent both parts, except where noted specifically by the respective part number.

Confidential

VSC7147-0x Block Diagram



APPLICATION EXAMPLES

12 Drives, One Connector Per Loop

In this application, up to twelve drives on a single loop may be accessed with one connector. Fibre Channel data from a source enters the loop through the connector then passes through FibreTimer1 (in repeater mode) of VSC7147-0x #1, six PBCs, FibreTimer1 (in retimer mode) of VSC7147-0x #2, and then returns to the source through the VSC7147-0x #1's FibreTimer2 (in retimer mode). The retimer is used at the output of the system to ensure Fibre Channel compliance whereas repeaters are used elsewhere to minimize latency. FibreTimer2 in VSC7147-0x #2 is unused but could be used if the two chips are separated by more than two inches to minimize jitter.

Table 1. VSC7147-0x JBOD Configuration: 12-Drive JBOD, One Connector per Loop

Signal	VSC7147-0x #1	VSC7147-0x #2
M7	HIGH	LOW
M8	HIGH	HIGH
M9	HIGH	HIGH
M10	HIGH	HIGH
R/T1	HIGH	HIGH
R/T2	LOW	HIGH

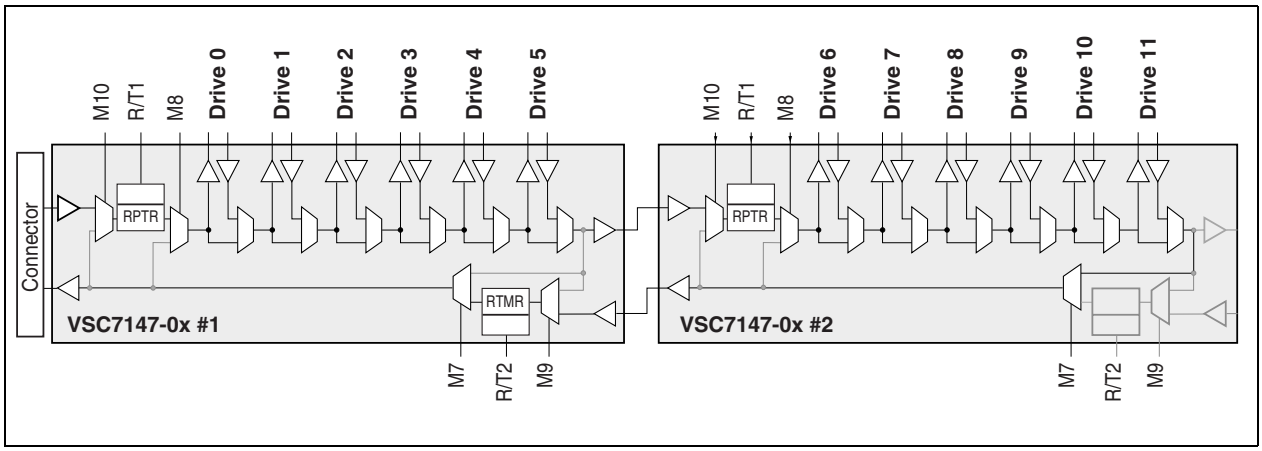


Figure 1. 12-Drive JBOD, 1 Connector Per Loop

12 Drives, Two Connectors Per Loop

In this application, up to twelve drives on a single loop may be accessed with two daisy-chainable connectors. At any given time, either connector may be active. Table 2 shows the configurations of the device when connector 1 is the only active link, when connector 2 is the only active link, or when both connectors are active. Ideally, the FibreTimer cells will be configured as retimers only when they are the output to the connector. For this reason, FibreTimer2 in VSC7147-0x #1 is a retimer when connector 1 is active. Likewise, FibreTimer2 in VSC7147-0x #2 is a retimer when connector 2 is active.

This scheme has one system-level disadvantage: when both connectors are active, the six drives on VSC7147-0x #1 will be sequential and the six drives associated with VSC7147-0x #2 will be sequential. However, additional FC-AL devices would be located between these two groups externally. If this is an acceptable solution, then this scheme is simple.

Table 2. VSC7147-0x JBOD Configuration: 12-Drive Cascadable JBOD, Two Connectors Per Loop

Signal	Connector 1 Active		Connector 2 Active		Both Connectors Active	
	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2
M7	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
M8	HIGH	LOW	LOW	HIGH	HIGH	HIGH
M9	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
M10	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
R/T1	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
R/T2	LOW	LOW	LOW	LOW	LOW	LOW

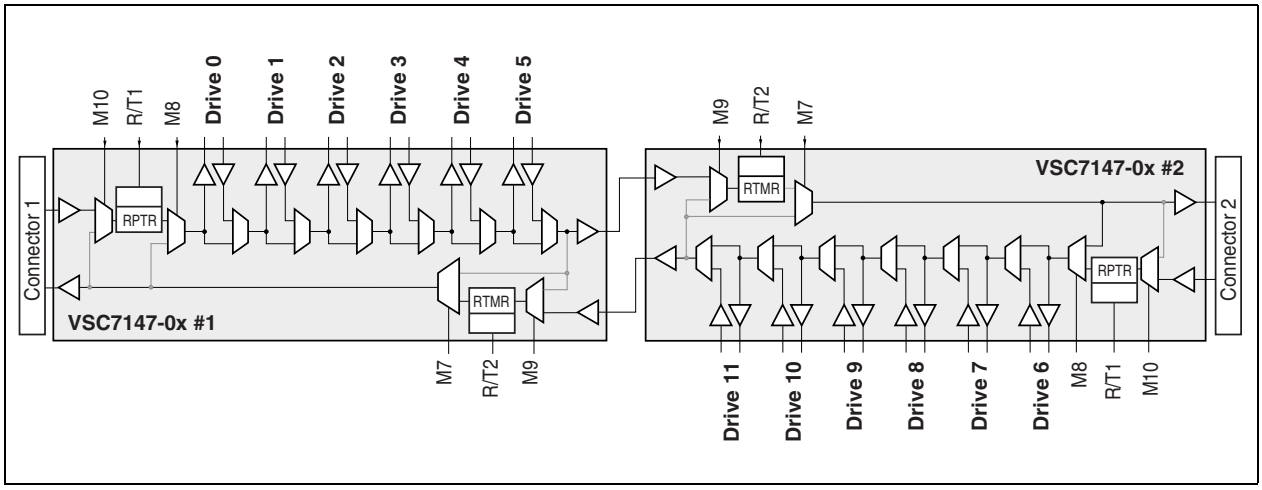


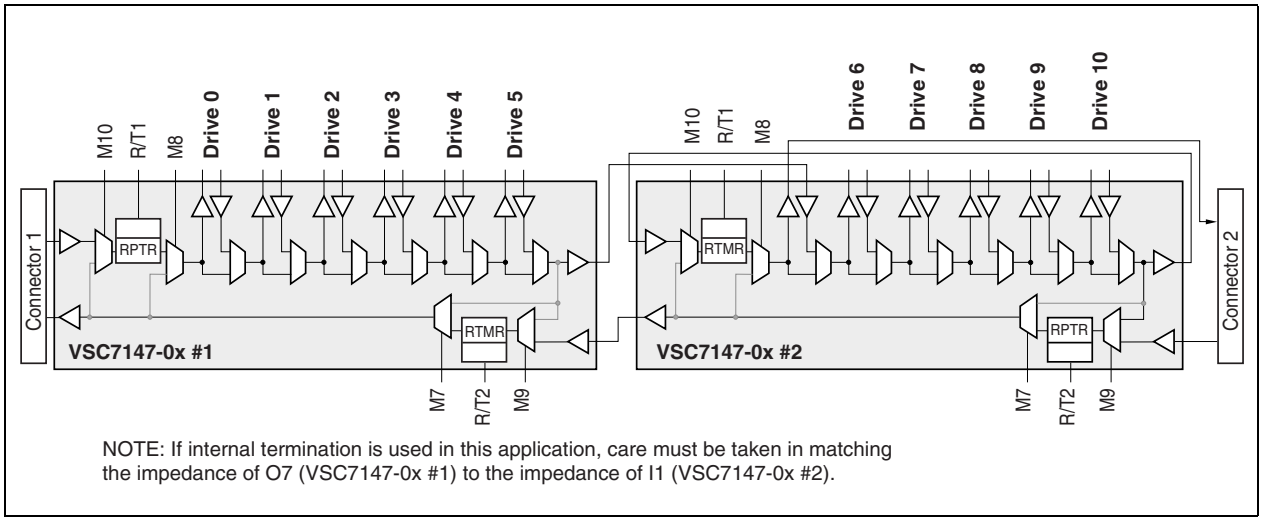
Figure 2. 12-Drive Cascadable JBOD, Two Connectors Per Loop

11 Drives, Two Connectors Per Loop

In this application, up to eleven drives on a single loop may be accessed with two daisy-chainable connectors. This is similar to the previous example, however, one PBC is sacrificed in order to keep all eleven drives arranged sequentially. FibreTimer1 of VSC7147-0x #2 is used as a retimer after the last disk drive, but before the connector. This scheme has one disadvantage; the path from FibreTimer1 in VSC7147-0x #1 through the eleven drives and back to FibreTimer2 in VSC7147-0x #1 does not have any repeater/retimers in the path. This forces the two devices to be located close to each other in order to minimize chip-to-chip jitter.

Table 3. VSC7147-0x JBOD Configuration: 11-Drive Cascadable JBOD, Two Connectors Per Loop

Signal	Connector 1 Active		Connector 2 Active		Both Connectors Active	
	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2
M7	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
M8	HIGH	HIGH	LOW	HIGH	HIGH	HIGH
M9	HIGH	LOW	HIGH	HIGH	HIGH	HIGH
M10	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
R/T1	HIGH	LOW	HIGH	LOW	HIGH	LOW
R/T2	LOW	HIGH	LOW	HIGH	LOW	HIGH



NOTE: If internal termination is used in this application, care must be taken in matching the impedance of O7 (VSC7147-0x #1) to the impedance of I1 (VSC7147-0x #2).

Figure 3. 11-Drive Cascadable JBOD, Two Connectors Per Loop

10 Drives, Two Connectors Per Loop

In this application, up to ten drives on a single loop may be accessed with two daisy-chainable connectors. This is similar to the previous example, however, one additional PBC is sacrificed in order to provide internal termination. This option is recommended if internal termination is utilized, and connector 1 and connector 2 require a different impedance than the drive ports. This application scheme provides proper impedance matching for connections between VSC7147-0x #1 and VSC7147-0x #2 while keeping the ten drives arranged sequentially.

Additionally, this scheme implements a repeater/retimer approach specifically at each connector. This scheme has one disadvantage in that the devices need to be located close to each other in order to minimize chip-to-chip jitter.

Table 4. VSC7147-0x JBOD Configuration: 10-Drive Cascadable JBOD, Two Connectors Per Loop

Signal	Connector 1 Active		Connector 2 Active		Both Connectors Active	
	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2	VSC7147-0x #1	VSC7147-0x #2
M7	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
M8	HIGH	LOW	LOW	HIGH	HIGH	HIGH
M9	LOW	LOW	LOW	LOW	LOW	LOW
M10	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
R/T1	HIGH	LOW	HIGH	HIGH	HIGH	LOW
R/T2	LOW	LOW	LOW	LOW	LOW	LOW

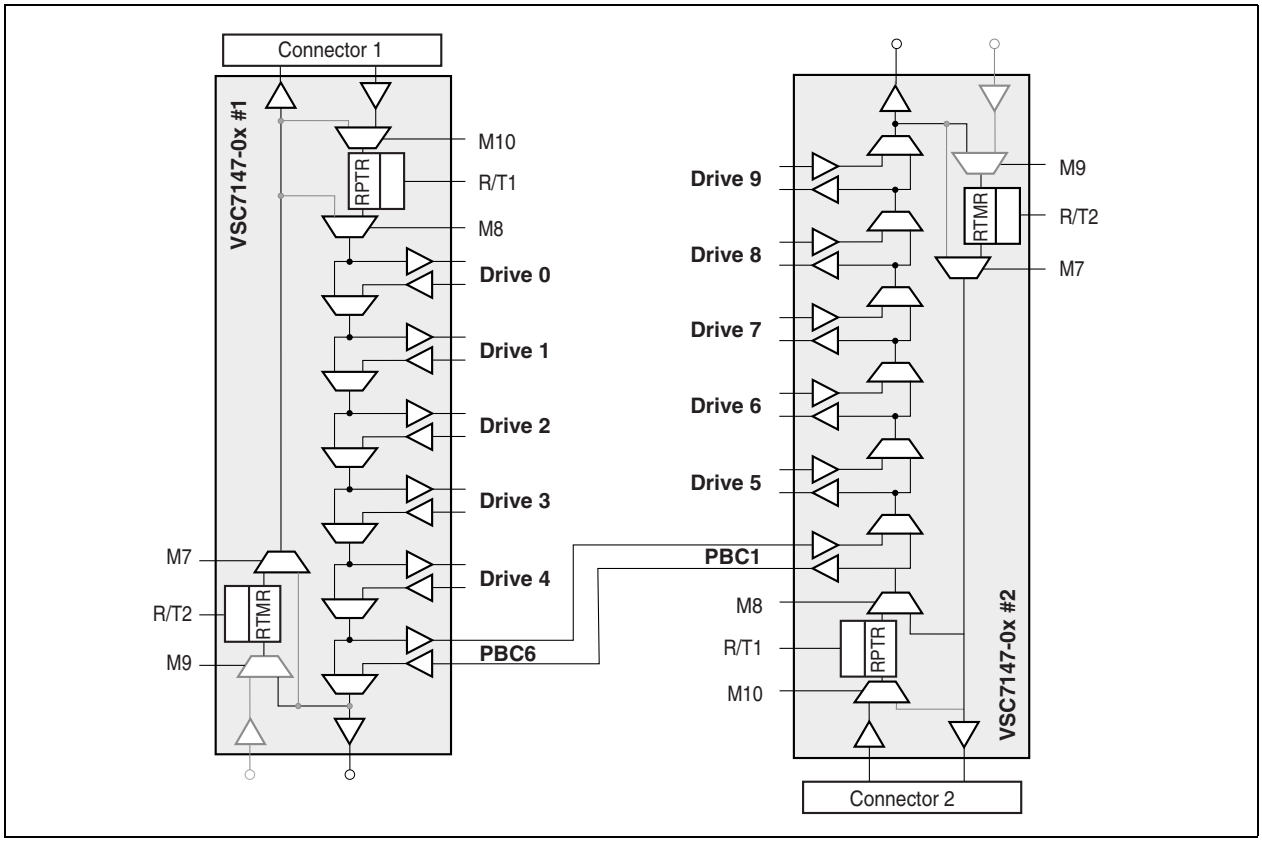


Figure 4. 10-Drive Cascadable JBOD, Two Connectors Per Loop

FUNCTIONAL DESCRIPTION

Notation. Differential signals can be identified individually, e.g., I0+ and I0–, or together, e.g., I0. Signals and circuits that are repeated are generically named using a “x” to denote any channel, e.g., PBCx for any PBC.

Clock Multiplier Unit

The VSC7147-0x Clock Multiplier Unit (CMU) Phase-Locked Loop (PLL) multiplies the reference frequency provided on the REFCLK pin by either 20 or 40, as determined by the RFSEL input, to generate an internal clock at 2.125GHz. If RFSEL is HIGH (Vitesse’s recommended configuration), a 106.25MHz reference clock is used and the CMU multiplies by 20. If RFSEL is LOW, a 53.125MHz reference clock is used and the CMU multiplies by 40. REFCLK and RFSEL are independent of the data rate selected by the F/S1 and F/S2 inputs. If the REFLCK frequency does not match the RFSEL input, unpredictable behavior may occur. The reference clock is used by the CMU to generate the internal bit rate clock. In order to maximize signal quality of the high-speed outputs, REFCLK should be of the highest quality possible with sharp edges and low jitter. To optimize jitter performance, it is recommended that the user set RFSEL HIGH and the input CMU operate in 20x mode. In 40x mode, the jitter may not comply with all Fibre Channel jitter specifications. Duty cycle distortion is as critical because only the rising edge of REFCLK is used. Separate power (VDDA) and ground (VSSA) are provided in order to allow a separately filtered power supply to the PLL in order to reduce noise. Figure 5 shows the recommended VDDA filtering scheme.

The on-chip PLL uses external filtering connected to CAP0 and CAP1 to control the loop filter. Figure 6 is the required loop filtering scheme to provide the best noise immunity. These capacitors should be multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient. The capacitors are used to minimize the impact of common-mode noise on the CMU, especially power supply noise. 0.1µF is adequate, but larger values are better. Higher value capacitors provide better robustness in systems. NPO is preferred but X7R is acceptable. If an X7R capacitor is used, the power supply noise sensitivity will vary with temperature. These components should be isolated from noisy traces.

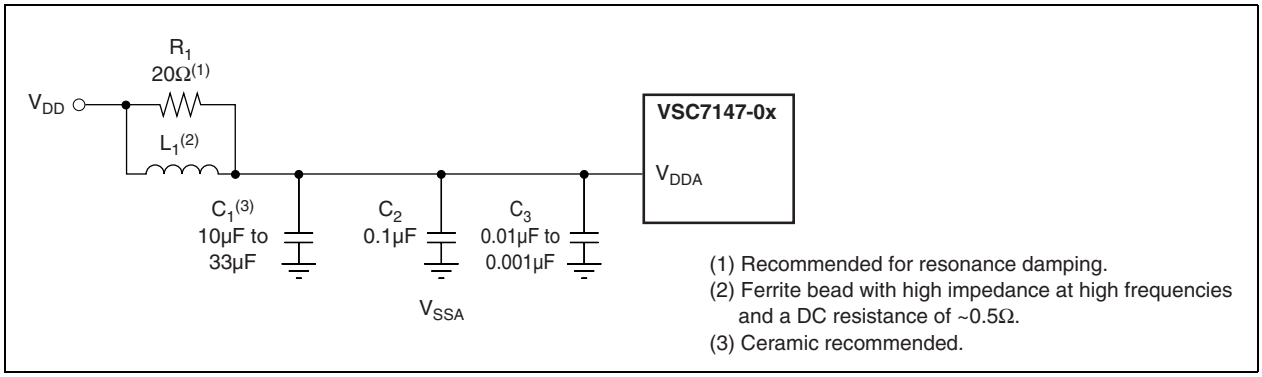


Figure 5. V_{DDA} Filtering (Recommended Circuit)

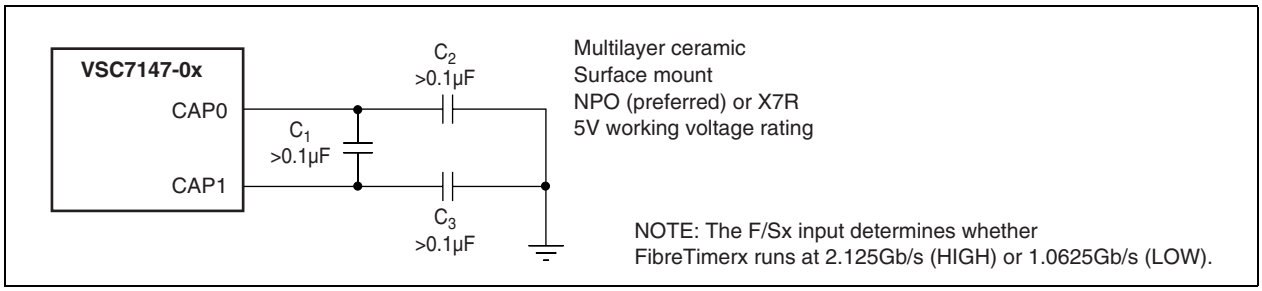


Figure 6. Loop FIlter Capacitors (Required Circuit)

High-Speed Input Buffers, Signal Detection, and Cable Equalization

All high-speed, differential inputs contain a cable equalization circuit (included in the input buffer) that accentuates high-frequency signals in order to compensate for the high-frequency loss found in copper cables and traces. All input buffers are powered only when used. For example, I4+/– is powered when S4 is HIGH, I0+/– is powered only when M10 is HIGH and I7+/– is powered only when M9 is HIGH.

On-chip impedance matching resistors are provided for optimal signal quality. RHSL determines the on-chip impedance of I0 and I7. RPSL determines the on-chip impedance of the I1 through I6 input buffers, providing two impedance domains for flexibility.

An external 1% resistor should be placed between RHSL/RPSL and ground in order to set the impedance of the termination.

NOTE: *If 100Ω differential termination is desired, a 100Ω resistor should be used. If 150Ω differential termination is desired, a 150Ω resistor should be used.*

Configuration Multiplexers

Four configuration multiplexers, MUX7 through MUX10, configure the device for various modes of operation. MUX7 selects between the output of PBC6 (when M7 is LOW) or FibreTimer2 (when M7 is HIGH) to be sent to O0, MUX8 and MUX10. MUX8 selects between the output of MUX7 (when M8 is LOW) or the output of FibreTimer1 (when M8 is HIGH) to be sent to PBC1. MUX9 selects between the output of PBC6 (when M9 is LOW) or I7 (when M9 is HIGH) to be sent to FibreTimer2. MUX10 selects between the output of MUX7 (when M10 is LOW) or I0 (when M10 is HIGH) to be sent to FibreTimer1. I0+/– is powered only when M10 is HIGH. I7+/– is powered only when M9 is HIGH.

Table 5. Configuration Multiplexer Settings

Signal	Setting	Result
M7	HIGH	Select output of FibreTimer2
	LOW	Select output of PBC6
M8	HIGH	Select output of FibreTimer1
	LOW	Select output of MUX7
M9	HIGH	Select input I7
	LOW	Select output of PBC6
M10	HIGH	Select input I0
	LOW	Select output of MUX7

High-Speed Output Buffers

All high-speed differential outputs have on-chip termination resistors. However, if the end termination is the source of unwanted reflections, it is recommended that 22Ω to 35Ω series resistors be added to all high-speed outputs for impedance matching. Additionally, each output has a transmitter enable pin, Tx, which when LOW, powers down the output driver to reduce power and electromagnetic emissions. Tx must be HIGH for normal operation.

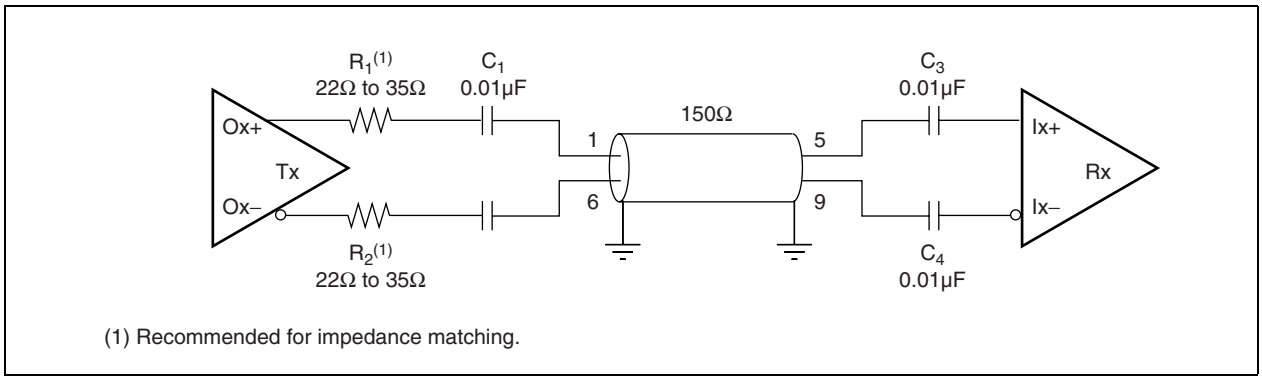


Figure 7. Typical Link Example

Pre-Emphasis

All high-speed, differential outputs contain a pre-emphasis circuit, which can be enabled to accentuate higher frequency signals in a transmitted data stream. This feature takes into consideration that a signal loses amplitude and affects the data eye opening as it goes through long cables or trace length runs. The pre-emphasis circuitry is a peaking amplifier with its peak at or above 1.6GHz and is incorporated into the output pads. The target is to pre-equalize the data signal for a frequency-dependent loss of up to –10dB/decade at 1.6GHz (e.g., 20 meters of RG58 cable). A total gain of 2dB to 3dB is produced by the pre-emphasis circuit for higher frequency components of a data stream, which produces more open data eyes at the end of a long cable or trace length run. Figure 8 shows the effects of the pre-emphasis feature when enabled versus disabled.

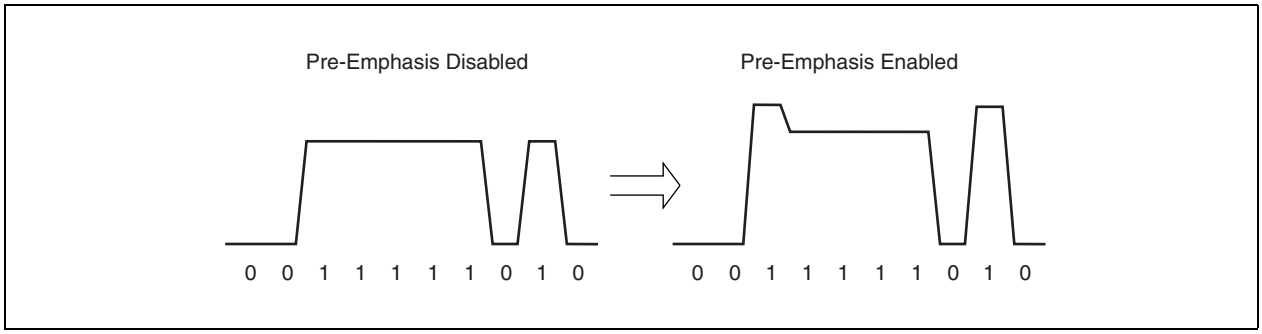


Figure 8. Pre-Emphasis Effect

The HPEMP (pin 47) and PPEMP (pin 48) inputs control the pre-emphasis functions for the VSC7147-0x high-speed, differential outputs. HPEMP controls the pre-emphasis feature on O0+/– and O7+/–, and PPEMP controls the pre-emphasis feature on O1+/– through O6+/–. HIGH will disable pre-emphasis, and LOW will enable pre-emphasis for the associated pins.

Clock and Data Recovery Units (FibreTimerx)

There are two all-digital Clock and Data Recovery Units (CDRx), known as FibreTimer cells, in the VSC7147-0x. Each is paired with an SDU to indicate if the input to the CDR is a valid Fibre Channel signal. When R/Tx is HIGH, the FibreTimer cell is configured as a repeater. When R/Tx is LOW, the cell is a retimer. FibreTimer1 recovers data from MUX10 and sends it to MUX8. FibreTimer2 recovers data from MUX9 and sends it to MUX7.

Repeater Mode

The term “repeater” will be used for a CDR function where the recovered serial data is retransmitted synchronously to the recovered clock. Unlike standard PLL-based CDRs, this circuit is all-digital, resulting in good jitter tolerance, excellent jitter transfer and low latency in a circuit which performs identically across process, voltage, and temperature.

In repeater mode, serial data enters the CDR where the clock is extracted from the data and the data is resynchronized to the recovered clock. The resynchronized output of the CDR contains serial data with improved signal quality due to amplification of the signal and attenuation of input jitter. In repeater mode, not all of the jitter at the input is eliminated from the recovered data. However, any jitter that passes through the repeater is low frequency and therefore, benign to downstream devices.

Retimer Mode

The term “retimer” is used for a CDR which retransmits the recovered serial data synchronously to the locally generated internal bit clock. This complex CDR function eliminates jitter transfer at the expense of latency. Due to the potential mismatch between the bit rate of the incoming data and the local reference clock (±200ppm), an add/drop elasticity buffer is needed to insert/delete special ordered sets, called fill words, to accommodate this rate difference. The rules for adding and dropping fill words are delineated in documents generated by the T11 committee; *FC-PH, FC-PH2, FC-PH3, FC-AL, FC-AL2* and *FC-AL3*. By eliminating jitter transfer, compliance to signal quality standards is ensured.

In retimer mode, serial data enters CDRx where the clock is extracted from the data and the data is resynchronized to the recovered clock. This data is then input to a 4-word deep add/drop FIFO. Data is removed from the FIFO and retransmitted from FibreTimerx synchronously to the CMU’s bit rate clock derived from REFCLK. Since the retransmitted data is synchronized with the bit clock and not the recovered clock, jitter does not pass through the retimer. The output of the retimer is compliant with all Fibre Channel signal quality specifications.

Retimer mode is most useful when the output of the CDR is exiting a system which must meet Fibre Channel signal quality standards. Because the latency of the retimer is quite high, repeaters are preferable in situations where full Fibre Channel jitter compliance is not required.

Analog Signal Detect

The SDU of the VSC7147-0x has been modified from the VSC7147 to include an Analog Signal Detect (ASD) function, which is intended to eliminate crosstalk and small amplitude signals from incorrectly triggering the SDU in each FibreTimer. In order to provide backwards compatibility with the VSC7147-0x, ASD is disabled when pin 98 is HIGH. Pin 98 was a reserved pin in the VSC7147, which should have been pulled HIGH in all existing designs. When using the VSC7147-0x, pulling pin 98 LOW will enable the ASD function in both FibreTimers. The name for pin 98 has been changed from “RES” (VSC7147) to “ASDDIS” (VSC7147-0x).

Signal Detect Units (SDU)

Each FibreTimer cell is associated with an SDU that is used to determine if the input to the FibreTimer is a valid Fibre Channel signal. An ASD circuit monitors the input to the FibreTimer for valid levels in order to determine when the input is below a certain threshold. The output of the FibreTimer is monitored with two digital signal detection criteria aimed at confirming that the signal has the characteristics of Fibre Channel data.

The Sx and Mx inputs to the device determine which input buffer will be used as the ASD input to the SDU for each FibreTimer. Table 6 on page 13 identifies each condition.

The recovered clock from CDRx is divided down to provide a ~31µs period at 1.06Gb/s (or 15.5µs at 2.12Gb/s) during which two criteria are monitored:

1. Run length violations (more than five consecutive 0s or 1s).
2. The presence of a K28.5– symbol (which should occur every 20µs at 1.0625Gb/s or 10µs at 2.125Gb/s).

The SDUx output changes state every 2^{15} bit times, or ~31µs/15.5µs, depending on 1.0625Gb/s versus 2.125Gb/s.

The SDUs test the output of the CRUs for valid Fibre Channel data by looking for run length errors (more than five consecutive 1s or 0s) and the absence of a K28.5– character (0011111010). This K28.5– pattern should occur at least twice in every valid Fibre Channel frame and multiple times between frames. The maximum length of a Fibre Channel frame is 2148 bytes (or 21,480 encoded bits) and the SDU divides time into ~31µs/15.5µs time intervals (2^{15} bit times). At the end of each interval, any run length or K28.5– errors that occurred during the interval are stored internally for use by the state machine that drives the SDUx output.

RLL Detection

The SDUx Run Length Limit (RLL) detection scheme uses 32761-bit windows, and in between those windows are single 7-bit sections that are not included in the RLL detection. If RLL errors overlap into this 7-bit section from a 32761-bit window, or if an RLL starts within this 7-bit section and overlaps into a subsequent window, they will go undetected. More than 5 bits of the RLL must be in one of the 32761-bit windows for the RLL to be detected.

If an RLL does occur, but happens within the 7-bit void section, an RLL detection may not be indicated. As depicted in Figure 9, six sequential bits (0s or 1s) or more must occur in the 32761-bit windows for the digital signal detect to deassert. When the group of RLL bits overlap into the 7-bit section, with less than six of the RLL bits occurring within the 32761-bit window, the digital signal detect will stay asserted. This RLL scenario occurs in all modes and speeds.

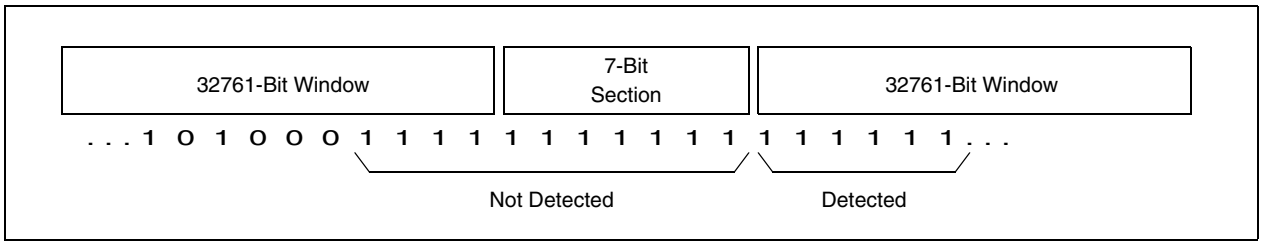


Figure 9. RLL Detection Cases

K28.5– Detection

The SDUx K28.5– character detection scheme uses 32761-bit windows, and in between those windows are single 7-bit sections that are not included in the K28.5– detection. If K28.5– characters overlap into this 7-bit section from a 32761-bit window, or if a K28.5– character starts within this 7-bit section and overlaps into a subsequent window, they will go undetected.

As depicted in Figure 10, an entire K28.5– character must be present in the 32761-bit windows for the digital signal detect to assert. Generally, six or more IDLE or fill words containing K28.5– characters exist in between frames of compliant Fibre Channel traffic. The occurrence of any delay in the assertion of the signal detect should not occur. Inversely, the occurrence of the deassertion of the signal detect due to this detection scheme should not occur. With the use of Fibre Channel-compliant data, the K28.5– character detection scheme will operate nominally. This K28.5– character detection scheme is present in all modes and speeds.

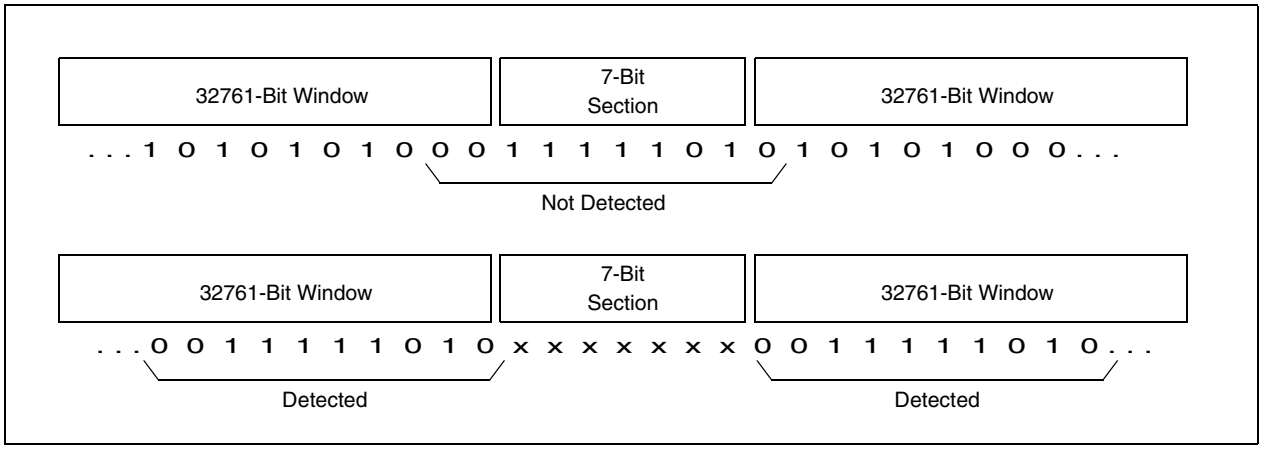


Figure 10. K28.5– Character Detection Cases

SDUSEL Operation

SDUSEL selects one of two different modes supported by the SDUs; single-frame (LOW) or multiple-frame (HIGH) error mode. In single-frame error mode, any error condition that occurs within the ~31µs/15.5µs time interval causes SDUx to be asserted LOW during the next interval. SDUx remains asserted until immediately after an error-free interval occurs. Single-frame error mode allows the user to develop their own algorithm for monitoring data and enabling external logic to control M7 or M8. In multiple-frame error mode, SDUx is asserted after four consecutive ~31µs/15.5µs time intervals containing errors and remains asserted until four consecutive error-free intervals occur. Multiple-frame error mode allows M7 or M8 to directly control SDU1 or SDU2, which configures the port to bypass I0+/– or I7+/– whenever valid data is not present.

Analog Signal Detect (ASD)

The ASD monitors the selected input to the FibreTimer for adequate amplitude. This criteria will fail if the signal is under 45mV differential peak-to-peak or pass if over 200mV differential peak-to-peak. This criteria is indeterminate if the input is between 45mV and 200mV. This criteria is checked during the same ~31µs/15.5µs interval as the digital criteria. Refer to Table 6 on page 13 for enabling ASD on specific high-speed input buffers.

Table 6: Input Buffer Selection

S1	S2	S3	S4	S5	S6	M7	M8	M9	M10	Source for SDU1	Source for SDU2
x	x	x	x	x	1	0	x	x	0	I6	-
x	x	x	x	1	0	0	x	x	0	I5	-
x	x	x	1	0	0	0	x	x	0	I4	-
x	x	1	0	0	0	0	x	x	0	I3	-
x	1	0	0	0	0	0	x	x	0	I2	-
1	0	0	0	0	0	0	x	x	0	I1	-
x	x	x	x	x	x	x	x	x	1	I0	-
x	x	x	x	x	x	1	x	1	0	I7	I7
x	x	x	x	x	1	1	x	0	0	I6	I6
x	x	x	x	1	0	1	x	0	0	I5	I5
x	x	x	1	0	0	1	x	0	0	I4	I4
x	x	1	0	0	0	1	x	0	0	I3	I3
x	1	0	0	0	0	1	x	0	0	I2	I2
1	0	0	0	0	0	1	x	0	0	I1	I1
0	0	0	0	0	0	x	1	0	1	I0	I0
x	x	x	x	x	x	x	x	1	x	-	I7
x	x	x	x	x	1	x	x	0	x	-	I6
x	x	x	x	1	0	x	x	0	x	-	I5
x	x	x	1	0	0	x	x	0	x	-	I4
x	x	1	0	0	0	x	x	0	x	-	I3
x	1	0	0	0	0	x	x	0	x	-	I2
1	0	0	0	0	0	x	x	0	x	-	I1

NOTE: *Assumes ASDDIS is LOW. All other conditions disable ASD.*

Speed Indicators

Each FibreTimer cell has an output, SFTx, which indicates the speed of the input data as shown in Table 7. The SFTx outputs are synchronized to the same interval timer as the signal detect outputs (SDUx). These outputs may be used by an external device to control the F/Sx input in order to set the speed of the FibreTimers.

Table 7. Speed Selection Truth Table

F/Sx Input	Input Data Rate	SFTx Output
LOW	1.06Gb/s	LOW
LOW	2.12Gb/s	HIGH(1)
HIGH	1.06Gb/s	LOW
HIGH	2.12Gb/s	HIGH

1. *If F/Sx is LOW (operating at 1.0625Gb/s), but the incoming data rate is 2.12Gb/s, the SFTx outputs could be intermittent. This intermittent behavior should be carefully considered when setting the F/Sx pins.*

The method for determining the SFTx output is to count the number of serial data negative edges coming through the FibreTimers. Because of the nature of this method, it is remotely possible that accurate results from the SFTx output

may be intermittent when F/Sx is LOW and the input data rate equals 2.12Gb/s. Therefore, SFTx should not be connected directly to F/Sx. Some combination of external logic or an Enclosure Management Controller is required to configure F/Sx properly by extracting the actual data rate from the SFTx output behavior. Otherwise, it is recommended to strap the VSC7147-0x for either 1.06Gb/s or 2.12Gb/s operation.

Auto-Speed Negotiation

The VSC7147-0x is not capable of implementing Auto-Speed Negotiation for speed selection as a standalone unit. However, if a dual speed (1Gb/s and 2Gb/s) transceiver (SerDes) is located nearby, the Tx and Rx speed selects of the SerDes would be tied to the VSC7147-0x F/Sx speed selects. The protocol controller and/or local microprocessor that controls the SerDes will actually be controlling both the SerDes and the VSC7147-0x.

Input Structures

Two input structures exist in the VSC7147-0x; TTL and high-speed, differential inputs. The LVTTL inputs will interface with any TTL or 3.3V/5V CMOS outputs. The high-speed, differential inputs are intended to be AC-coupled per the *FC-PH* specification, but do not require any external termination if internal termination is utilized. Being AC-coupled, the high-speed, differential input buffers are biased at (V_{DD} • 0.75).

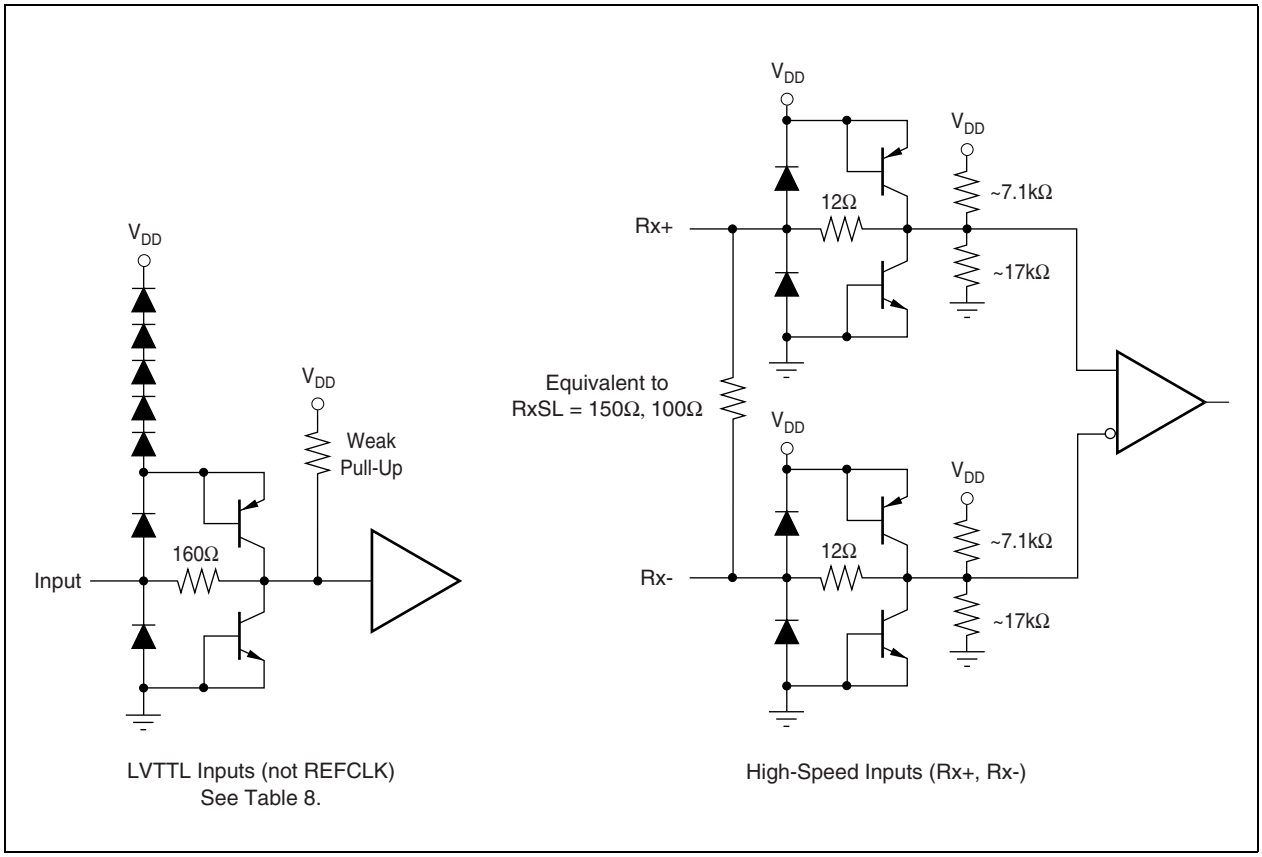


Figure 11. Input Structures

Output Structures

Two output structures exist in the VSC7147-0x; TTL and high-speed, differential outputs. The LVTTL outputs will interface with any TTL or 3.3V/5V CMOS inputs. The high-speed, differential outputs are intended to be AC-coupled per the *FC-PH* specification. The high-speed, differential outputs do not require external termination. Please refer to *Application Note AN-54* for recommended impedance matching guidelines.

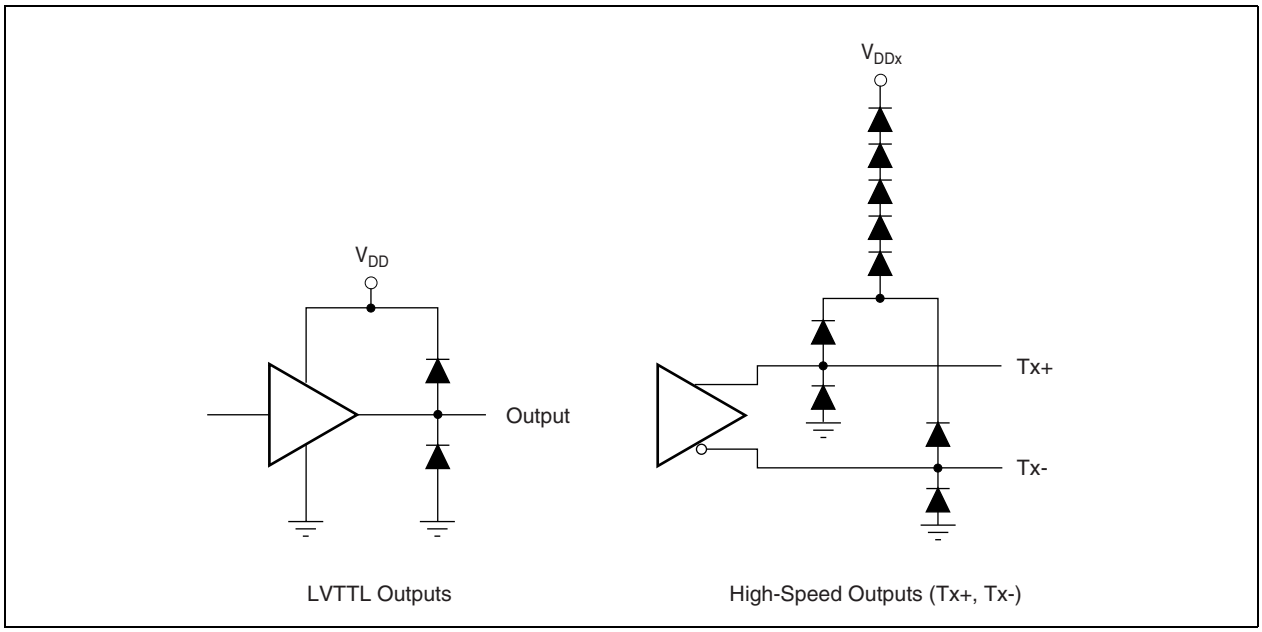


Figure 12. Output Structures

ELECTRICAL SPECIFICATIONS

DC Characteristics

Over Recommended Operating Conditions.

Table 8. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage (LVTTL)(1)	2.0		5.5	V	5V tolerant
V_{IL}	Input LOW voltage (LVTTL)(1)	0		0.8	V	
I_{IH}	Input HIGH current (LVTTL)(1)			40	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current (LVTTL) (1)			–100	µA	V_{IN} = 0.5V
V_{OH}	Output HIGH voltage (LVTTL)(1)	2.2			V	I_{OH} = –500µA
V_{OL}	Output LOW voltage (LVTTL)(1)			0.5	V	I_{OL}= +500µA
V_{DD}	Supply voltage	2.37	2.5	2.63	V	V_{DD} = 2.5V ±5%
P_D	Power dissipation		1.5	1.7	W	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current (total)		570	645	mA	Outputs open, V_{DD} = V_{DD} max
I_{DDA}	Supply current		60	80	mA	Outputs open, V_{DD} = V_{DD} max

1. The use of pull-up/pull-down resistors on these lines for the initial design is recommended. Use a 1kΩ resistor for pull-ups to 2.5V-5V lines. Use a 1kΩ resistor for pull-downs. Once the design is validated, connections directly to 2.5V-5V or GND are acceptable.

AC Characteristics

Over Recommended Operating Conditions.

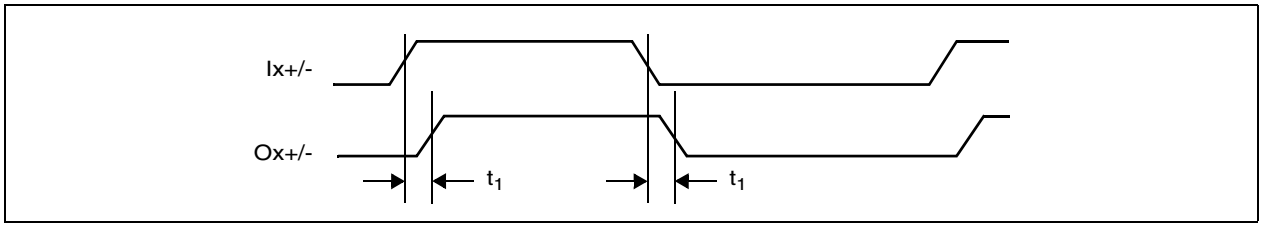


Figure 13. Timing Waveforms

Table 9. 1.0625Gb/s AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_1	Progration delay (repeater mode)			10	ns	Delay with all circuits bypassed.
t_1	Propagation delay (retimer mode)		100	200	bit times	Delay with all circuits bypassed.
t_R, t_F	Serial data rise and fall times	80	120	190	ps	At ΔV_{IN} minimum levels.
$t_{J(PBC)}$	Data jitter accumulation (PBC only)		30	60	ps	Peak-to-peak on Ox+/– in PBC mode.
$t_{J(RTMR)}$	Total data output jitter (retimer mode)		140	192	ps	Jitter generation at Ox+/– when driven by the CRU in retimer mode.
$t_{DJ(RTMR)}$	Serial data output deterministic jitter, peak-to-peak (retimer mode)		36	80	ps	Jitter generation at Ox+/– when driven by the CRU in retimer mode.
t_{JTOL}	Jitter tolerance	0.24			UI	Minimum eye opening for proper operation as defined in MJS 10.0, with a 400mVp-p differential swing.

NOTE: *Characteristics were derived using a 106.25MHz reference clock.*

Table 10. 2.125Gb/s AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_1	Progration delay (repeater mode)			7	ns	Delay with all circuits bypassed.
t_1	Propagation delay (retimer mode)		100	200	bit times	Delay with all circuits bypassed.
t_R, t_F	Serial data rise and fall times	80	116	190	ps	At ΔV_{IN} minimum levels.
$t_{J(PBC)}$	Data jitter accumulation (PBC only)		30	60	ps	Peak-to-peak on Ox+/– in PBC mode.
$t_{J(RTMR)}$	Total data output jitter (retimer mode)		100	117	ps	Jitter generation at Ox+/– when driven by the CRU in retimer mode.
$t_{DJ(RTMR)}$	Serial data output deterministic jitter, peak-to-peak (retimer mode)		35	61	ps	Jitter generation at Ox+/– when driven by the CRU in retimer mode.
t_{JTOL}	Jitter tolerance	0.30			UI	Minimum eye opening for proper operation as defined in MJS 10.0, with a 400mVp-p differential swing.

NOTE: *Characteristics were derived using a 106.25MHz reference clock.*

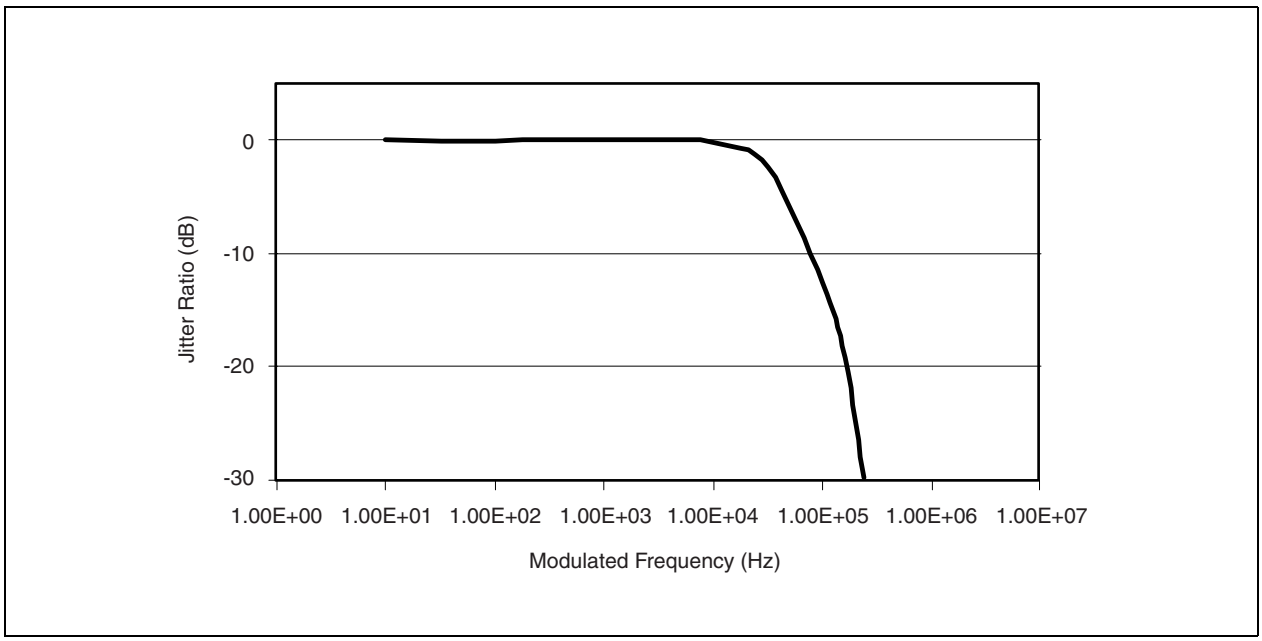


Figure 14. Repeater Jitter Transfer at 1.0625Gb/s (Typical Conditions)

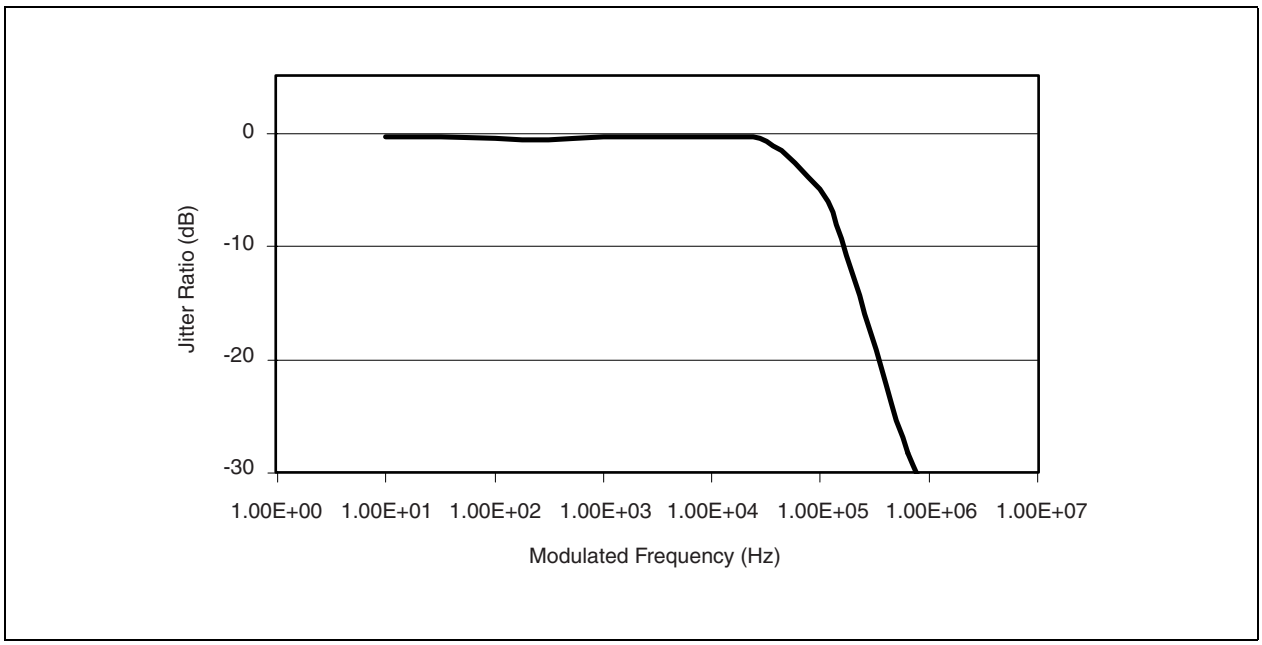


Figure 15. Repeater Jitter Transfer at 2.125Gb/s (Typical Conditions)

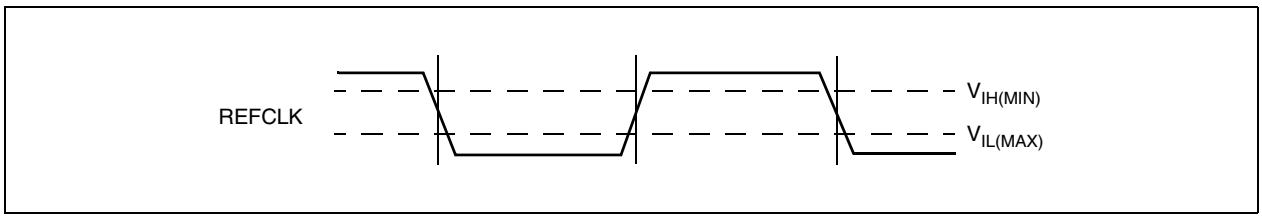


Figure 16. REFCLK Timing Waveform

Table 11. Reference Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units	Conditions
FR	Frequency range	105 52.5		107 53.5	MHz MHz	RFSEL = HIGH RFSEL = LOW
FO	Frequency offset	–200		+200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link.
DC	Duty cycle	35		65	%	Measured at 1.5V.
t_R, t_F	Rise and fall tImes			1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.

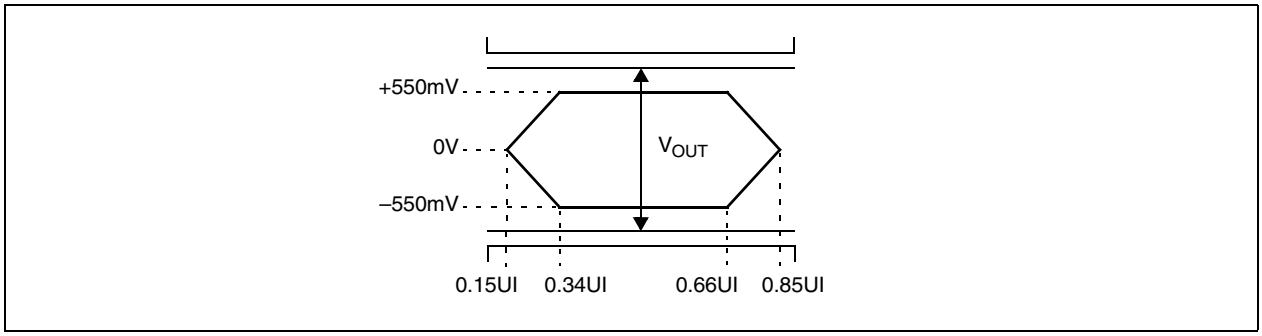


Figure 17. Amplitude Eye Diagram

Table 12. Amplitude AC Characteristics

Symbol	Parameter	Min(1)	Typ	Max(2)	Units	Conditions
ASD	Analog Signal Detection range	45(3)		200	mVp-p	AC-coupled.
V_{IN}	PECL input swing(4): (Ix+) – (Ix–)	200		2200	mVp-p	AC-coupled. Internally biased at V_{DD} • 0.75.
V_{OUT75}	PECL output swing(4): $[V_{OH}$ (Ox+) – V_{OL} (Ox+)] + [V_{OH} (Ox–) – V_{OL} (Ox–)]	1050	1325	2200	mVp-p	Refer to Figure 17.
V_{OUT50}	PECL output swing(4): $[V_{OH}$ (Ox+) – V_{OL}(Ox+)] + [V_{OH} (Ox–) – V_{OL} (Ox–)]	950	1200	2200	mVp-p	Refer to Figure 17.

1. *Measured eye amplitude (inside of eye).*
2. *Measured signal amplitude (outside of eye).*
3. *Note 2 applies to minimum measurement instead of Note 1.*
4. *Refer to Application Note AN-37 for details regarding differential voltage measurements.*

Table 13. Termination Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
	100Ω internal termination tolerance (target)	90	100	110	Ω	RPSL/RHSL pulled down to ground through a 100Ω 1% resistor.
	150Ω internal termination tolerance (target)	135	150	165	Ω	RPSL/RHSL pulled down to ground through a 150Ω, 1% resistor.
	Internal termination limits (target)	42		262	Ω	These limits may vary from part-to-part but are within the limits specified.

Recommended Operating Conditions

Table 14. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Power supply voltage	2.375	2.5	2.625	V
T	Operating temperature range at exposed pad[1]	0		+120	°C
	Operating temperature range at top of package[1]	0		+99	°C

1. Lower limit of specification is ambient temperature and upper limit is case temperature.

Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Power supply voltage	–0.5	+2.8	V
	DC input voltage, PECL	–0.5	V_{DD} + 0.5	V
	DC input voltage, LVTTL	–0.5	5.5	V
	DC voltage applied to LVTTL outputs	–0.5	V_{DD} + 0.5	V
	Output current, LVTTL and PECL	–50	+50	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature	–65	+150	°C
V_{ESD}	ESD voltage (Human Body Model)	–500	+500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

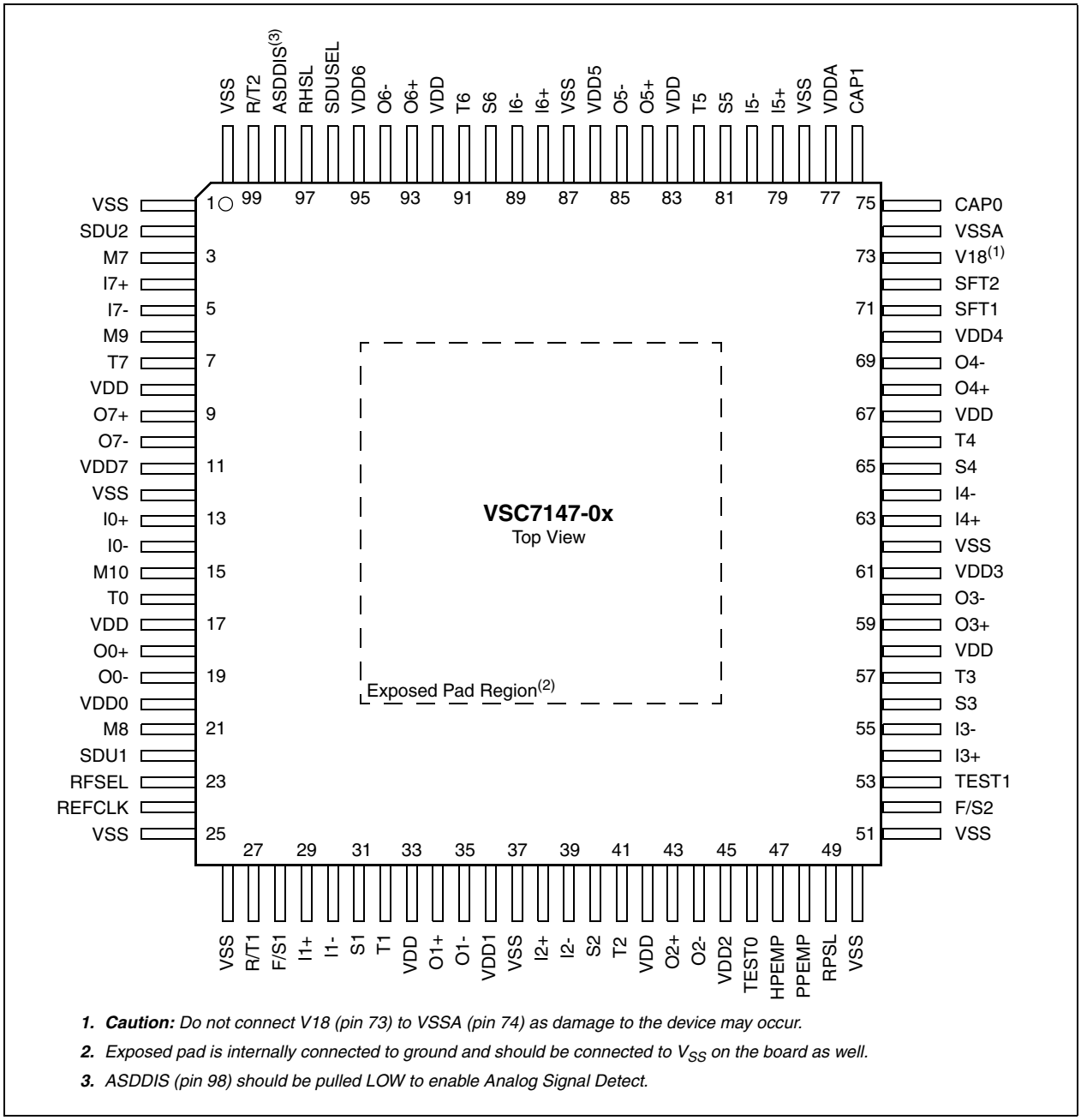
ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

The VSC7147-0x devices are available in two packages. VSC7147RM-0x is a 100-pin, exposed pad TQFP. The VSC7147XRM-0x is a lead-free, 100-pin exposed pad TQFP. Lead-free products from Vitesse comply with the temperatures and profiles defined in the JEDEC standard PC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

Pin Diagram



1. ***Caution:*** *Do not connect V18 (pin 73) to VSSA (pin 74) as damage to the device may occur.*
2. *Exposed pad is internally connected to ground and should be connected to V_{SS} on the board as well.*
3. *ASDDIS (pin 98) should be pulled LOW to enable Analog Signal Detect.*

Figure 18. Pin Diagram for 100-Pin Exposed Pad TQFP (RM)

Pin Identifications

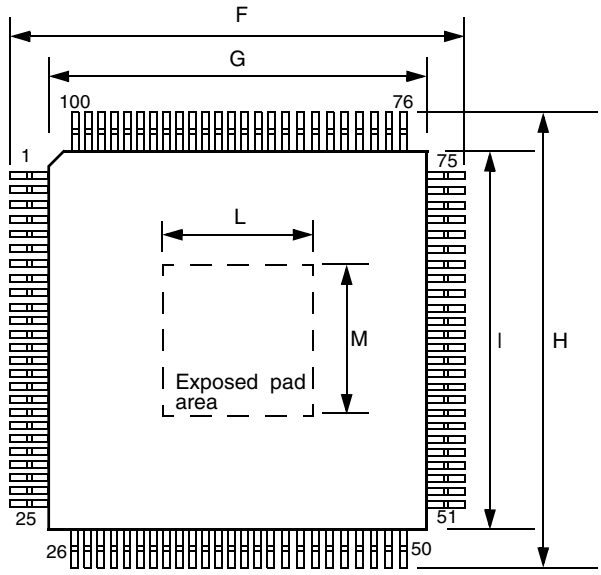
Table 16. Pin Identifications

Pin	Signal	I/O	Level	Description
18, 19, 34, 35 43, 44, 59, 60 68, 69, 84, 85 93, 94, 9, 10	O0+,O0–, O1+, O1– O2+, O2–, O3+, O3– O4+, O4–, O5+, O5– O6+, O6–, O7+, O7–	O	PECL	Differential, High-Speed Serial Output From PBCx to Disk Drive "x." AC-coupling recommended. ***NOTE:*** *22Ω to 35Ω series resistors are recommended for all outputs for impedance matching.*
13, 14, 29, 30 38, 39, 54, 55 63, 64, 79, 80 88, 89, 4, 5	I0+, I0–, I1+, I1– I2+, I2–, I3+, I3– I4+, I4–, I5+, I5– I6+, I6–, I7+, I7–	I	PECL	Differential, Serial Input From Disk Drive "x" to PBCx. AC-coupling recommended (biased internally at V_{DD} • 0.75). Internal terminations are included in each buffer and may be set to 100Ω or set to 150Ω as determined by the RHSL/RPSL inputs. ***NOTE:*** *Additional external components may be required for impedance matching.*
31, 40, 56, 65, 81 90, 3, 21, 6, 15	S1, S2, S3, S4, S5 S6, M7, M8, M9, M10	I	LVTTL	Configures PBCs and Configuration MUXs. When HIGH, the Sx input is enabled. When LOW, the Sx input is bypassed.
16, 32, 41, 57 66, 82, 91, 7	T0, T1, T2, T3 T4, T5, T6, T7	I	LVTTL	Transmit Enable Control for Ox+/– Output. When HIGH, the output is enabled. When LOW, the output is disabled such that the output is powered down and there is no output differential voltage (0V).
97	RHSL	I	Analog	Receiver Termination Control for Inputs I0 and I7. An external 1% resistor at the value of the desired differential impedance (i.e., 100Ω) should be used. This pin should not be left open.
49	RPSL	I	Analog	Receiver Termination Control for Inputs I1 through I6. An external 1% resistor at the value of the desired differential impedance (i.e., 100Ω) should be used. This pin should not be left open.
24	REFCLK	I	LVTTL	Reference Clock at 53.125MHz or 106.25MHz as determined by RFSEL. Used for internal CMU.
23	RFSEL	I	LVTTL	REFCLK Select. When HIGH, REFCLK is 106.25MHz. When LOW, REFCLK is 53.125MHz.
22 2	SDU1 SDU2	O	LVTTL	When LOW, indicates that the output of FibreTimerx does not contain valid Fibre Channel data.
27 99	R/T1 R/T2	I	LVTTL	When HIGH, FibreTimerx is configured as a repeater. When LOW, as a retimer.
28 52	F/S1 F/S2	I	LVTTL	When F/Sx is HIGH, FibreTimerx operates at 2.12Gb/s. When LOW, 1.0625Gb/s.
75 76	CAP0 CAP1		Analog	The on-chip PLL requires three external 0.1µF capacitors, connected between CAP0 and CAP1. Refer to Figure 6 on page 7.
96	SDUSEL	I	LVTTL	Selects the algorithm to drive the SDU1/SDU2 outputs. When HIGH, the multiple-frame error mode is used. When LOW, the single-frame error mode is selected.
71 72	SFT1 SFT2	O	LVTTL	Speed Indicators for Each FibreTimer. When HIGH, indicates the input of FibreTimerx is receiving 2.12Gb/s data. When LOW, indicates the input of FibreTimerx is receiving 1.0625Gb/s data.
46 53	TEST0 TEST1	I	LVTTL	LOW for factory test, HIGH for normal operation.

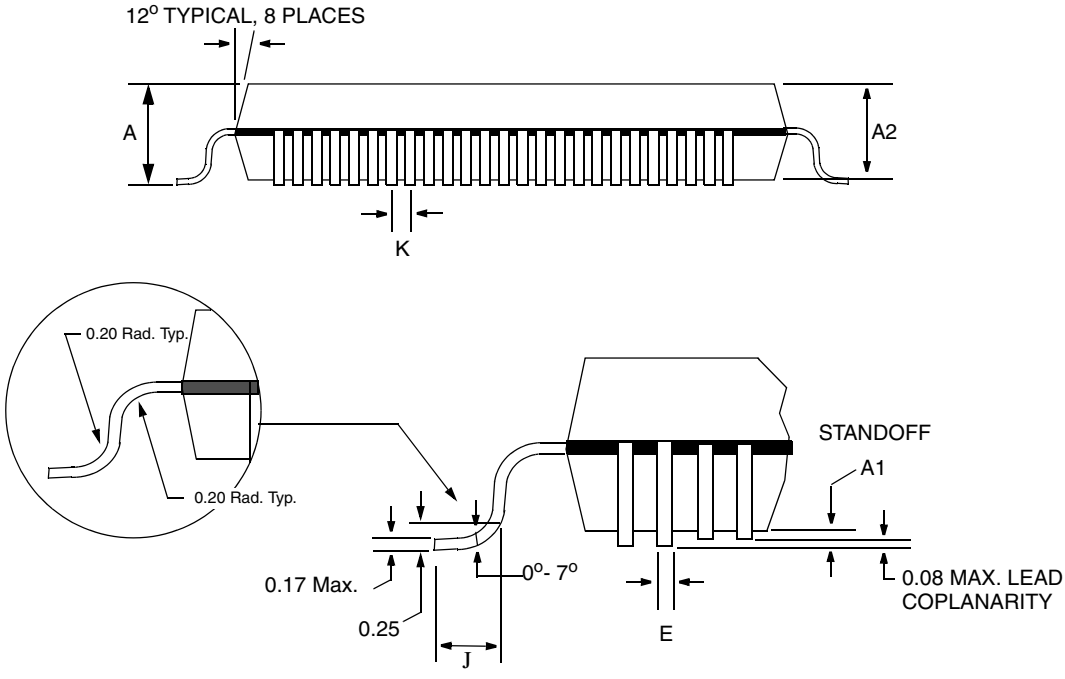
Table 16. Pin Identifications (continued)

Pin	Signal	I/O	Level	Description
47 48	HPEMP PPEMP	I	LVTTL	These pins control pre-emphasis functions on O0+/– and O7+/– (HPEMP) and O1+/– through O6+/– (PPEMP). HIGH will disable pre-emphasis. LOW will enable pre-emphasis.
98	ASDDIS	I	LVTTL	The ASD function is enabled when this input is pulled LOW. See Table 6 on page 13.
73	V18		Pwr	Internally Generated 1.8V Power Supply. Bypass to ground with a 0.1µF and at least a 4.7µF capacitor. ***Caution:*** *Do not connect this pin to VSSA (pin 74) as damage to the device may occur.*
8, 17, 33, 42, 58 67, 83, 92	VDD		Pwr	2.5V Power Supply
20, 36 45, 61 70, 86 95, 11	VDD0, VDD1 VDD2, VDD3 VDD4, VDD5 VDD6, VDD7		Pwr	2.5V Supply for PECL Drivers. V_{DDx} powers the Ox+/– output buffer. If the Ox+/– output is not used, connect VDDx to VSS.
77	VDDA		Pwr	Analog Power Supply, 2.5V for CMU PLL. Should be filtered separately from the other 2.5V supplies.
74	VSSA		Pwr	Analog Ground for the PLL.
1, 12, 25, 26, 37 50, 51, 62, 78 87, 100	VSS		Pwr	Ground

Package Drawing

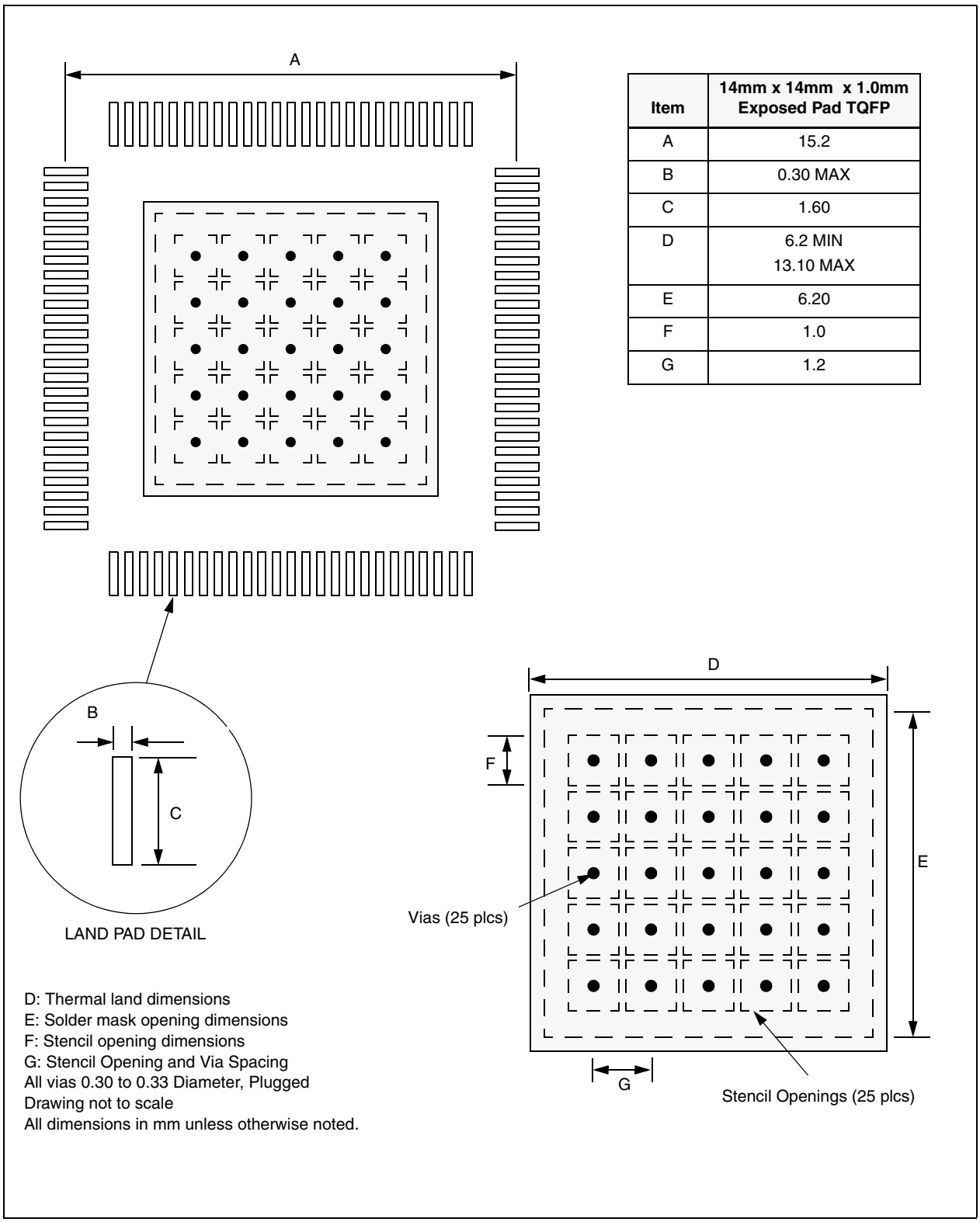


Item	14mm	Tolerance
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	16.00	±0.20
G	14.00	±0.05
H	16.00	±0.20
I	14.00	±0.05
J	0.60	±0.15
K	0.50	BASIC
L	5.7	BASIC
M	5.7	BASIC



NOTE: *Drawing not to scale. All units in mm unless otherwise specified.*

Figure 19. Package Drawing for 100-Pin Exposed Pad TQFP (RM)



Item	14mm x 14mm x 1.0mm Exposed Pad TQFP
A	15.2
B	0.30 MAX
C	1.60
D	6.2 MIN 13.10 MAX
E	6.20
F	1.0
G	1.2

Figure 20. Recommended Land Pattern

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

When the exposed pad is fully soldered to the ground pad, approximately 80% of the heat generated by the device is dissipated through the exposed pad and 20% through the top of the mold compound.

Table 17. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7147RM-01	15[1]	44	39	36
VSC7147RM-01	2.8[2]			
VSC7147XRM-01	15[1]	44	39	36
VSC7147XRM-01	4.0[2]			
VSC7147RM-05	15[1]	44	39	36
VSC7147RM-05	4.0[2]			
VSC7147XRM-05	15[1]	44	39	36
VSC7147XRM-05	4.0[2]			

1. *Simulated on the top of the mold compound with the exposed pad soldered to a ground pad on the PCB.*
2. *Calculated on the exposed pad soldered to a ground pad on the PCB.*

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC7147-0x Hex PBC with Dual Repeater/Retimer for 1.0625Gb/s and 2.125Gb/s FC-AL Disk Arrays

Part Number	Description
VSC7147RM-01	100-pin exposed pad TQFP, 14mm x 14mm x 1.0mm body, with Analog Signal Detect
VSC7147XRM-01	Lead-free 100-pin exposed pad TQFP, 14mm x 14mm x 1.0mm body, with Analog Signal Detect
VSC7147RM-05	100-pin exposed pad TQFP, 14mm x 14mm x 1.0mm body, with Analog Signal Detect IR reflow temperature profile: +250°C +0/–5°C per JEDEC standard IPC/JEDEC J-STD-020B.
VSC7147XRM-05	Lead-free 100-pin exposed pad TQFP, 14mm x 14mm x 1.0mm body, with Analog Signal Detect IR reflow temperature profile: +250°C +0/–5°C per JEDEC standard IPC/JEDEC J-STD-020B.

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