VITESSE

VSC7123
Datasheet

10-Bit Transceiver for Fibre Channel and Gigabit Ethernet

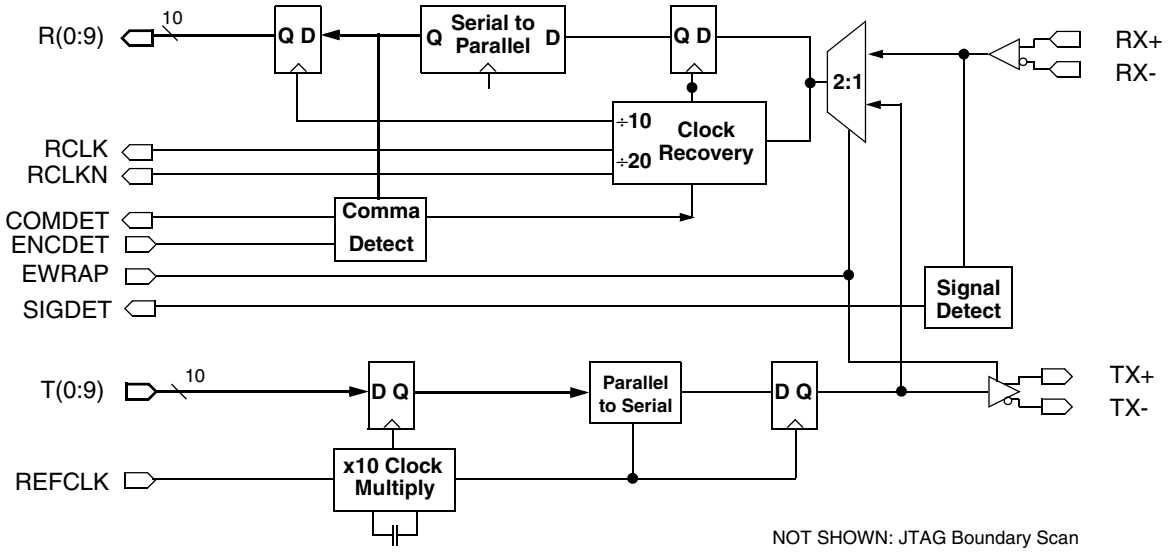
Features

- 802.3z Gigabit Ethernet-compliant 1.25 Gbps transceiver
- ANSI X3T11 Fibre Channel-compliant 1.0625 Gbps transceiver
- 0.98 to 1.36 Gbps full-duplex operation
- 10-Bit TTL interface for transmit and receive data
- Automatic lock-to-reference
- RX cable equalization
- Analog and digital signal detection
- JTAG access port for testability
- Single +3.3 V supply, 650 mW typical
- Packages: 64-pin 10 mm and 14 mm QFP and 10 mm and 14 mm TQFP

General Description

The VSC7123 is a full-speed Fibre Channel and Gigabit Ethernet transceiver with industry-standard pinouts. The VSC7123 accepts 10-bit 8B/10B encoded transmit data, latches it on the rising edge of REFCLK and serializes the data onto the TX PECL differential outputs at a baud rate, which is 10 times the REFCLK frequency. Serial data input on the RX PECL differential inputs is resampled by the Clock Recovery Unit (CRU) and deserialized onto the 10-bit receive data bus synchronously to complementary divide-by-twenty clocks. The VSC7123 receiver detects "Comma" characters for frame alignment. An analog/digital signal detection circuit indicates that a valid signal is present on the RX input. A cable equalizer compensates for InterSymbol Interference (ISI) to increase maximum cable distances. The VSC7123 is a higher performance, lower cost replacement for the VSC7125 and VSC7135.

Block Diagram



Functional Descriptions

Clock Synthesizer

The VSC7123 clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock between 0.98 GHz and 1.36 GHz. The on-chip Phase Lock Loop (PLL) uses a single external 0.1 µF capacitor to control the Loop Filter.

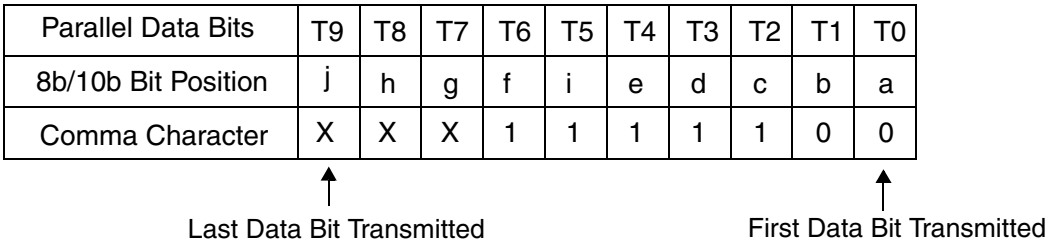
Serializer

The VSC7123 accepts TTL input data as a parallel 10-bit character on the T(0:9) bus, which is latched into the input register on the rising edge of REFCLK. This data is serialized and transmitted on the TX PECL differential outputs at a baud rate that is 10 times the frequency of the REFCLK, with bit T0 transmitted first. User data should be encoded using 8b/10b block code or the equivalent.

Transmission Character Interface

An encoded byte is 10 bits and is referred to as a transmission character. The 10-bit interface on the VSC7123 corresponds to a transmission character. This mapping is illustrated in the following illustration.

Figure 1 Transmission Order and Mapping of an 8b/10b Character



Clock Recovery

The VSC7123 accepts differential high-speed serial inputs on the RX+/RX- pins, extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for InterSymbol Interference which may be present in the incoming data. The serial bit stream should be encoded to provide DC balance and limited run length by an 8b/10b encoding scheme. The Clock Recovery Unit is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within ±200 ppm of 10 times the REFCLK frequency. For example, Gigabit Ethernet systems would use 125 MHz oscillators with a ±100 ppm accuracy resulting in ±200 ppm between VSC7123 pairs.

Deserializer

The recovered serial bit stream is converted into a 10-bit parallel output character. The VSC7123 provides complementary TTL recovered clocks, RCLK and RCLKN, which are $1/20^{th}$ of the serial baud rate. The clocks are generated by dividing down the high-speed recovered clock, which is phase-locked to the serial data. The serial data is retimed, deserialized and output on R(0:9). The parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN.

If serial input data is not present or does not meet the required baud rate, the VSC7123 continues to produce a recovered clock, allowing downstream logic functionality to continue. Under these circumstances, the RCLK/RCLKN output frequency differ from its expected frequency by no more than ±1%.

Word Alignment

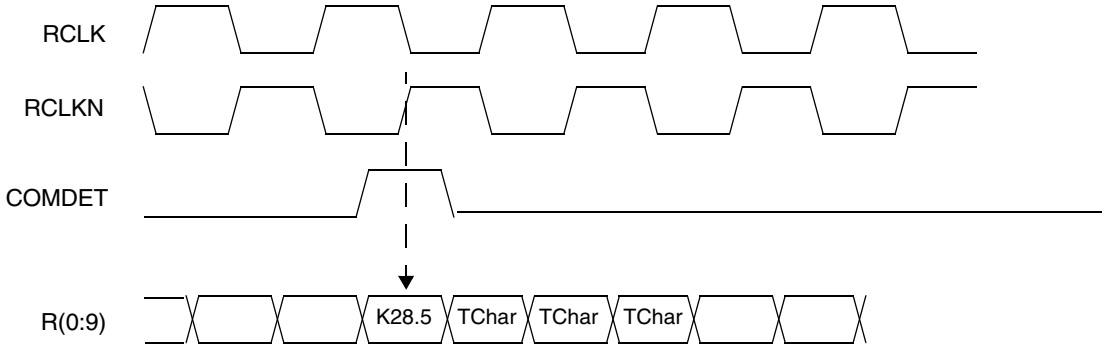
The VSC7123 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled by asserting ENCDET HIGH. When synchronization is enabled, the receiver examines the recovered serial data for the presence of the "Comma" character. This pattern is "0011111XXX", where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8b/10b coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5, and K28.7, which are defined for synchronization purposes. Improper alignment of the comma character is defined as any of the following conditions.

1. The comma is not aligned within the 10-bit transmission character such that R0...R6 = "0011111."
2. The comma straddles the boundary between two 10-bit transmission characters.
3. The comma is properly aligned but occurs in the received character presented during the rising edge of RFCLK rather than RCLKN.

When ENCDET is HIGH and an improperly aligned comma is encountered, the recovered clock is stretched (never slivered) so that the comma character and recovered clocks are properly aligned to R(0:9). This results in proper character and word alignment. When the parallel data alignment changes in response to a improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. Additionally, the first Comma pattern may also be lost or corrupted. Subsequent data will be output correctly and properly aligned. When ENCDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

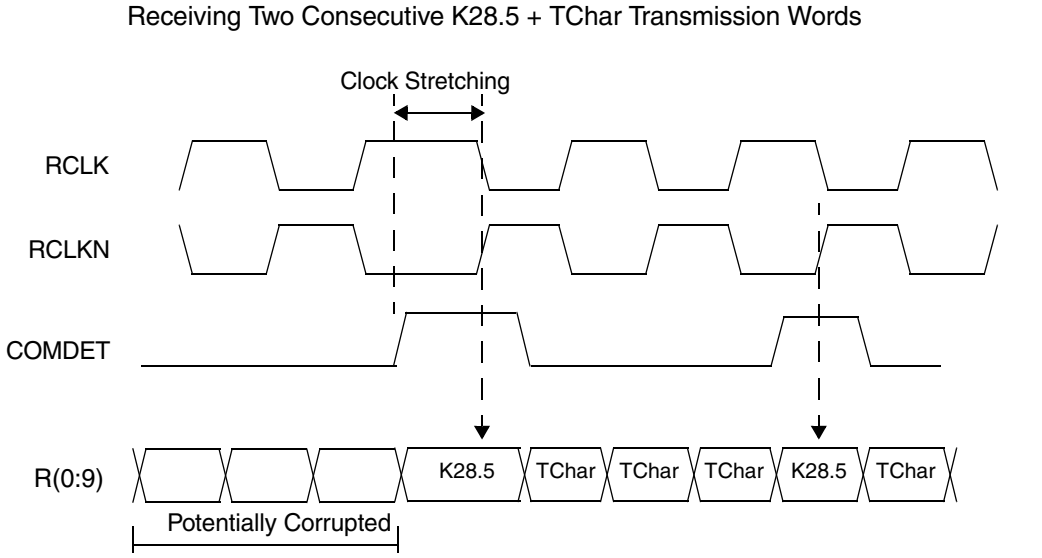
When encountering a comma character, COMDET is driven HIGH. The COMDET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COMDET signal is timed so that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 2 and Figure 3. Figure 2 shows the case when a comma character is detected and no phase adjustment is necessary. This figure illustrates the position of the COMDET pulse in relation to the comma character on R(0:9). Figure 3 shows the case where the K28.5 is detected, but it is misaligned so a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

Figure 2. Detection of a Properly Aligned Comma Character



TChar: 10-Bit Transmission Character

Figure 3. Detection and Resynchronization of an Improperly Aligned Comma



TChar: 10-Bit Transmission Character

Signal Detection

The receiver has an output, SIGDET, indicating, when HIGH, that the RX input contains a valid Fibre Channel or Gigabit Ethernet signal. A combination of one analog and three digital checks are used to determine if the incoming signal contains valid data. SIGDET is updated every four RCLKs. If during the current period, all four criteria are met, SIGDET will be HIGH during the next four RCLK periods. If during the current period, any of the four criteria is not met, SIGDET will be LOW during the next four RCLK periods.

1. Analog transition detection is performed on the input to verify that the signal swings are of adequate amplitude. The RX± input buffer contains a differential voltage comparator which goes HIGH if the differential peak-to-peak amplitude is greater than 400 mV or LOW if under 200 mV. If the amplitude is between 200 mV and 400 mV, the output is indeterminate.
2. Data on R(0:9) is monitored for all zeros (0000000000). If this pattern is encountered during the current RCLK interval, the SIGDET output goes LOW during the next four RCLK intervals.
3. Data on R(0:9) is monitored for all ones (1111111111). If this pattern is encountered during the current RCLK interval, the SIGDET output goes LOW during the next four RCLK intervals.
4. Data on R(0:9) is monitored for K28.5– (0011111010). Unlike previous patterns, the interval during which a K28.5– must occur is 64 K + 24 10-bit characters in length. Valid Fibre Channel or Gigabit Ethernet data contains a K28.5– character during any period of this length. If a K28.5– character is not detected during the monitoring period, SIGDET goes LOW during the next period.

The behavior of SIGDET is affected by EWRAP and ENCDET, as shown in Table 1. Note that COMDET, RCLK, RCLKN, and R(0:9) are unaltered by SIGDET.

Table 1. Signal Detect Behavior

EWRAP	ENCDET	COMDET	Transition Detect	All Zeros/ All Ones	K28.5 Presence	Mode
0	0	Disabled	Enabled	Enabled	Enabled	Normal
0	1	Enabled	Enabled	Enabled	Disabled	SIGDET ignores commas
1	0	Disabled	Enabled	Disabled	Disabled	Rollback
1	1	Enabled	Enabled	Disabled	Disabled	Loopback

JTAG Access Port

A JTAG Access Port is provided to assist in board-level testing. Through this port, most pins can be accessed or controlled and all TTL outputs can be tri-stated.

Electrical Specifications

AC Characteristics

Specifications listed in the following tables are guaranteed over the recommended operating conditions listed in Table 6 unless otherwise noted.

Figure 4. Transmit Timing Waveforms

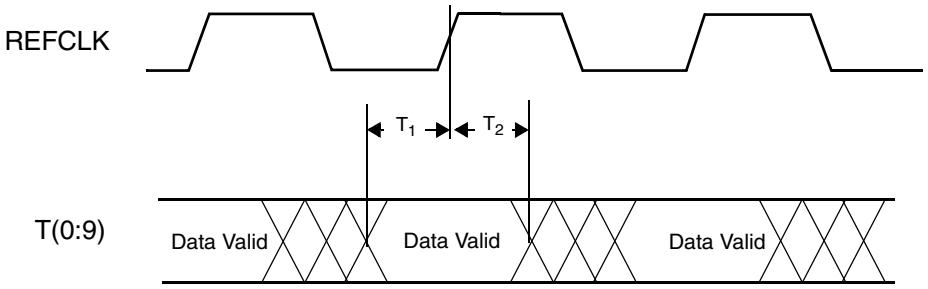


Table 2. Transmit AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
T_1	T(0:9) Setup time to the rising edge of REFCLK	1.5			ns	Measured between the valid data level of T(0:9) to the 1.4 V point of REFCLK.
T_2	T(0:9) hold time after the rising edge of REFCLK	1.0			ns	
T_{SDR},T_{SDF}	TX+/TX– rise and fall time			300	ps	20% to 80%, 50 Ω load to V_{DD} – 2.0.
T_{LAT}	Latency from rising edge of REFCLK to T0 appearing on TX+/TX–	8bc		8bc + 4 ns	ns	bc = Bit clocks ns = Nanosecond
Transmitter Output Jitter Allocation						
RJ	Random jitter (RMS)		5	8	ps	Measured at SO±, 1 sigma deviation of 50% crossing point.
DJ	Serial data output deterministic jitter (p-p)		30	80	ps	IEEE 802.3Z Clause 38.68, tested on a sample basis.

Figure 5. Receive Timing Waveforms

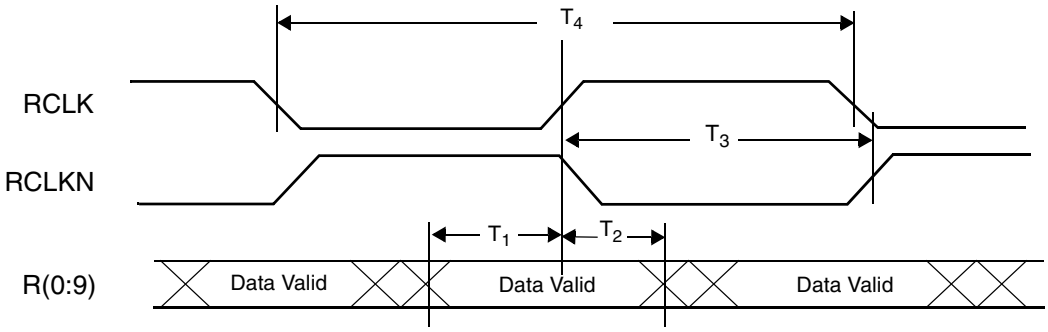


Table 3. Receive AC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Condition
T_1	TTL Outputs Valid prior to RCLK/RCLKN rise	4.0 3.0		ns	At 1.0625 Gbps At 1.25 Gbps
T_2	TTL Outputs Valid after RCLK or RCLKN rise	3.0 2.0		ns	At 1.0625 Gbps At 1.25 Gbps
T_3	Delay between rising edge of RCLK to rising edge of RCLKN	10 x T_{RX} –500	10 x T_{RX} +500	ps	T_{RX} is the bit period of the incoming data on Rx.
T_4	Period of RCLK and RCLKN	1.98 x T_{REFCLK}	2.02 x T_{REFCLK}	ps	Whether or not locked to serial data.
T_R, T_F	R(0:9), COMDET, SIGDET, RCLK and RCLKN rise and fall time		2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$, into 10 pF load.
R_{LAT}	Latency from RX to R(0:9)	12 bc + 1 ns	13 bc + 9 ns	bc ns	bc = bit clocks ns = nanoseconds
T_{LOCK}[1]	Data acquisition lock time		1400	bc	8b/10b pattern. bc = bit clocks

1. Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH revision 4.3.

Figure 6. REFCLK Timing Waveforms

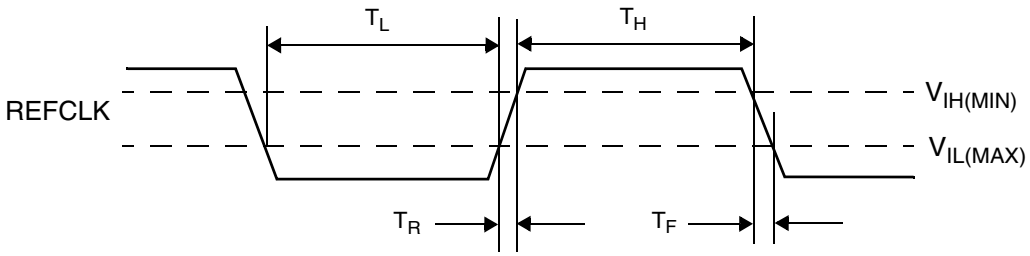
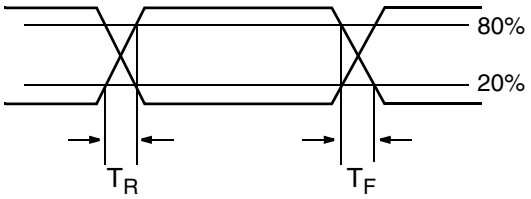


Table 4. Reference Clock Requirements

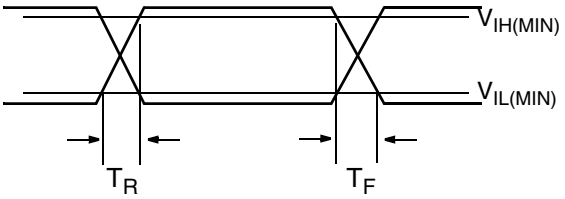
Symbol	Parameter	Minimum	Maximum	Unit	Condition
FR	Frequency range	98	136	MHz	Range over which both transmit and receive reference clocks on any link may be centered.
FO	Frequency offset	–200	200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link.
DC	REFCLK duty cycle	35	65	%	Measured at 1.5 V
T_R,T_F	REFCLK rise and fall time		1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
t_{REFCLK_JT}	REFCLK jitter tolerance		100	ps	Peak-to-peak total jitter for frequencies between 10 Hz and 7 MHz

Figure 7. Parametric Measurement Information

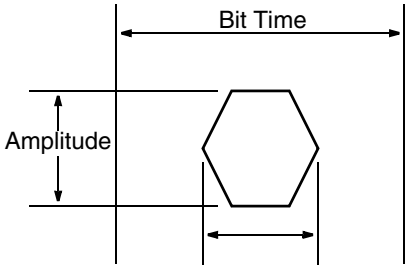
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time



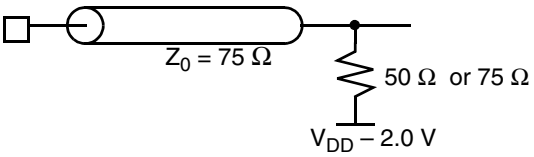
Receiver Input Eye Diagram Jitter Tolerance Mask



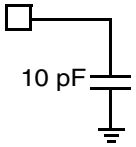
24% Minimum Eye Width%

Parametric Test Load Circuit

Serial Output Load



TTL AC Output Load



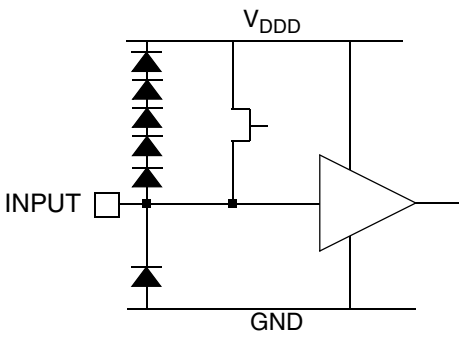
DC Characteristics

Specifications listed in the following tables are guaranteed over the recommended operating conditions listed in Table 6 unless otherwise noted. For differential measurement techniques, see Application Note, AN-37.

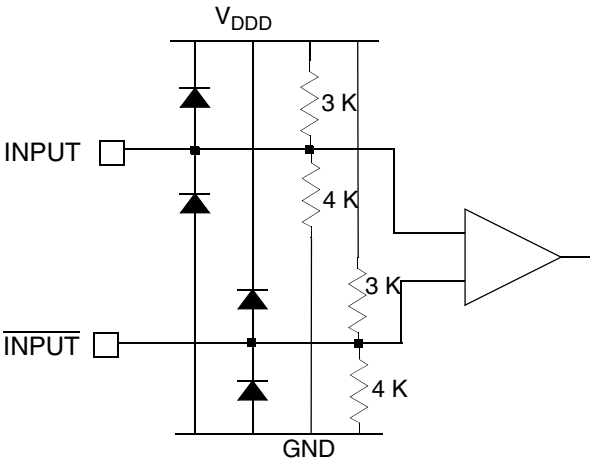
Table 5. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH voltage (TTL)	2.4			V	I_{OH} = –1.0 mA
V_{OL}	Output LOW voltage (TTL)			0.5	V	I_{OL} = 1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0		5.5	V	5 V tolerant inputs
V_{IL}	Input LOW voltage (TTL)	0		0.8	V	
I_{IH}	Input HIGH current (TTL)		50	500	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)			–500	µA	V_{IN} = 0.5 V
ΔV_{OUT75}[1]	TX output differential peak-to-peak voltage swing	1200		2200	mVp-p	75 Ω to V_{DD} – 2.0 V (TX+) – (TX–)
ΔV_{OUT50}[1]	TX output differential peak-to-peak voltage swing	1000		2200	mVp-p	50 Ω to V_{DD} – 2.0 V (TX+) –(TX–)
ΔV_{IN}[1]	RX Input differential peak-to-peak input sensitivity	300		2600	mVp-p	Internally biased to V_{DD} / 2 (RX+) – (RX–)
V_{DD}	Supply voltage	3.14		3.47	V	3.3 V ±5%
P_D	Power dissipation		650	900	mW	Outputs open, V_{DD} = V_{DD} maximum
I_{DD}	Supply current (all supplies)		190	260	mA	Outputs open, case temperature = 95 °C, V_{DD} = V_{DD} maximum
I_{DDA}	Analog supply current			100	mA	V_{DDA} = V_{DDA} maximum

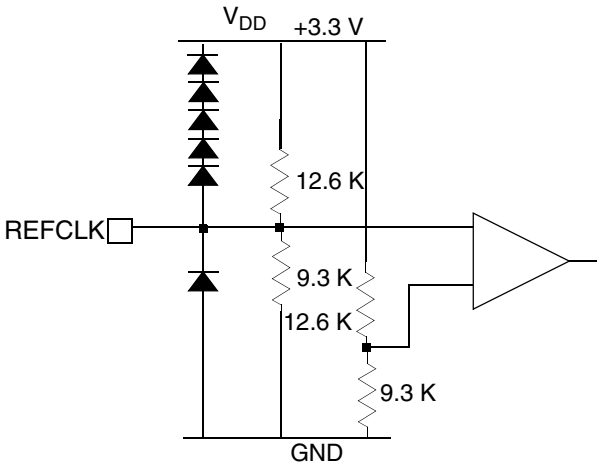
Figure 8. Input Structures



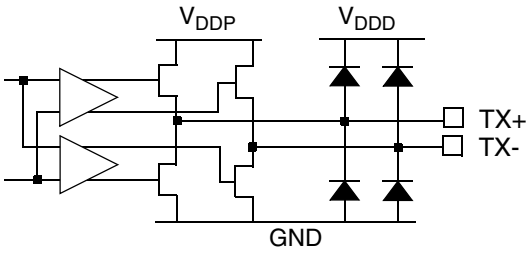
TTL Inputs (not REFCLK)



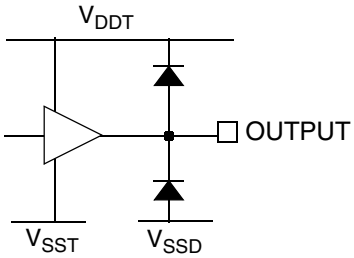
High-Speed Input (RX+/RX-)



REFCLK TTL Input



High-Speed Outputs (TX+/-)



TTL Outputs

Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}, V_{CCP}	Power supply voltage	3.135	3.3	3.465	V
T	Operating temperature for VSC7123RD, VSC7123XRD, VSC7123YW, and VSC7123XYW[1]	0		115	°C
T	Operating temperature for VSC7123QU, VSC7123QN, and VSC7123XQN[2]	0		105	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature measured at the exposed pad.

2. Lower limit of specification is ambient temperature, and upper limit is case temperature measured at the plastic case.

Maximum Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage	–0.5	4	V
	DC input voltage (PECL inputs)	–0.5	V_{DD} + 0.5	V
	DC input voltage (TTL inputs)	–0.5	5.5	V
	DC output voltage (TTL outputs)	–0.5	V_{DD} + 0.5	V
	Output current (TTL outputs)	–50	50	mA
	Output current (PECL outputs)	–50	50	mA
T_C	Case temperature under bias	–55	125	°C
T_S	Storage temperature	–65	150	°C
V_{ESD_HBM}	Electrostatic discharge voltage, human body model	–2000	2000	V
V_{ESD_CDM}	Electrostatic discharge voltage, charged device model	–1000	1000	V

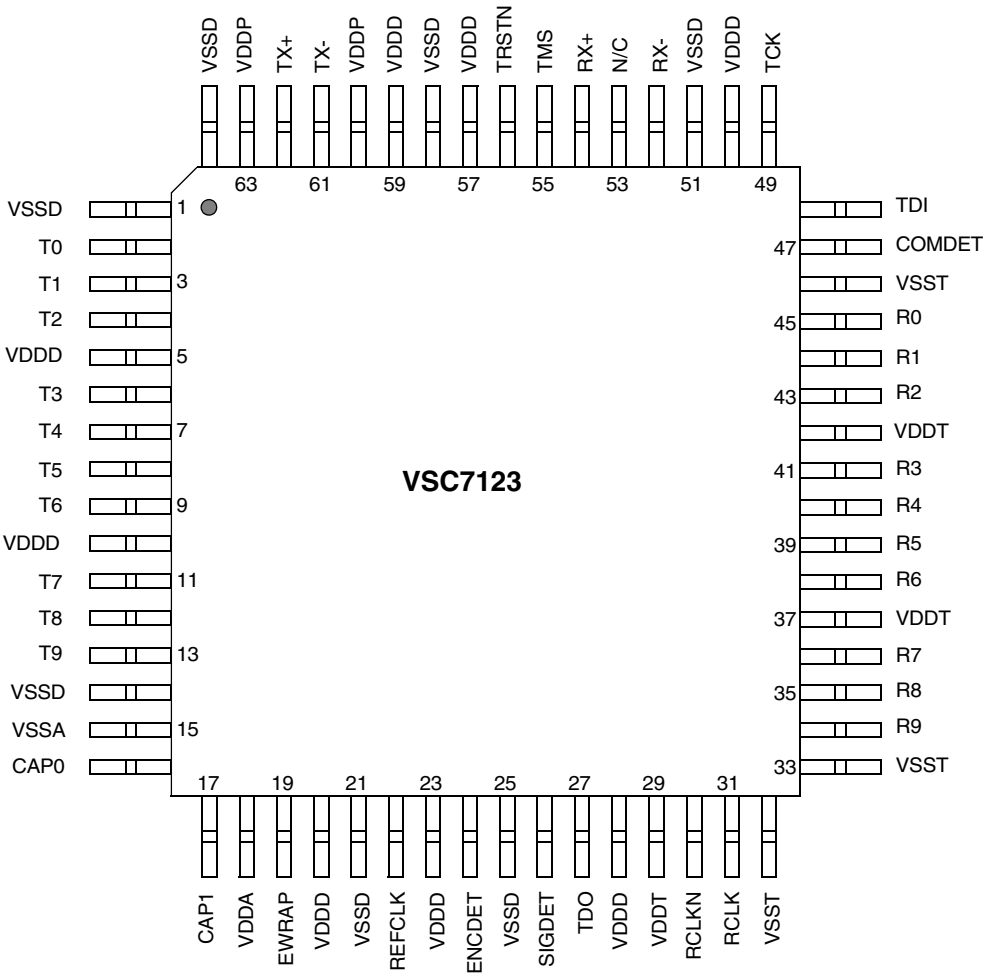
ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

Pin Descriptions

Pin Diagram

Figure 9. Pin Diagram (Top View)



Pin Identifications

Table 8. Pin Descriptions

Pin #	Name	Description
2,3,4,6 7,8,9,11 12,13	T0,T1,T2,T3 T4,T5,T6,T7 T8,T9	INPUTS - TTL: 10-bit transmit character. Parallel data on this bus is clocked in on the rising edge of REFCLK. The data bit corresponding to T0 is transmitted first.
22	REFCLK	INPUT - TTL: This rising edge of this clock latches T(0:9) into the input register. It also provides the reference clock, at one-tenth the baud rate to the PLL.
62, 61	TX+, TX–	OUTPUTS - Differential PECL (AC-coupling recommended): These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX– is LOW.
45,44,43,41 40,39,38,36 35,34	R0,R1,R2,R3 R4,R5,R6,R7 R8,R9	OUTPUTS - TTL: 10-bit received character. Parallel data on this bus is clocked out on the rising edges of RCLK and RCLKN. R0 is the first bit received on RX+/RX–.
19	EWRAP	INPUT - TTL: LOW for normal operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled. TX+ is held HIGH and TX– is held LOW.
54, 52	RX+, RX–	INPUTS - Differential PECL (AC-coupling recommended): The serial receive data inputs selected when EWRAP is LOW. Internally biased to VDD / 2, with 3.3 KΩ resistors from each input pin to VDD and GND.
31, 30	RCLK, RCLKN	OUTPUT - Complementary TTL: Recovered clocks derived from 1/20th of the RX± data stream. Each rising transition of RCLK or RCLKN corresponds to a new word on R(0:9).
24	ENCDET	INPUT - TTL: Enables COMDET and word resynchronization when HIGH. When LOW, keeps current word alignment and disables COMDET.
47	COMDET	OUTPUT - TTL: This output goes HIGH for half of an RCLK period to indicate that R(0:9) contains a comma character (‘0011111XXX’). COMDET goes HIGH only during a cycle when RCLKN is rising. COMDET is enabled by ENCDET being HIGH.
26	SIGDET	OUTPUT - TTL SIGnal DETect. This output goes HIGH when the RX input contains a valid Fibre Channel or Gigabit Ethernet signal. A LOW indicates an invalid signal.
16, 17	CAP0, CAP1	ANALOG: Differential capacitor for the CMU’s VCO, 0.1 µF nominal.
49	TCK	INPUT - TTL: JTAG clock input. Not normally connected.
48	TDI	INPUT - TTL: JTAG data input. Not normally connected.
55	TMS	INPUT - TTL: JTAG mode select input. Normally tied to V_{DDD}
56	TRSTN	INPUT - TLL: JTAG reset input. Tie to V_{SSD} for normal operation.
27	TDO	OUTPU - TTL: JTAG data output. Normally tri-stated.
18	VDDA	Analog power supply
15	VSSA	Analog ground
5,10,20,23 28,50,57,59	VDDD	Digital logic power supply
1,14,21,25 51,58,64	VSSD	Digital logic ground
29, 37, 42	VDDT	TTL output power supply
32, 33, 46	VSST	TTL output ground
60,63	VDDP	PECL I/O power supply
53	N/C	No internal connection

Package Information

The VSC7123 device is available in the following package types, including lead-free packages:

- VSC7123RD is a 64-pin, plastic thin quad flat pack (TQFP) with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.5 mm pin pitch. VSC7123XRD is the lead-free package.
- VSC7123YW is a 64-pin, plastic thin quad flat pack (TQFP) with an exposed pad, 14 mm × 14 mm body size, 1 mm body thickness, and 0.8 mm pin pitch. VSC7123XYW is the lead-free package.
- VSC7123QU is a 64-pin, thermally enhanced, plastic quad flat pack (QFP) with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.5 mm pin pitch.
- VSC7123QN is a 64-pin, thermally enhanced plastic quad flat pack (QFP) with a 14 mm × 14 mm body size, 2 mm body thickness, and 0.8 mm pin pitch. VSC7123XQN is the lead-free package.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and are modeled using an eight-layer test board. For more information, see the IPC and JEDEC standard.

Table 9. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7123RD	7	64.5	62.3	59.5
VSC7123XRD	7	64.5	62.3	59.5
VSC7123YW	6	63	61	58
VSC7123XYW	6	63	61	58
VSC7123QU	16	40	34	32
VSC7123QN	14.5	38	32	29
VSC7123XQN	14.5	38	32	29

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

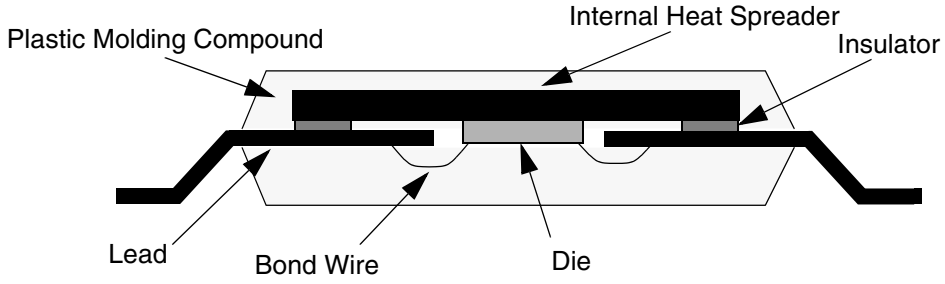
EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Package Thermal Considerations

The VSC7123QN, VSC7123XQN, and VSC7123QU use industry-standard EIAJ footprints that are enhanced to improve thermal dissipation The construction of these packages is shown in the following illustration.

Figure 10. Package Cross-Section for VSC7123QN, VSC7123XQN, and VSC7123QU



Note: The VSC7123RD, VSC7123XRD, VSC7123YW, and VSC7123XYW are packaged in an exposed pad TQFP. There is no internal heat spreader in any of these four packages.

Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020.

VSC7123RD, VSC7123XRD, VSC7123YW, VSC7123XYW, VSC7123QU, and VSC7123QN are rated moisture sensitivity level 3 or better.

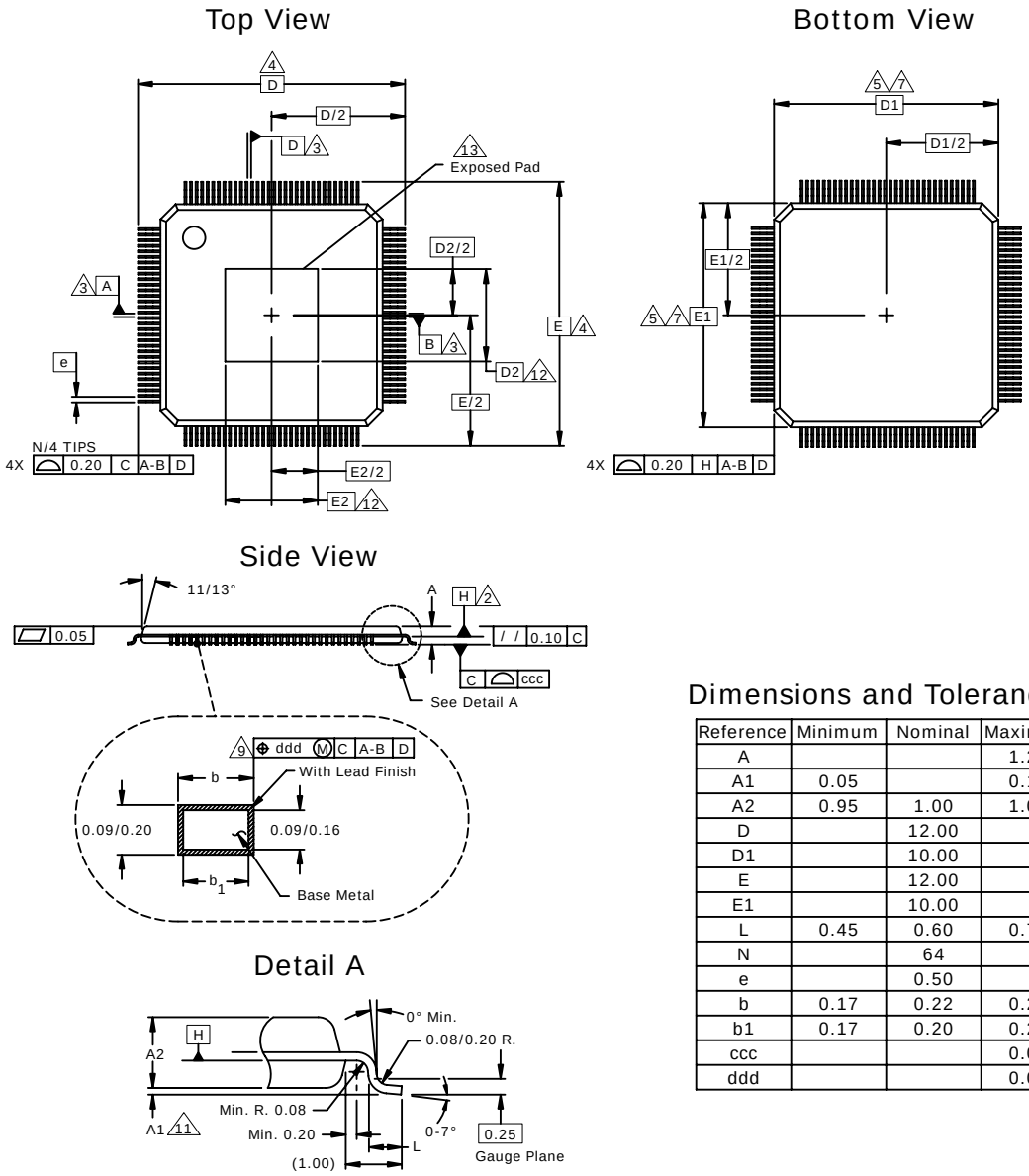
VSC7123XQN is rated moisture sensitivity level 4.

For more information, see the IPC and JEDEC standard.

Package Drawings

The following illustrations show the package drawings for the VSC7123 device.

Figure 11. Package Drawing for the VSC7123RD and VSC7123XRD



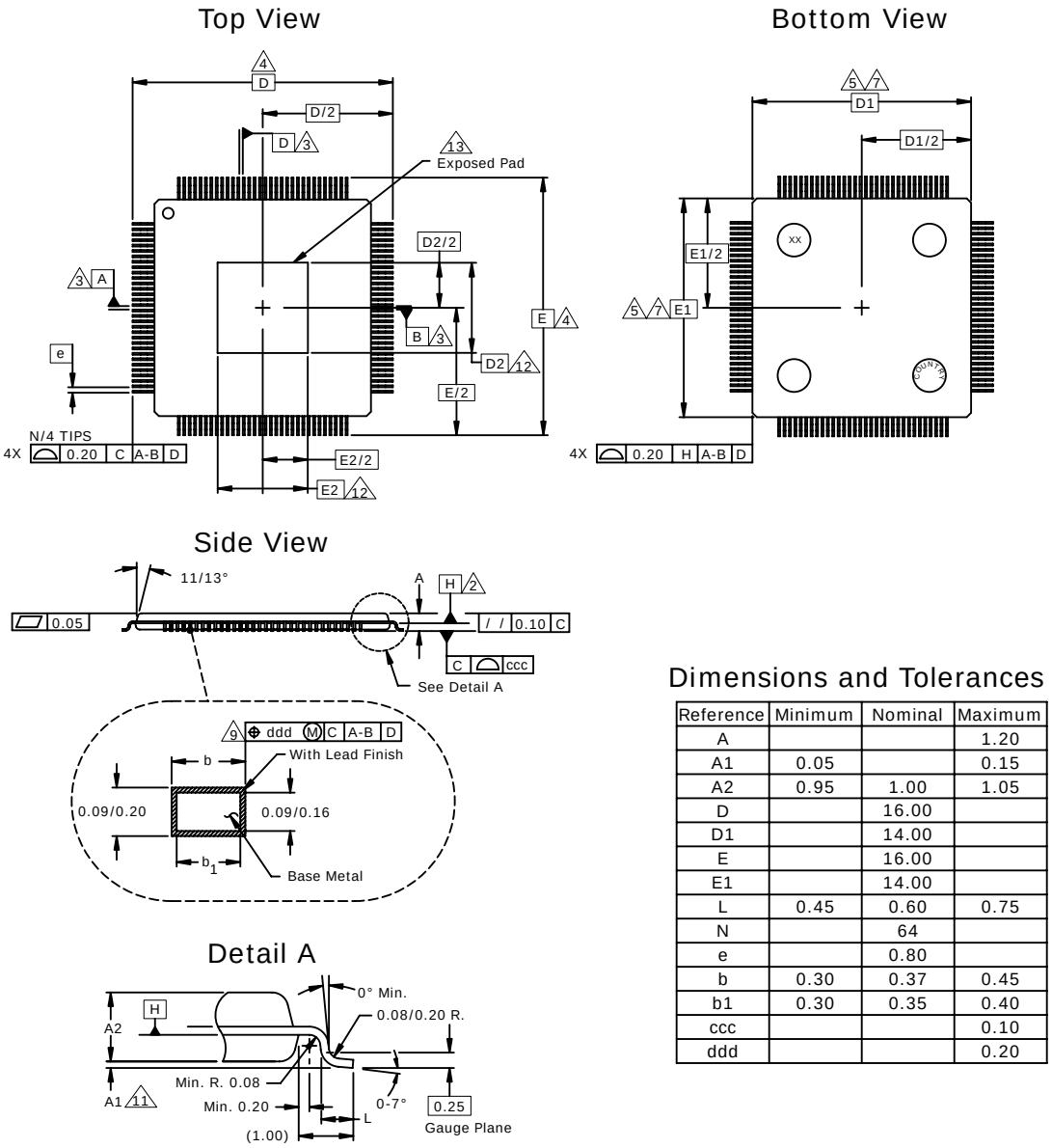
Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
L	0.45	0.60	0.75
N		64	
e		0.50	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
ccc			0.08
ddd			0.08

Notes

1. All dimensions and tolerances in millimeters.
2. Datum plane H located at the mold parting line and coincident with lead where lead exits plastic body at parting line.
3. Datums A-B and D to be determined at center line between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. N is the total number of terminals.
7. To be determined at datum plane H.
8. Package top dimensions are smaller than bottom dimensions, and top of package does not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion is 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. This outline conforms to JEDEC MS-026, variation ACD.
11. A1 is defined as the distance from the seating plane to lowest point of the package body.
12. Dimensions D2 and E2 represent the size of the exposed pad, which is 3.8 mm x 3.8 mm typical.
13. Exposed pad is coplanar with the top of the package.

Figure 12. Package Drawing for VSC7123YW and VSC7123XYW



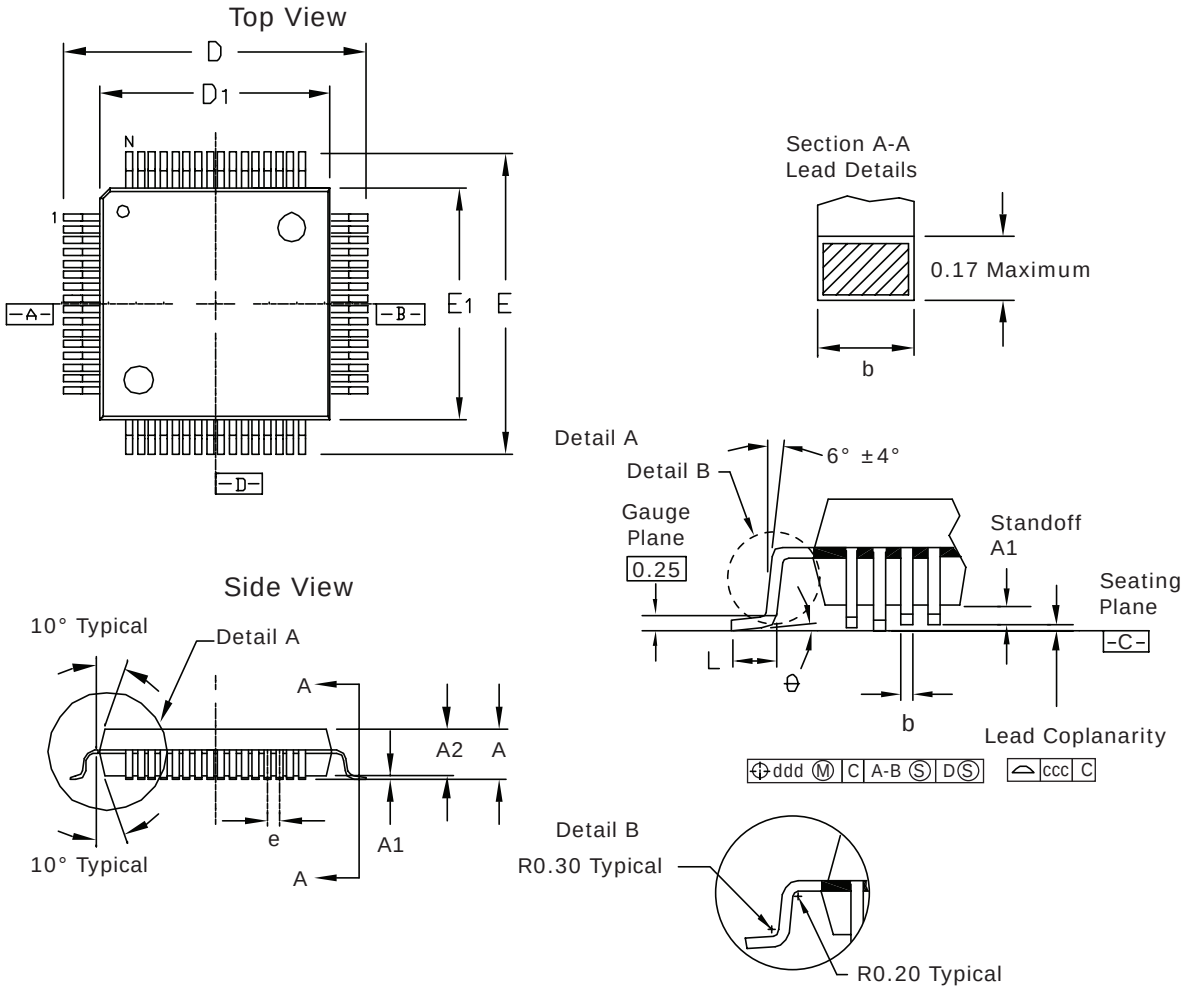
Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
D		16.00	
D1		14.00	
E		16.00	
E1		14.00	
L	0.45	0.60	0.75
N		64	
e		0.80	
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
ccc			0.10
ddd			0.20

Notes

1. All dimensions and tolerances in millimeters.
2. Datum plane H located at the mold parting line and coincident with lead where lead exits plastic body at parting line.
3. Datums A-B and D to be determined at center line between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. N is the total number of terminals.
7. To be determined at datum plane H.
8. Package top dimensions are smaller than bottom dimensions, and top of package does not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion is 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. This outline conforms to JEDEC MS-026, variation AEB.
11. A1 is defined as the distance from the seating plane to lowest point of the package body.
12. Dimensions D2 and E2 represent the size of the exposed pad, which is 4.0 mm x 4.0 mm typical.
13. Exposed pad is coplanar with the top of the package.

Figure 13. Package Drawing for VSC7123QU

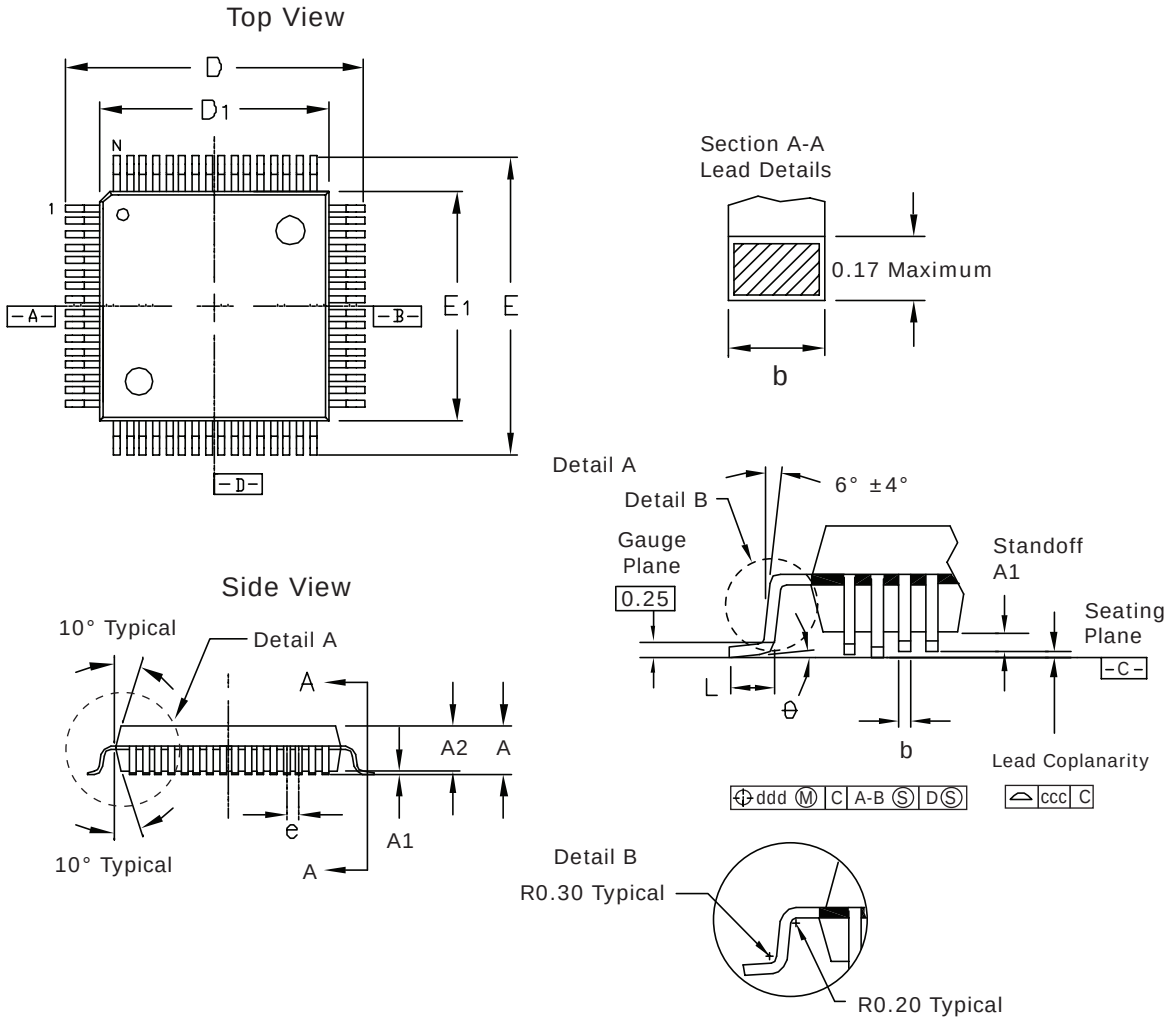


Notes

1. All dimensions in millimeters.
2. Dimensions shown are nominal with tolerances indicated.
3. Foot length L is measured at gauge plane 0.25 mm above seating plane.
4. N is the total number of leads.
5. This outline conforms to JEDEC MS-029, variation AA.

Reference	Minimum	Nominal	Maximum
A			2.50
A1	0.25		0.50
A2	1.95	2.00	2.10
D	12.95	13.20	13.45
D1	9.90	10.00	10.10
E	12.95	13.20	13.45
E1	9.90	10.00	10.10
L	0.73	0.88	1.03
N		64	
e		0.50	
b	0.17	0.22	0.27
θ		0° ~ 7°	
ddd			0.8
ccc			0.8

Figure 14. Package Drawing for VSC7123QN and VSC7123XQN



Notes

1. All dimensions in millimeters.
2. Dimensions shown are nominal with tolerances indicated.
3. Foot length L is measured at gauge plane 0.25 mm above seating plane.
4. N is the total number of leads.
5. This outline conforms to JEDEC MO-108, variation BC-1.

Reference	Minimum	Nominal	Maximum
A			2.45
A1			0.25
A2	1.95	2.00	2.10
D	16.95	17.20	17.45
D1	13.90	14.00	14.10
E	16.95	17.20	17.45
E1	13.90	14.00	14.10
L	0.78	0.88	1.03
N		64	
e		0.80	
b	0.30	0.35	0.40
θ		0° ~ 7°	
ddd		0.20	
ccc			0.10

Ordering Information

The VSC7123 device is available in the following package types, including lead-free packages:

- VSC7123RD is a 64-pin, plastic thin quad flat pack (TQFP) with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.5 mm pin pitch. VSC7123XRD is the lead-free package.
- VSC7123YW is a 64-pin, plastic thin quad flat pack (TQFP) with an exposed pad, 14 mm × 14 mm body size, 1 mm body thickness, and 0.8 mm pin pitch. VSC7123XYW is the lead-free package.
- VSC7123QU is a 64-pin, thermally enhanced, plastic quad flat pack (QFP) with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.5 mm pin pitch.
- VSC7123QN is a 64-pin, thermally enhanced, plastic quad flat pack (QFP) with a 14 mm × 14 mm body size, 2 mm body thickness, and 0.8 mm pin pitch. VSC7123XQN is the lead-free package.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Table 10. Ordering Information

Part Number	Description
VSC7123RD	64-pin, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.5 mm pin pitch
VSC7123XRD	Lead-free, 64-pin, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.5 mm pin pitch
VSC7123YW	64-pin, plastic TQFP with an exposed pad, 14 mm × 14 mm body size, 1 mm body thickness, and 0.8 mm pin pitch
VSC7123XYW	Lead-free, 64-pin, plastic TQFP with an exposed pad, 14 mm × 14 mm body size, 1 mm body thickness, and 0.8 mm pin pitch
VSC7123QU	64-pin, thermally enhanced, plastic QFP with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.5 mm pin pitch
VSC7123QN	64-pin, thermally enhanced, plastic QFP with a 14 mm × 14 mm body size, 2 mm body thickness, and 0.8 mm pin pitch
VSC7123XQN	Lead-free, 64-pin, thermally enhanced, plastic QFP with a 14 mm × 14 mm body size, 2 mm body thickness, and 0.8 mm pin pitch

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