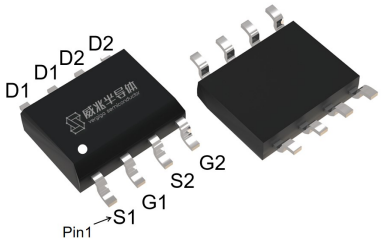
V_{DS}	40	V
$R_{DS(on),TYP}$@ V_{GS}=10V	8.1	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5V	11	mΩ
I_D	11	A

Features

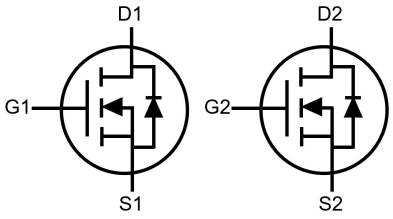
- Enhancement mode
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

SOP8



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS4620DS-G	SOP8	4620DS	3000pcs/Reel



Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_A = 25°C	1.7	A
I_D	Continuous drain current @VGS=10V	T_A = 25°C	11	A
I_D	Continuous drain current @VGS=10V	T_A = 70°C	9	A
I_{DM}	Pulse drain current tested ①	T_A = 25°C	44	A
EAS	Avalanche energy, single pulsed ②		64	mJ
P_D	Maximum power dissipation ③	T_A = 25°C	2	W
		T_A = 70°C	1.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter		Typical	Max	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead		23	28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient④	t≤10s	52	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient④	Steady State	78	94	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃) ⑤	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.3	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑥	V_{GS}=10V, I_D=10A	--	8.1	10.5	mΩ
		Tj=100℃ ⑤	--	10	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ⑥	V_{GS}=4.5V, I_D=6A	--	11	14	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑤	V_{DS}=20V,V_{GS}=0V, f=1MHz	--	870	--	pF
Coss	Output Capacitance ⑤		--	265	--	pF
Crss	Reverse Transfer Capacitance ⑤		--	20	--	pF
Rg	Gate Resistance	f=1MHz	--	1.8	--	Ω
Qg(10V)	Total Gate Charge ⑤	V_{DS}=20V,I_D=10A, V_{GS}=10V	--	13	--	nC
Qg(4.5V)	Total Gate Charge ⑤		--	6.3	--	nC
Qgs	Gate-Source Charge ⑤		--	2.7	--	nC
Qgd	Gate-Drain Charge ⑤		--	1.6	--	nC
Switching Characteristics ⑤						
Td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=10A, R_G=3Ω, V_{GS}=10V	--	5.6	--	ns
Tr	Turn-on Rise Time		--	29	--	ns
Td(off)	Turn-Off Delay Time		--	15	--	ns
Tf	Turn-Off Fall Time		--	4.6	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=10A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑤	I_{sd}=10A, V_{GS}=0V di/dt=100A/μs	--	18	--	ns
Qrr	Reverse Recovery Charge ⑤		--	7	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② EAS of 64mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 16A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 9A.

③ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

④ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑤ Guaranteed by design, not subject to production testing.

⑥ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

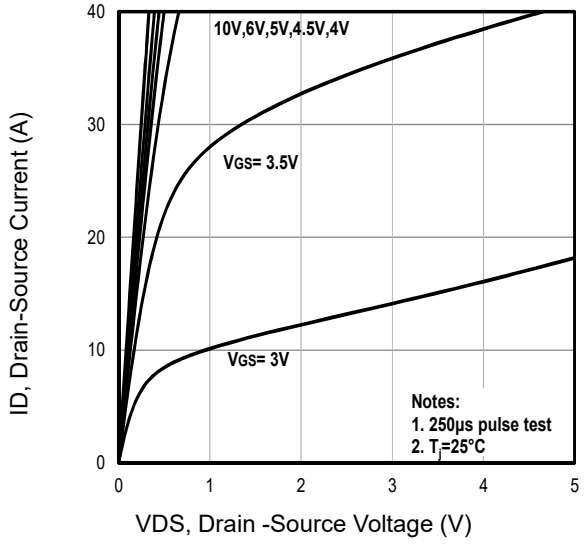


Fig1. Typical Output Characteristics

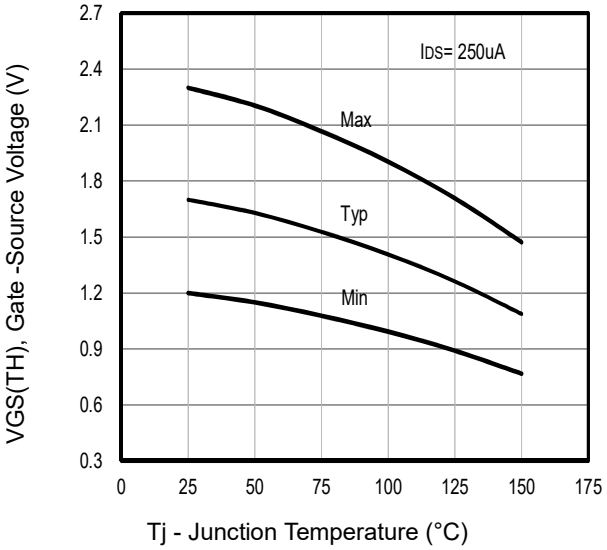


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

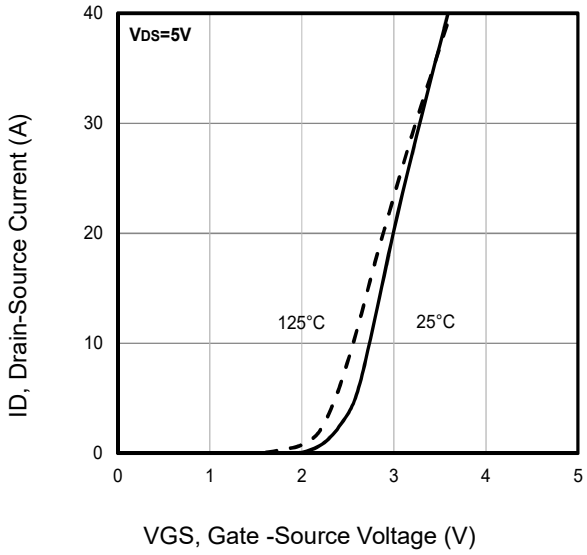


Fig3. Typical Transfer Characteristics

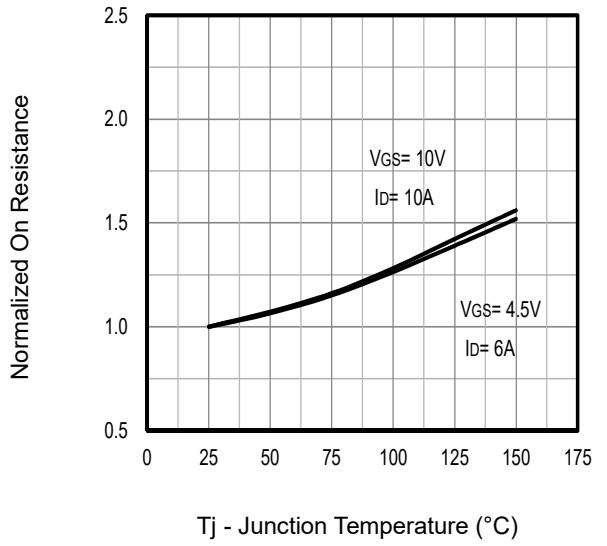


Fig4. Typical Normalized On-Resistance Vs. Tj

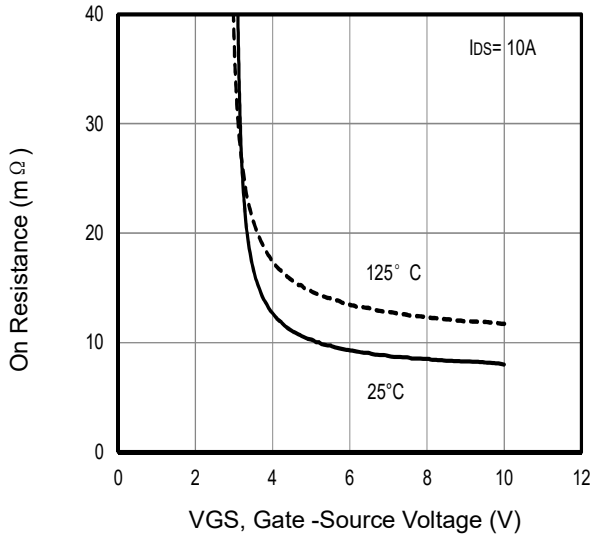


Fig5. Typical On Resistance Vs Gate -Source Voltage

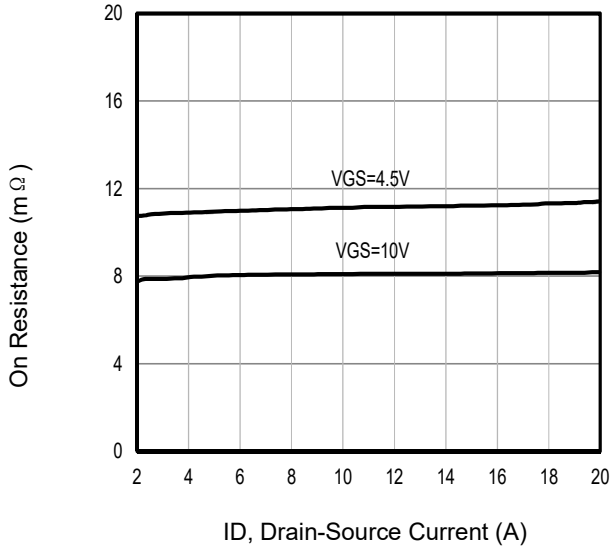


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

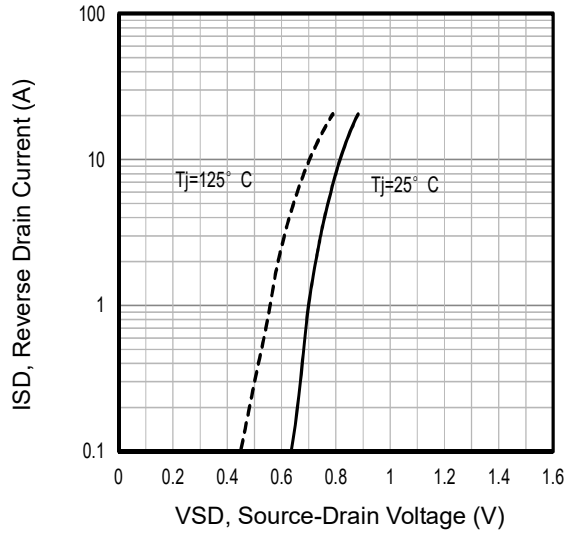


Fig7. Typical Source-Drain Diode Forward Voltage

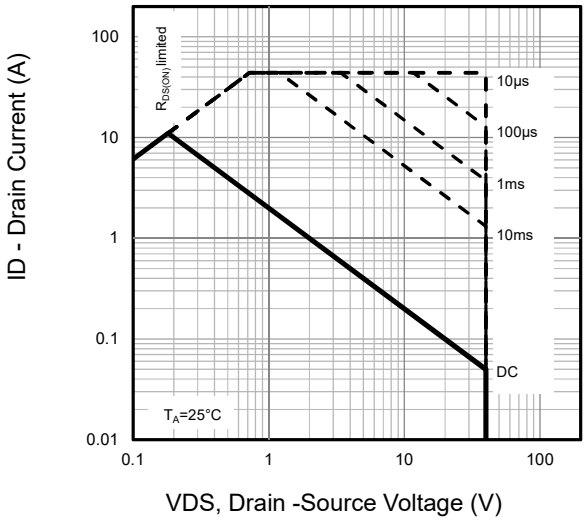


Fig8. Maximum Safe Operating Area

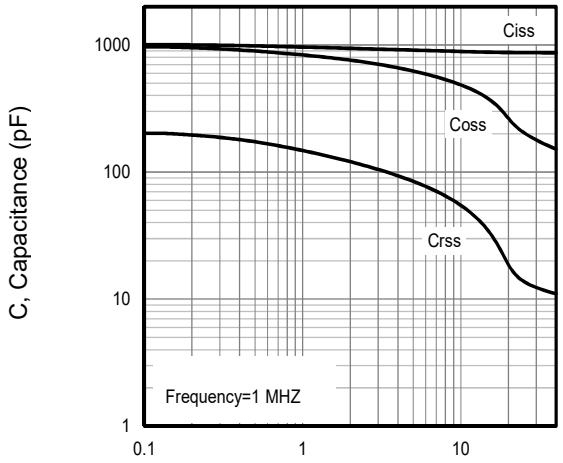


Fig9. Typical Capacitance Vs. Drain-Source Voltage

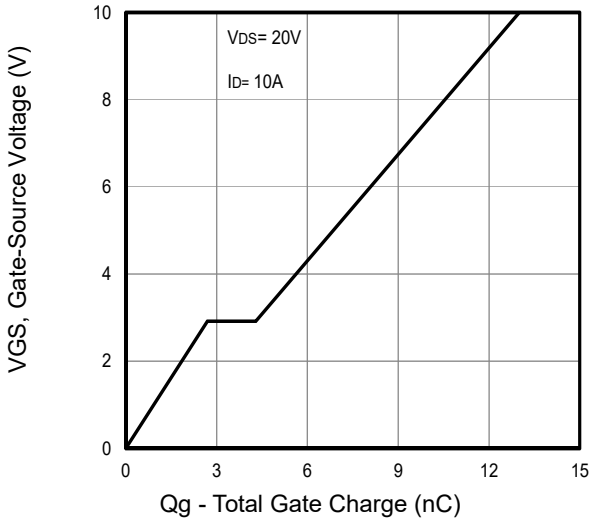


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

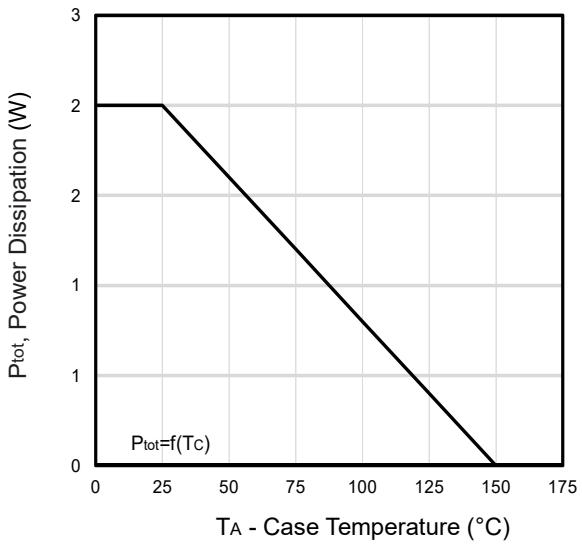


Fig11. Power Dissipation Vs. Case Temperature

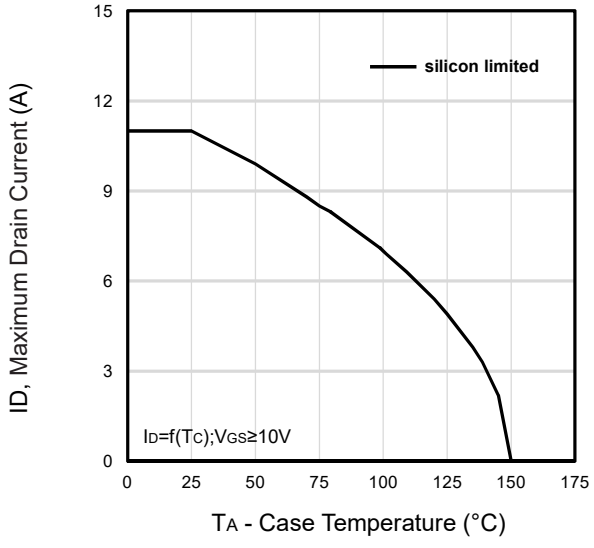


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

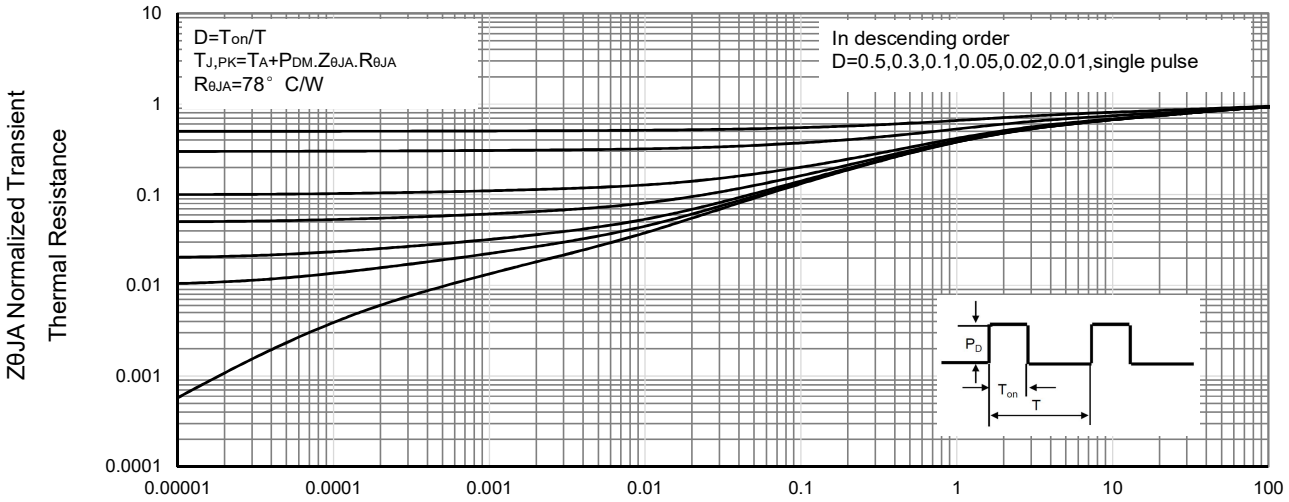


Fig13 . Normalized Maximum Transient Thermal Impedance

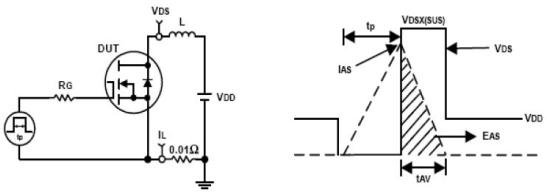


Fig14. Unclamped Inductive Test Circuit and waveforms

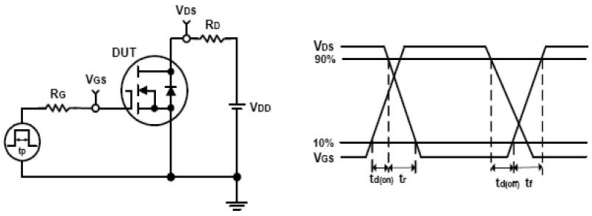
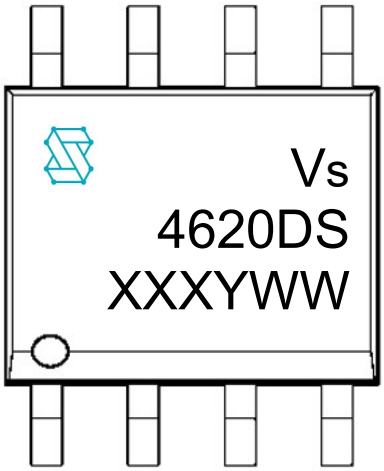


Fig15. Switching Time Test Circuit and waveforms

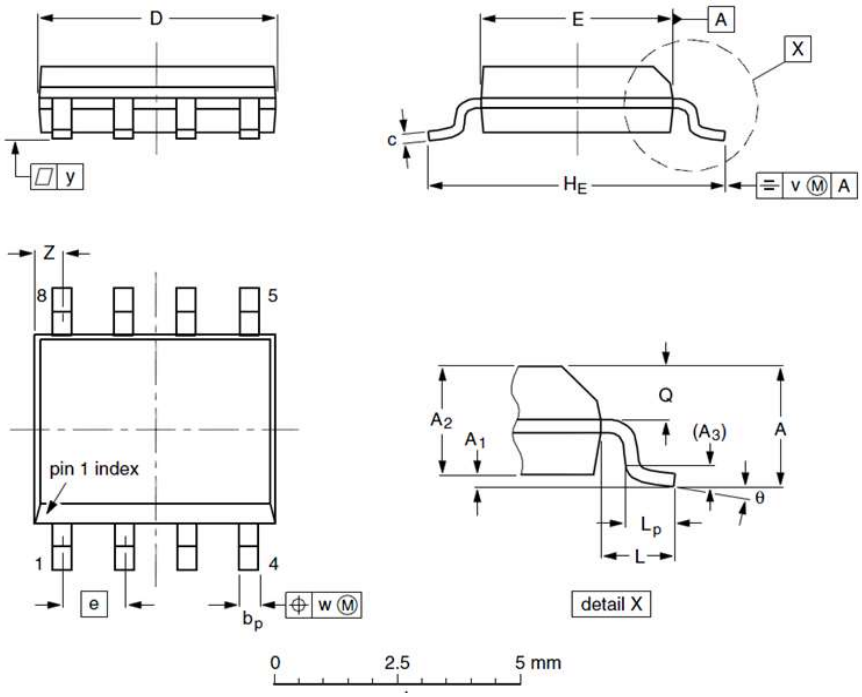
Marking Information



1st line: Vergiga Code（Vs），Vergiga Logo
2nd line: Part Number（4620DS）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

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