

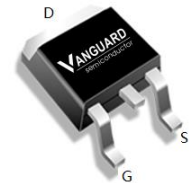
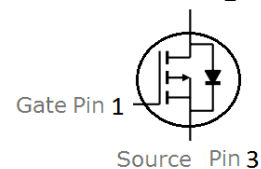
Features

- P-Channel, -5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=-4.5V$
- Fast Switching
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VS4504AD	TO-252	4504AD	2500PCS/Reel

V_{DS}	-40	V
$R_{DS(on),TYP@ V_{GS}=-10V}$	7	mΩ
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	10	mΩ
I_D	-90	A

TO-252

Drain Pin 2


Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
V _{(BR)DSS}	Drain-Source breakdown voltage		-40	V
V _{GS}	Gate-Source voltage		±20	V
I _S	Diode continuous forward current	T _C =25°C	-90	A
I _D	Continuous drain current @V _{GS} =-10V	T _C =25°C	-90	A
		T _C =100°C	-64	A
I _{DSM}	Continuous drain current @V _{GS} =-10V	T _A =25°C	10	A
		T _A =70°C	8	A
I _{DM}	Pulse drain current tested ①	T _C =25°C	-360	A
EAS	Avalanche energy, single pulsed ②		163	mJ
P _D	Maximum power dissipation	T _C =25°C	100	W
P _{DSM}	Maximum power dissipation ③	T _A =25°C	1.3	W
T _{STG} , T _J	Storage and Junction Temperature Range		-55 to 175	°C
Thermal Characteristics				
R _{θJC}	Thermal Resistance, Junction-to-Case		1.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient		100	°C/W



Typical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V,V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-40V,V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =-250μA	-1.3	-1.6	-2.4	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-20A	--	7	9	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-15A	--	10	13	mΩ
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-20V,V _{GS} =0V, f=1MHz	4600	5120	5600	pF
C _{oss}	Output Capacitance		400	490	600	pF
C _{rss}	Reverse Transfer Capacitance		300	415	510	pF
R _g	Gate Resistance	f=1MHz	--	7.7	--	Ω
Q _g (10V)	Total Gate Charge	V _{DS} =-20V,I _D =-20A, V _{GS} =-10V	--	85	--	nC
Q _g (4.5V)	Total Gate Charge		--	49	--	nC
Q _{gs}	Gate-Source Charge		--	17	--	nC
Q _{gd}	Gate-Drain Charge		--	20	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-20V, I _D =-20A, R _G =3.0Ω, V _{GS} =-10V	--	19.5	--	ns
t _r	Turn-on Rise Time		--	22	--	ns
t _{d(off)}	Turn-Off Delay Time		--	85.5	--	ns
t _f	Turn-Off Fall Time		--	39	--	ns
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-20A,V _{GS} =0V	--	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C,I _{SD} =-20A, V _{GS} =0V	--	29	--	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=-500A/us	--	167	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

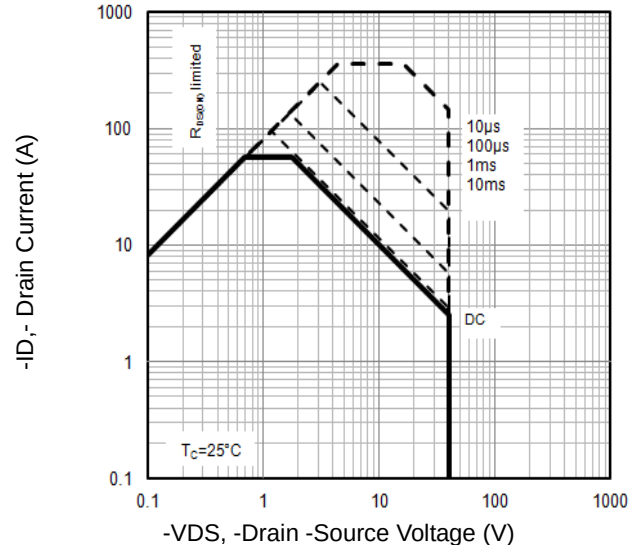
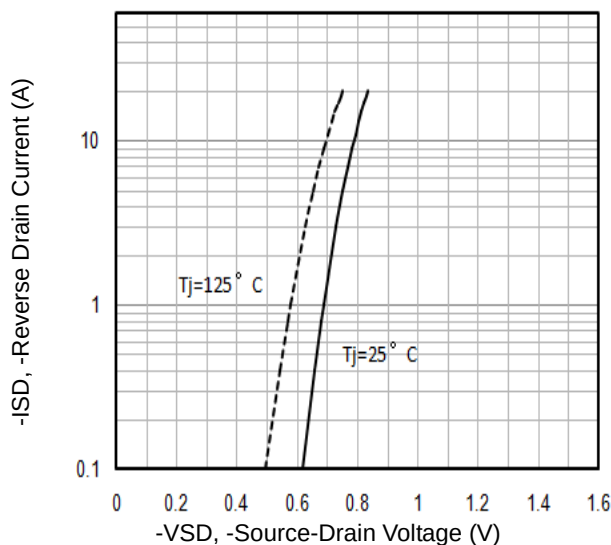
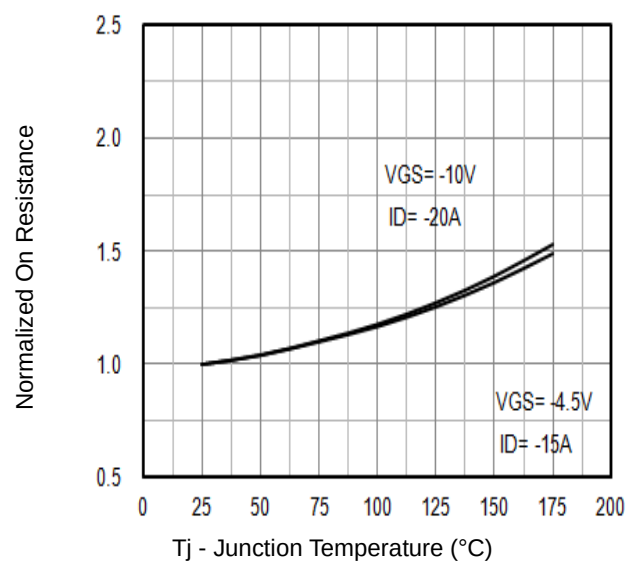
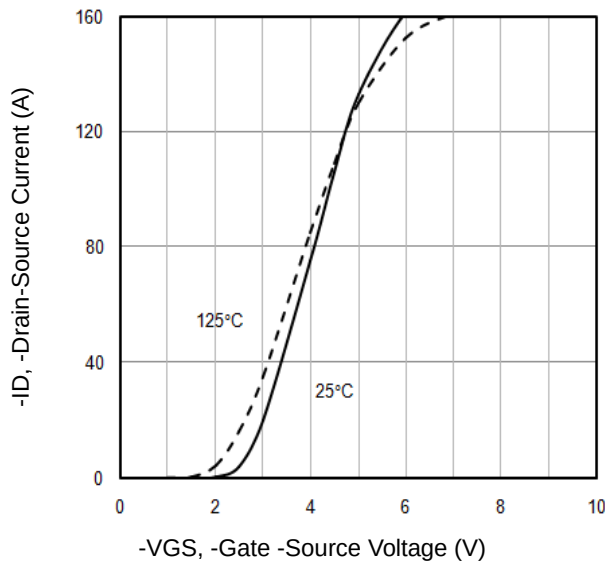
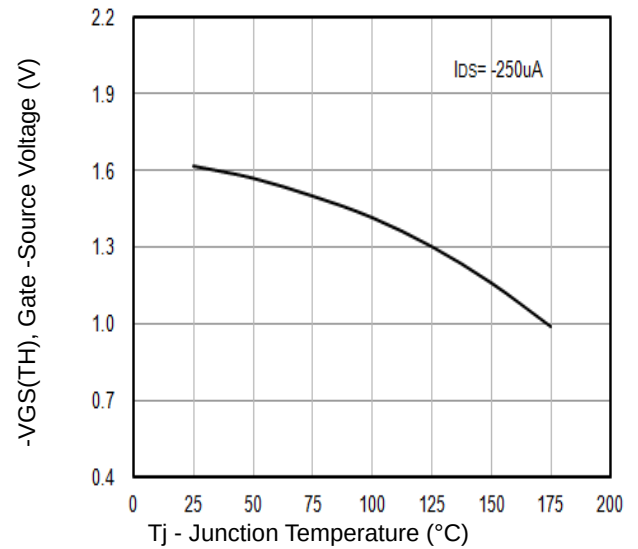
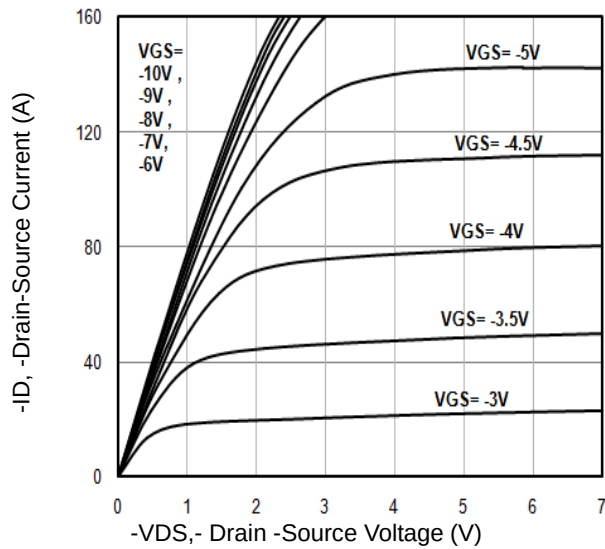
② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -20A, V_{GS} = -10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 300μs; duty cycles ≤ 2%.



Typical Characteristics



Typical Characteristics

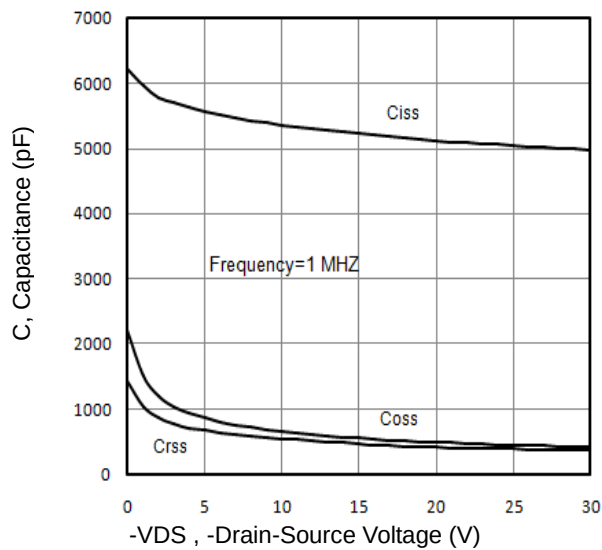


Fig7. Typical Capacitance Vs.Drain-Source Voltage

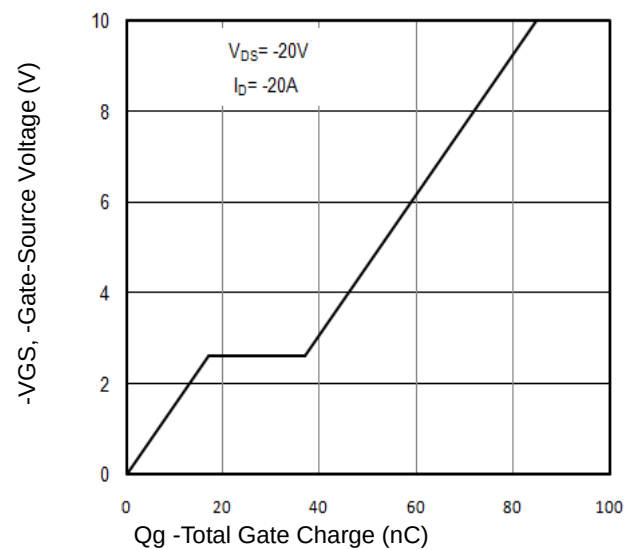


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

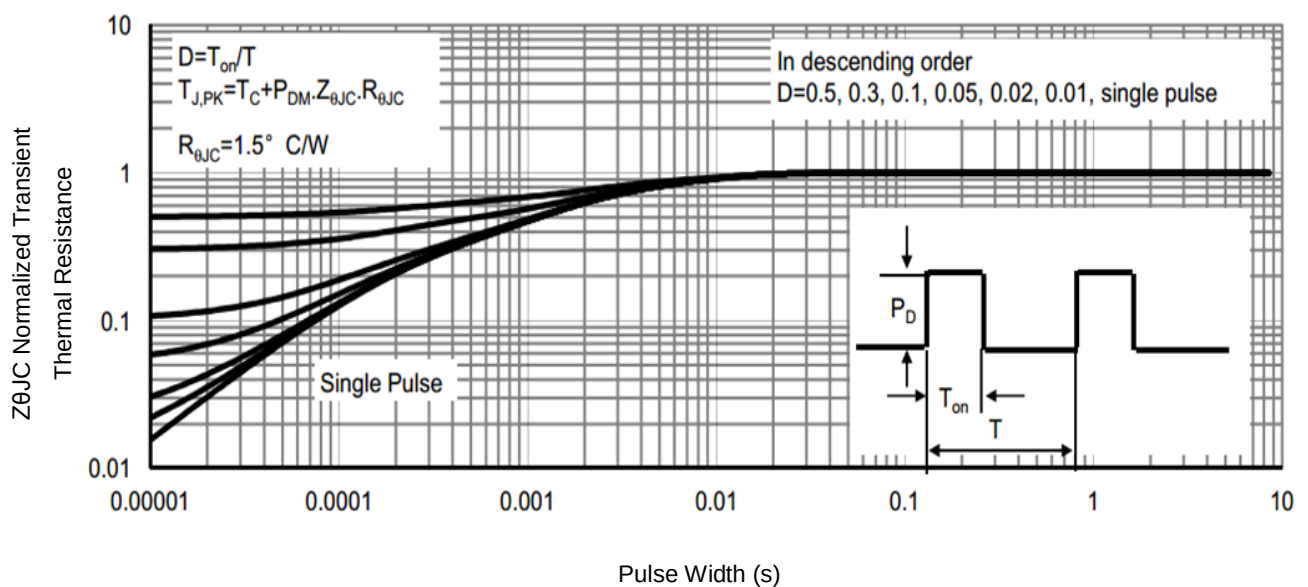


Fig9. Normalized Maximum Transient Thermal Impedance

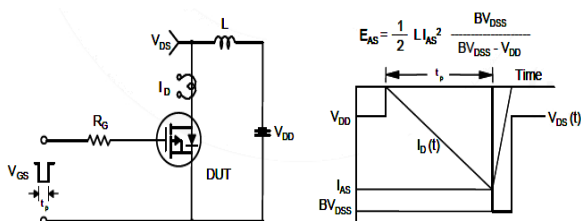


Fig10. Unclamped Inductive Test Circuit and Waveforms

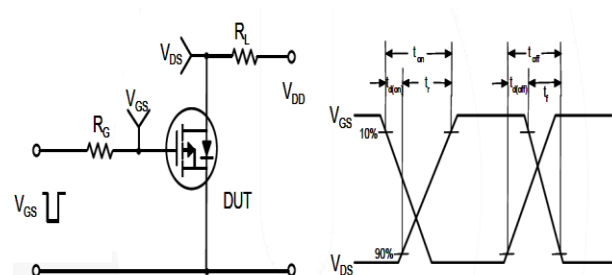
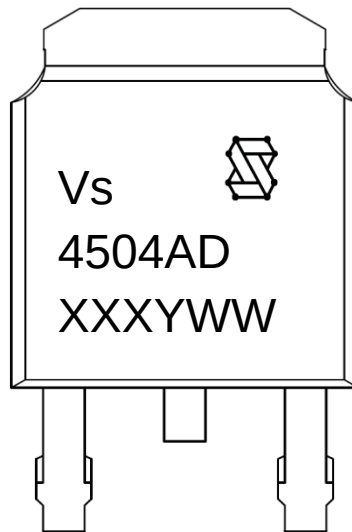


Fig11. Switching Time Test Circuit and waveforms



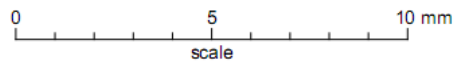
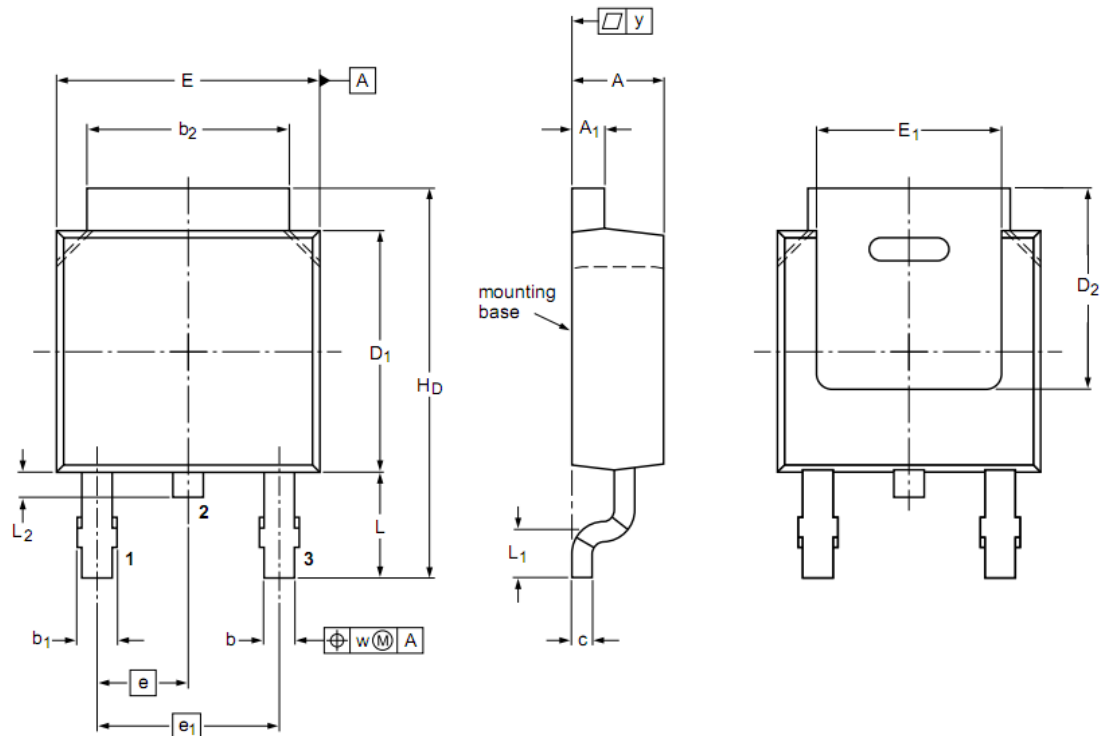
Marking Information



- 1st line: Vanguard Code (Vs), Vanguard Logo
2nd line: Part Number (4504AD)
3rd line: Date code (XXXYWW)
XXX: Wafer Lot Number
Y: Year Code, e.g. E means 2017
WW: Week Code



TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A ₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b ₁	0.77	0.85	1.14
b ₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D ₁	5.98	6.10	6.223
D ₂	5.21	--	--
E	6.40	6.60	6.731
E ₁	4.40	--	--
e	2.286 BSC		
e ₁	--	4.57	--
H _b	9.40	10.00	10.40
L	2.743 REF		
L ₁	1.40	1.52	1.77
L ₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

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