

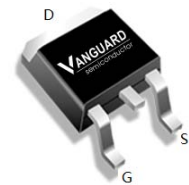
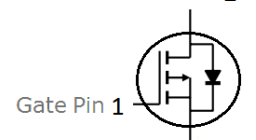
Features

- P-Channel, -5V Logic Level Control
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=-4.5V$
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VS3506AD	TO-252	3506AD	2500PCS/Reel

V_{DS}	-30	V
$R_{DS(on),TYP@ V_{GS}=-10V}$	6.5	mΩ
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	10	mΩ
I_D	-80	A

TO-252

Drain Pin 2

Source Pin 3

Maximum ratings, at $T_A=25^{\circ}C$, unless otherwise specified

Symbol	Parameter		Rating	Unit
V _{(BR)DSS}	Drain-Source breakdown voltage		-30	V
V _{GS}	Gate-Source voltage		±20	V
I _S	Diode continuous forward current	T _C =25°C	-80	A
I _D	Continuous drain current @V _{GS} =-10V	T _C =25°C	-80	A
		T _C =100°C	-55	A
I _{DM}	Pulse drain current tested ①	T _C =25°C	-320	A
I _{DSM}	Continuous drain current @V _{GS} =-10V	T _A =25°C	-10	A
		T _A =70°C	-8	A
EAS	Avalanche energy, single pulsed ②		36	mJ
P _D	Maximum power dissipation	T _C =25°C	75	W
P _{DSM}	Maximum power dissipation ③	T _A =25°C	1.25	W
MSL			Level 3	
T _{STG} T _J	Storage and Junction Temperature Range		-55 to 150	°C
Thermal Characteristics				
R _{θJC}	Thermal Resistance-Junction to Case		2.0	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient		100	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V,V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-30V,V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =-250μA	-1.0	--	-2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-20A	--	6.5	8	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-16A	--	10	12	mΩ
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-15V,V _{GS} =0V, f=1MHz	--	4750	--	pF
C _{oss}	Output Capacitance		--	545	--	pF
C _{rss}	Reverse Transfer Capacitance		--	490	--	pF
R _g	Gate Resistance	f=1MHz		3.4		Ω
Q _g	Total Gate Charge	V _{DS} =-15V,I _D =-20A, V _{GS} =-10V	--	89	--	nC
Q _{gs}	Gate-Source Charge		--	14	--	nC
Q _{gd}	Gate-Drain Charge		--	19	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, I _D =-20A, R _G =3.0Ω, V _{GS} =-10V	--	182	--	nS
t _r	Turn-on Rise Time		--	262	--	nS
t _{d(off)}	Turn-Off Delay Time		--	1.3	--	uS
t _f	Turn-Off Fall Time		--	9.8	--	uS
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-20A,V _{GS} =0V	--	-0.86	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25 °C,I _{sd} =-20A, V _{GS} =0V	--	34	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=-300A/μs		79		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -10A, V_{GS} = -10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycles ≤ 2%.

Typical Characteristics

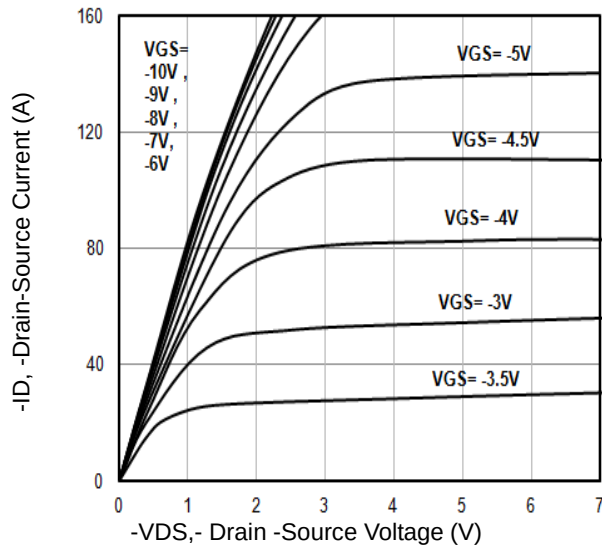


Fig1. Typical Output Characteristics

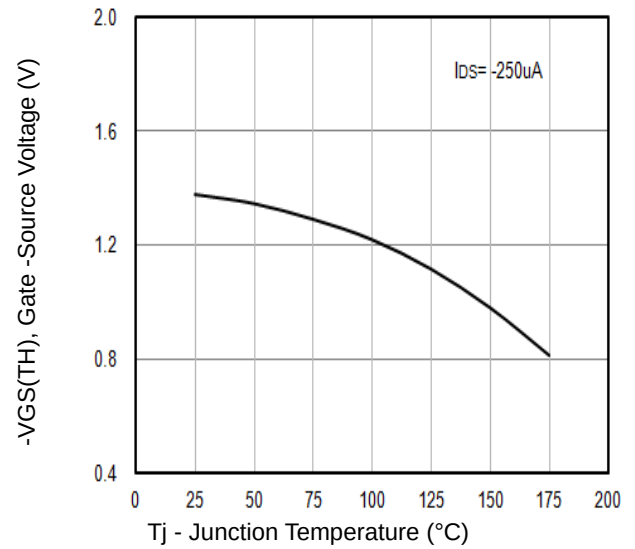


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

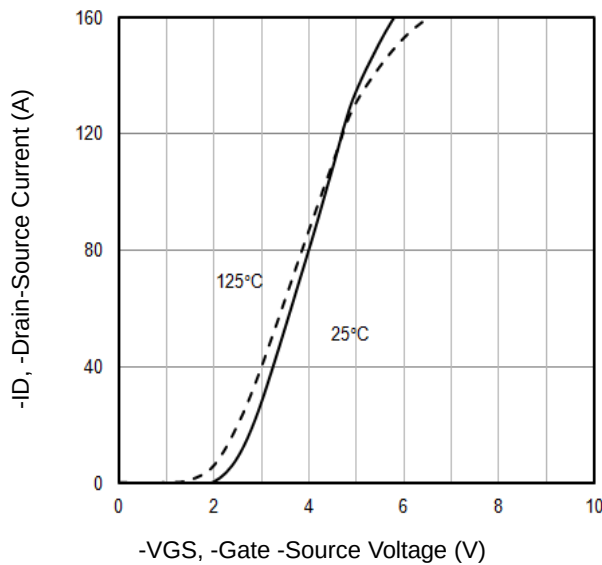


Fig3. Typical Transfer Characteristics

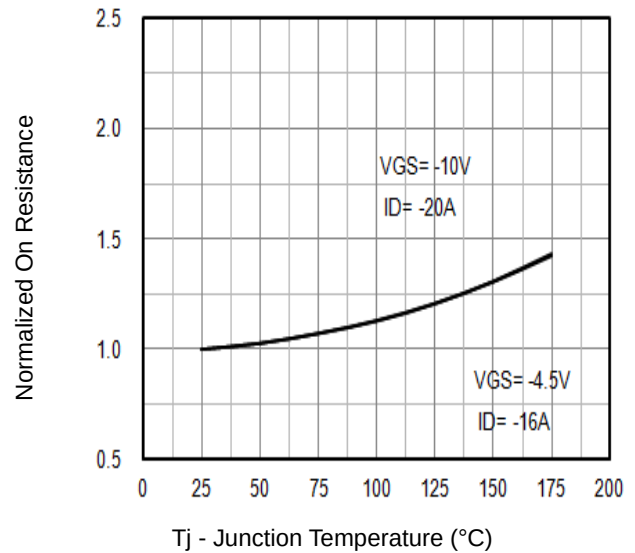


Fig4. Normalized On-Resistance Vs. T_j

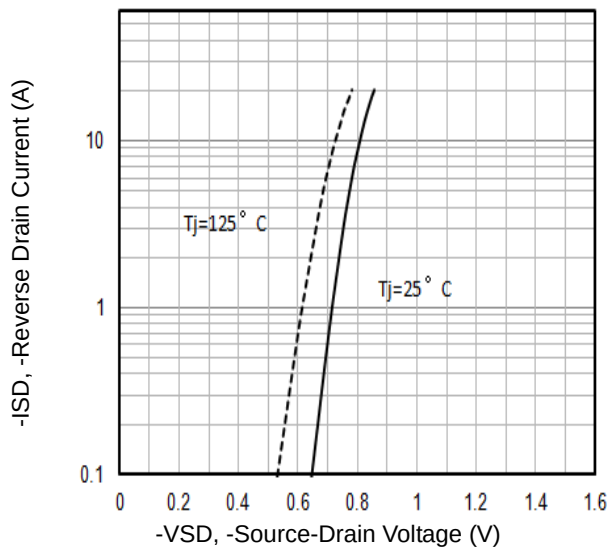


Fig5. Typical Source-Drain Diode Forward Voltage

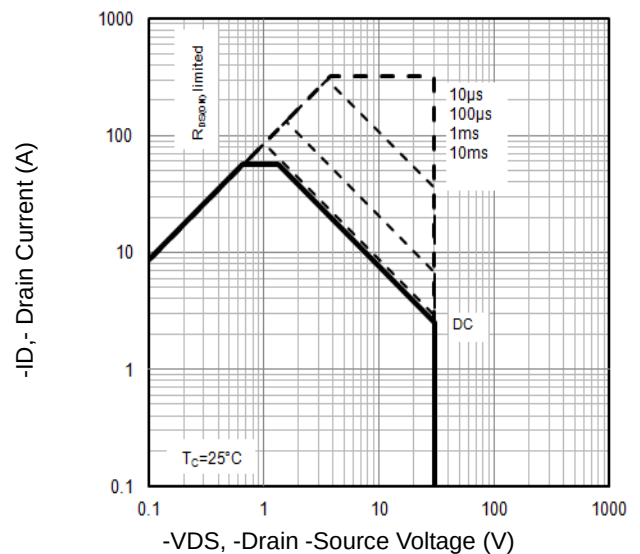


Fig6. Maximum Safe Operating Area

Typical Characteristics

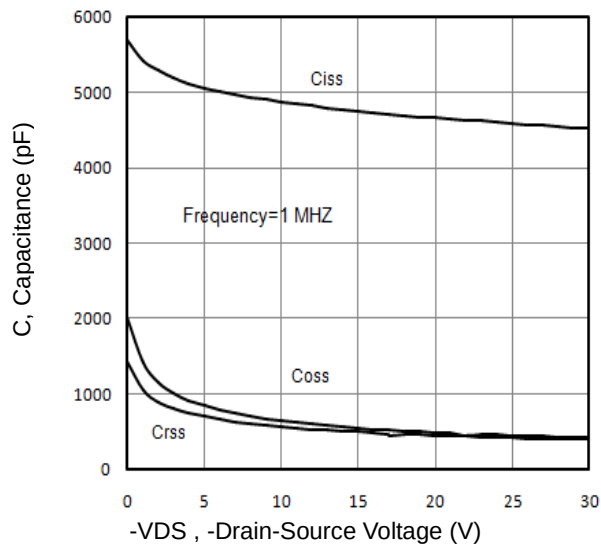


Fig7. Typical Capacitance Vs. Drain-Source Voltage

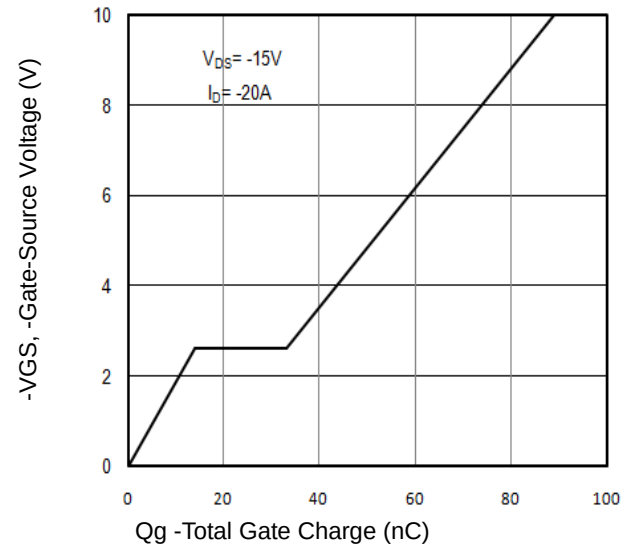


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

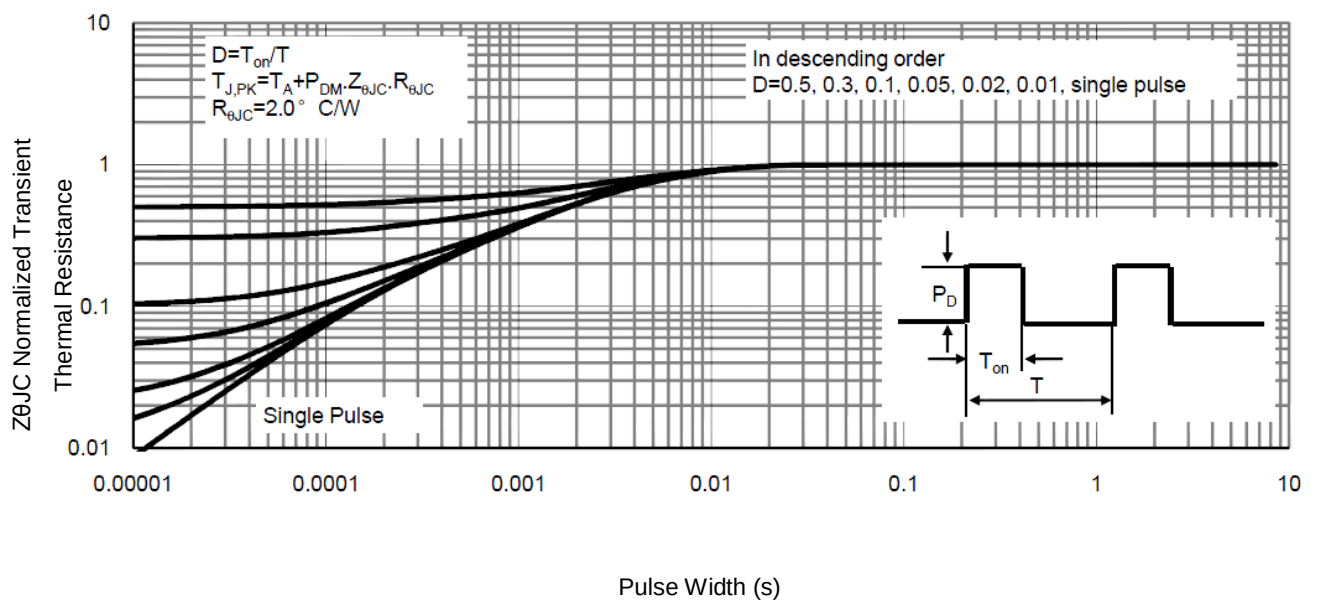


Fig9. Normalized Maximum Transient Thermal Impedance

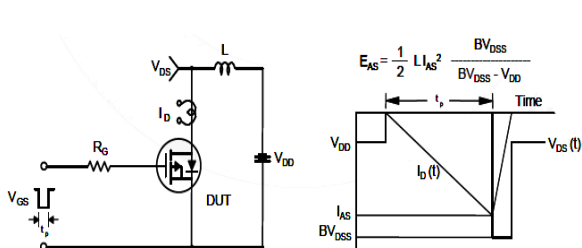


Fig10. Unclamped Inductive Test Circuit and Waveforms

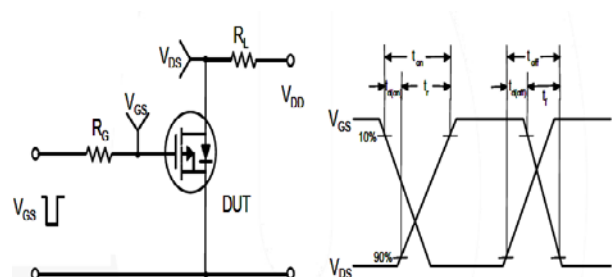
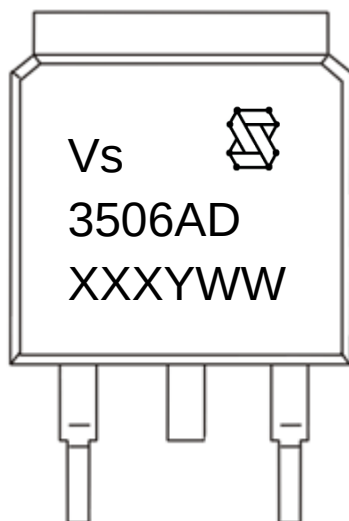


Fig11. Switching Time Test Circuit and waveforms

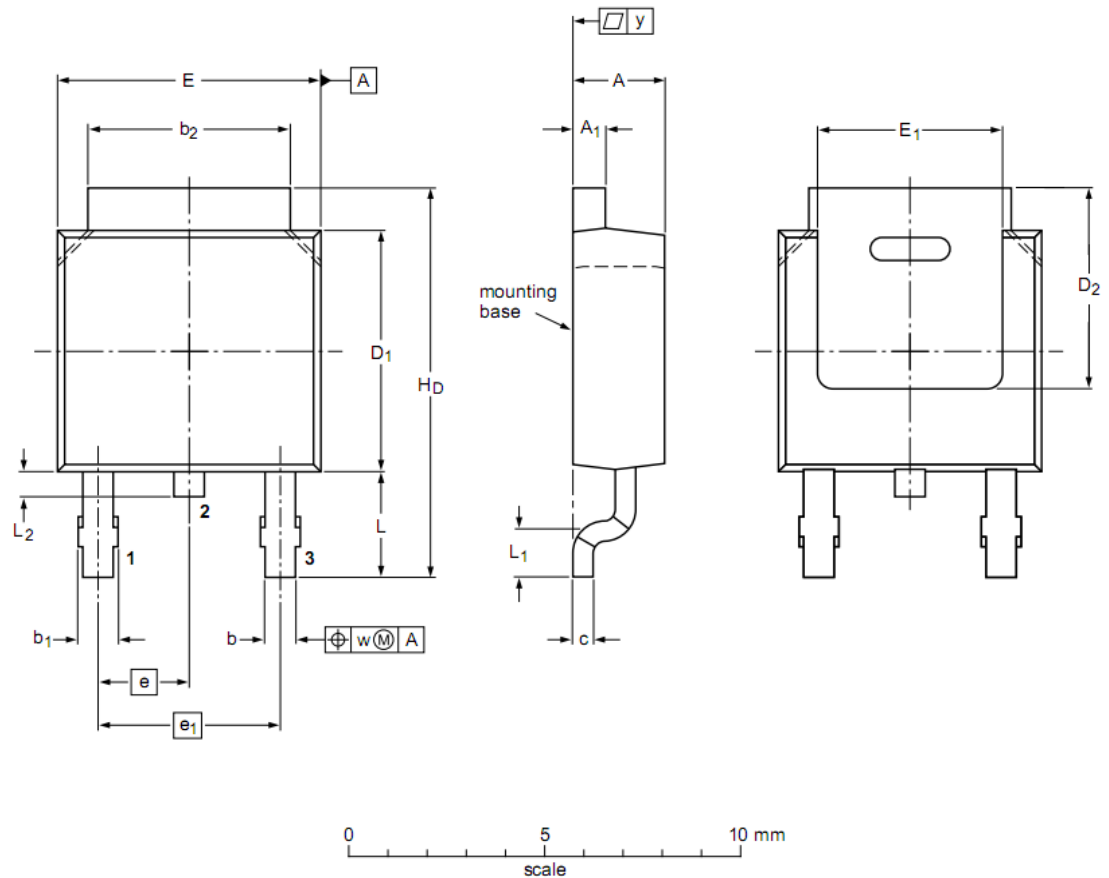


Marking Information



- 1st line: Company Code (Vs), Company Logo
2nd line: Part Number (3506AD)
3rd line: Date code (XXXYWW)
XXX: Wafer Lot Number
Y: Year Code, e.g. E means 2017
WW: Week Code

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b₁	0.77	0.85	1.14
b₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D₁	5.98	6.10	6.223
D₂	5.21	--	--
E	6.40	6.60	6.731
E₁	4.40	--	--
e	2.286 BSC		
e₁	--	4.57	--
H_D	9.40	10.00	10.40
L	2.743 REF		
L₁	1.40	1.52	1.77
L₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

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