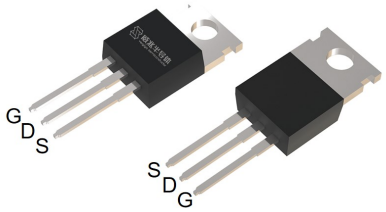
Features

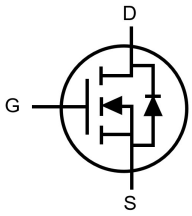
- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested, Rg 100% Tested

V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	3.6	mΩ
$I_{D(Wire\ bond\ limited)}$	130	A

TO-220AB



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VS1602GTH	TO-220AB	1602GTH	50pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C = 25°C	130	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	130	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	120	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	675	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	16	A
		T_A=70°C	12	A
EAS	Maximum Avalanche energy, single pulsed ②		484	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	250	W
P_{DSM}	Maximum power dissipation ④	T_A=25°C	2.1	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.5	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=40A	--	3.6	4.5	mΩ
		(Tj=100℃)⑦	--	4.7	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=100KHz	--	5195	--	pF
Coss	Output Capacitance ⑦		--	875	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	30	--	pF
Rg	Gate Resistance	f=1MHz	--	1.8	--	Ω
Qg	Total Gate Charge ⑦	V_{DS}=50V,I_D=40A, V_{GS}=10V	--	91	--	nC
Qgs	Gate-Source Charge ⑦		--	25	--	nC
Qgd	Gate-Drain Charge ⑦		--	25	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=50V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	21	--	ns
Tr	Turn-on Rise Time		--	69	--	ns
Td(off)	Turn-Off Delay Time		--	57	--	ns
Tf	Turn-Off Fall Time		--	70	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑦	Isd=40A, V_{GS}=0V di/dt=100A/μs	--	59	--	ns
Qrr	Reverse Recovery Charge ⑦		--	71	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 44A, V_{GS} =10V；100% FT tested at L = 0.5mH, I_{AS} = 22A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

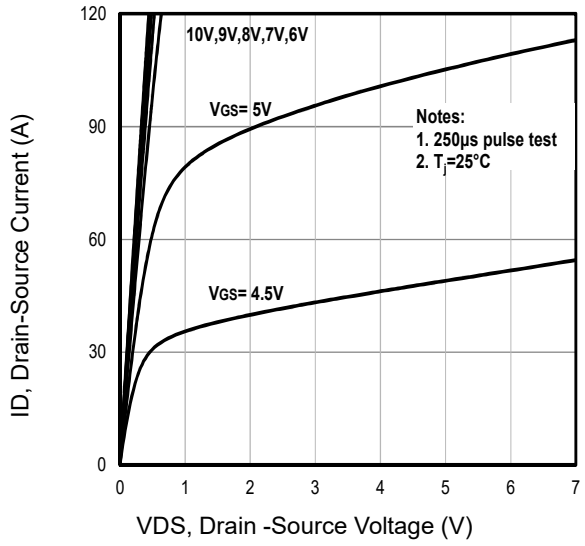


Fig1. Typical Output Characteristics

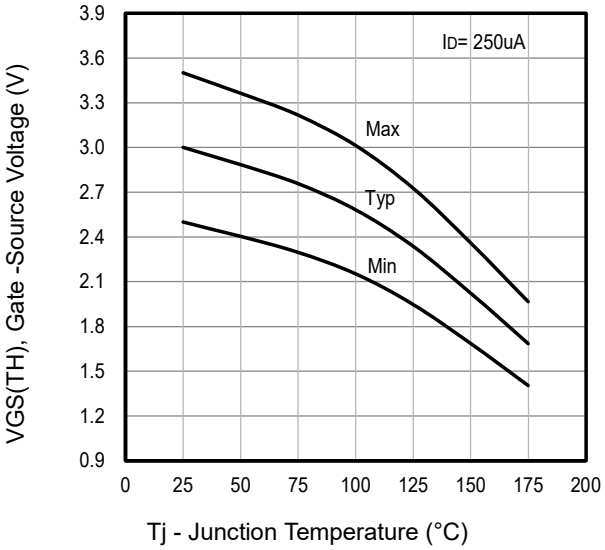


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

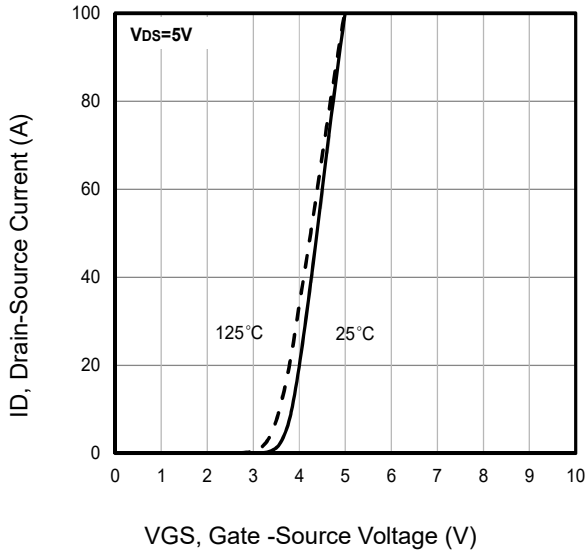


Fig3. Typical Transfer Characteristics

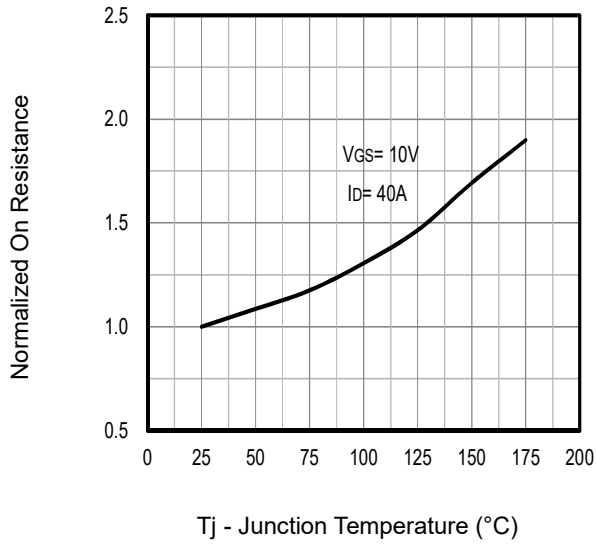


Fig4. Typical Normalized On-Resistance Vs. Tj

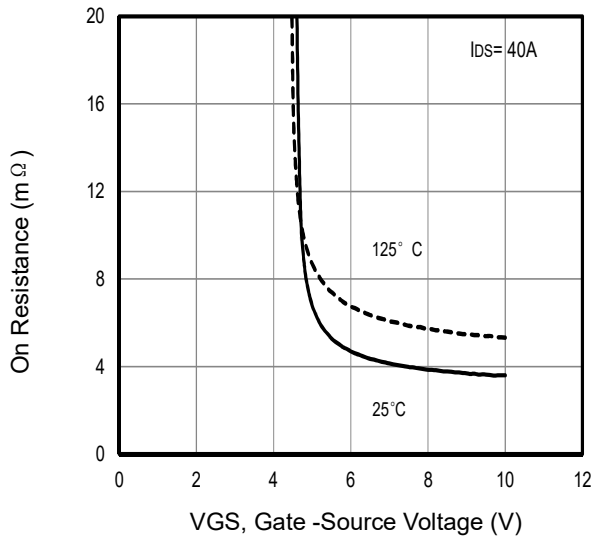


Fig5. Typical On Resistance Vs Gate -Source Voltage

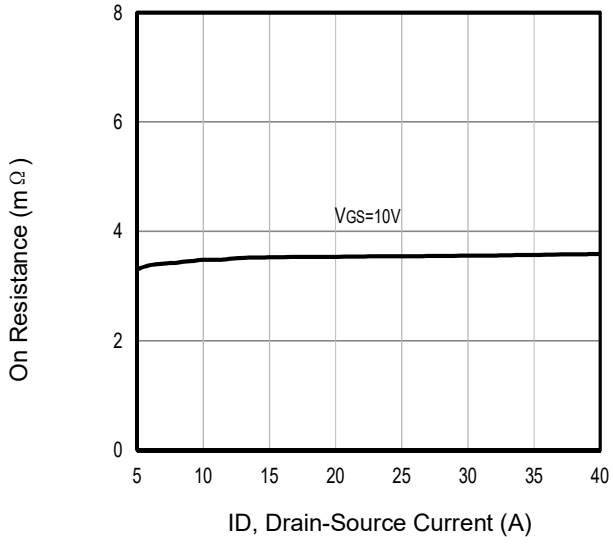


Fig6. Typical On Resistance Vs Drain Current and Gate

Typical Characteristics

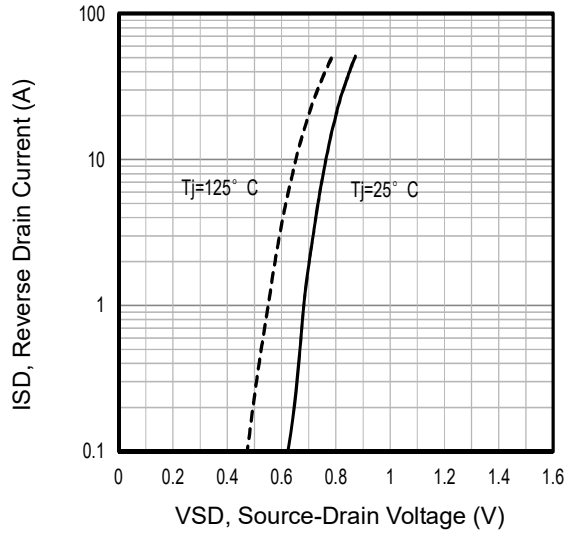


Fig7. Typical Source-Drain Diode Forward Voltage

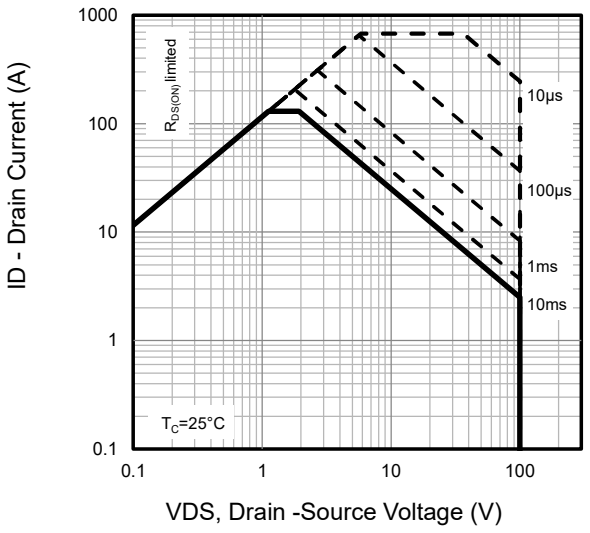


Fig8. Maximum Safe Operating Area

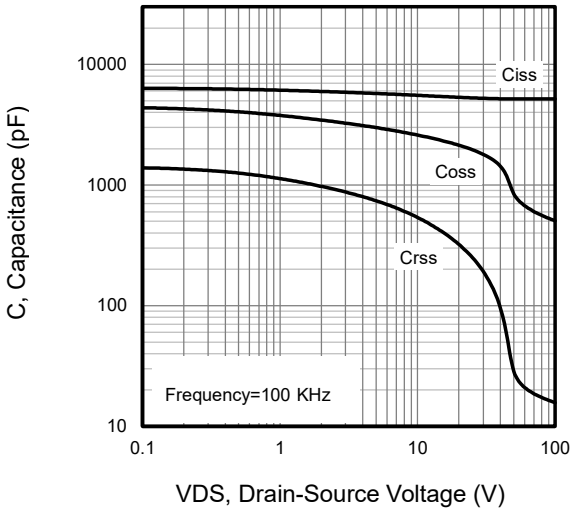


Fig9. Typical Capacitance Vs. Drain-Source Voltage

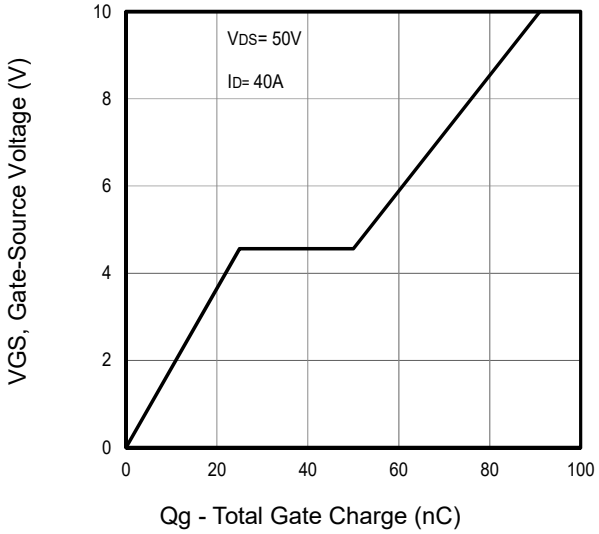


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

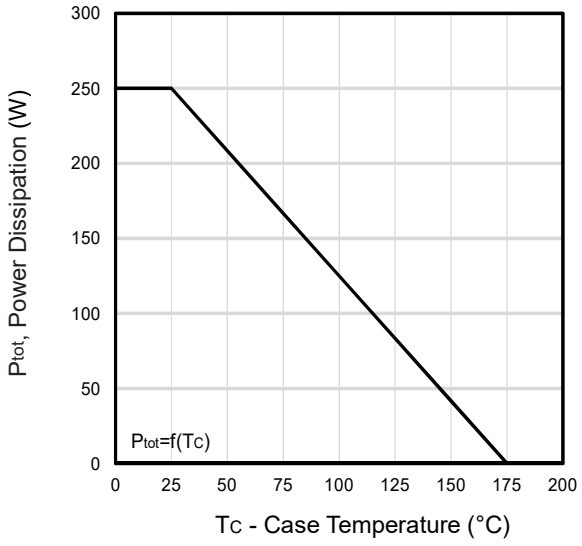


Fig11. Power Dissipation Vs. Case Temperature

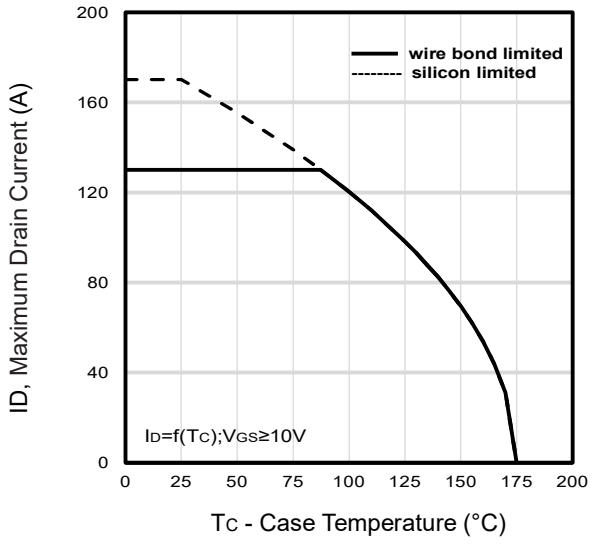


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

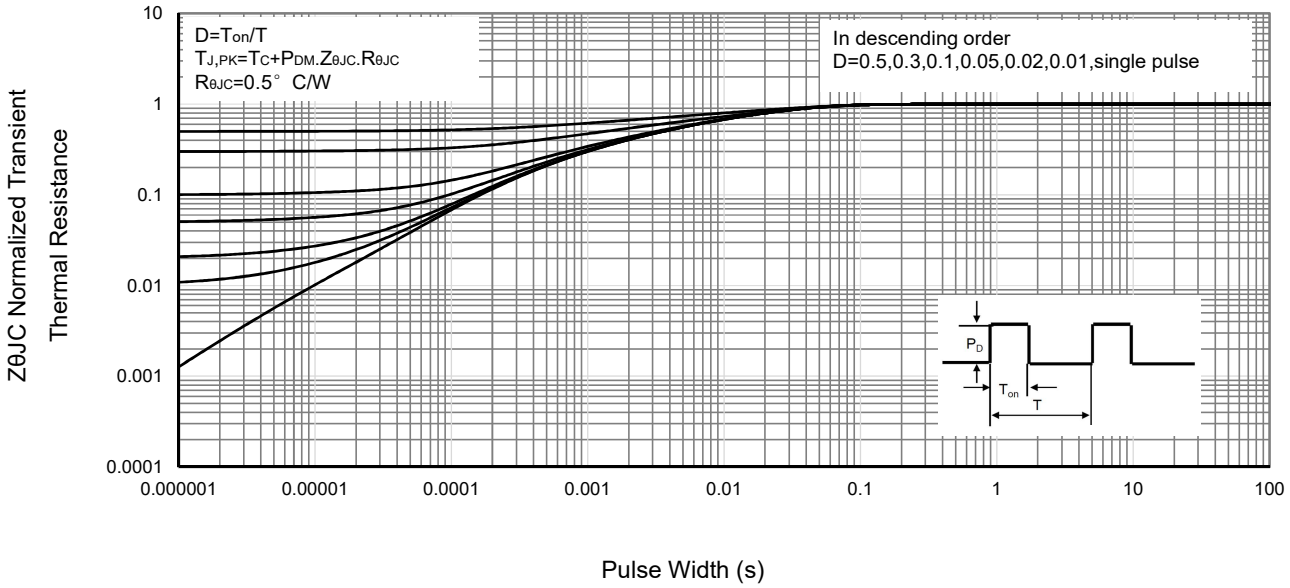


Fig13 . Normalized Maximum Transient Thermal Impedance

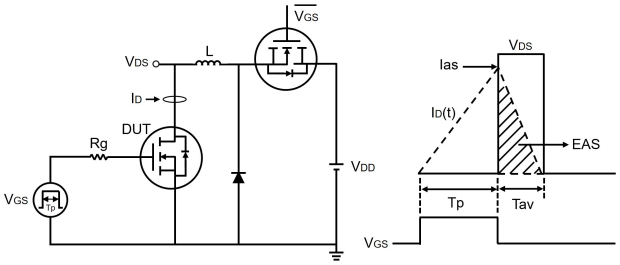


Fig14. Unclamped Inductive Test Circuit and waveforms

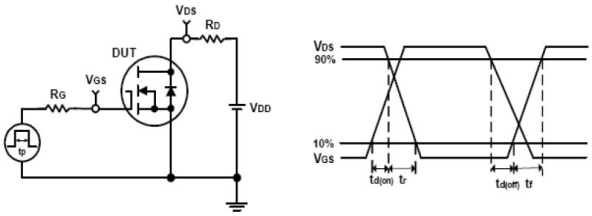
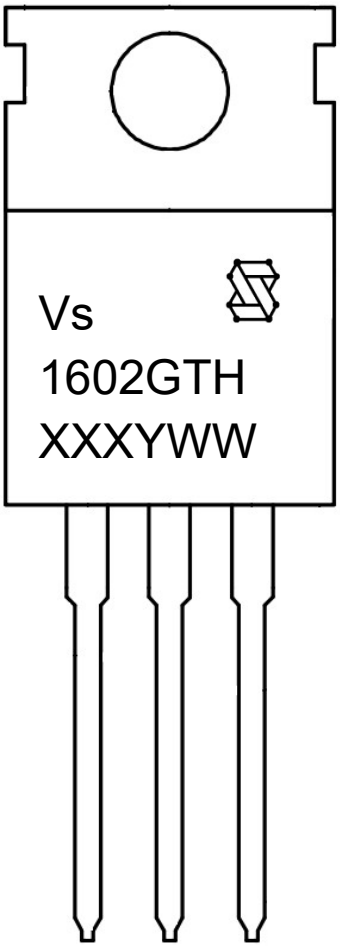


Fig15. Switching Time Test Circuit and waveforms

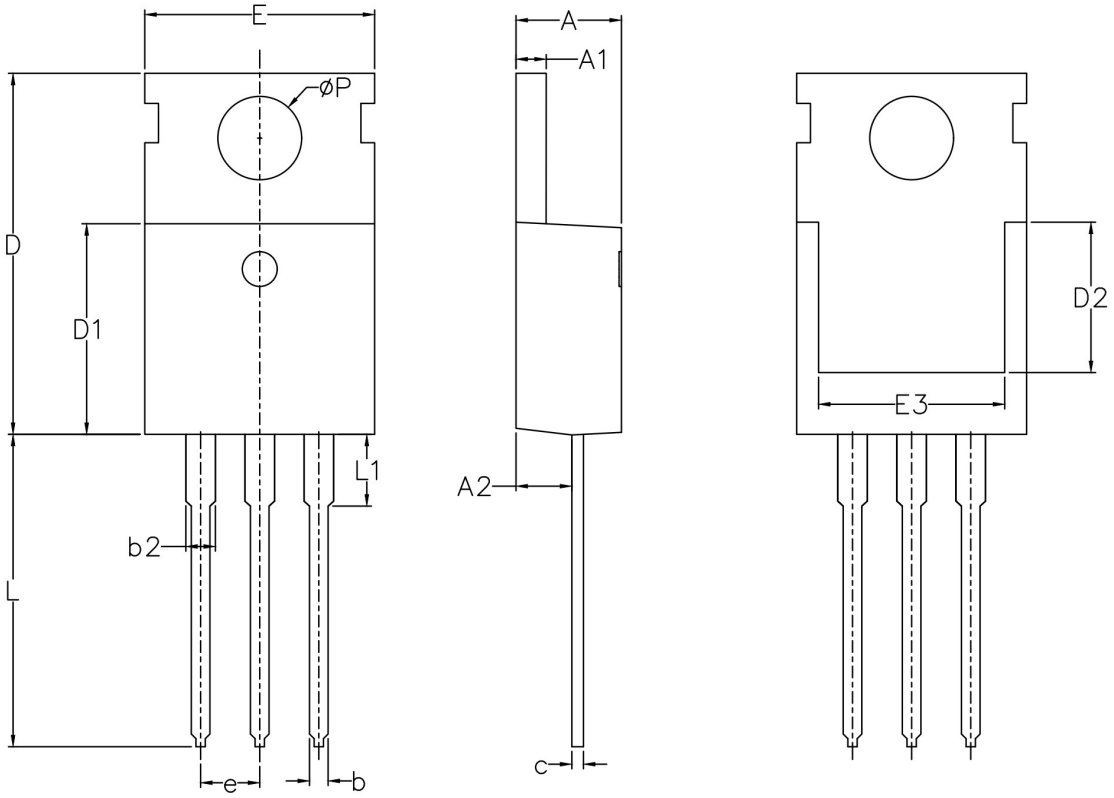
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（1602GTH）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code, refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.35	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.27	1.47
c	0.45	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	--	--
E	9.70	10.00	10.30
E3	7.00	--	--
e	2.54 BSC		
L	12.75	13.50	13.85
L1	--	3.10	3.40
ΦP	3.40	3.60	3.80

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.
3. Thermal pad contour optional within dimensions E,H1,D2&E1.
4. Dimension E2&H1 define A zone where stamping and singulation irregularities are allowed.