

ADD-A-PAK Generation VII Power Modules Schottky Rectifier, 200 A



PRODUCT SUMMARY			
I _{F(AV)}	200 A		
V_{R}	100 V		
Package	ADD-A-PAK		
Circuit	Two diodes doubler circuit		

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- · High surge capability
- · Easy mounting on heatsink

ELECTRICAL DESCRIPTION

The VS-VSKDS403.. Schottky rectifier doubler module has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
I _{F(AV)}	Rectangular waveform	200	А		
V _{RRM}		100	V		
I _{FSM}	t _p = 5 μs sine	20 000	А		
V _F	100 A _{pk} , T _J = 125 °C	0.66	V		
T _J	Range	-55 to 175	°C		

VOLTAGE RATINGS					
PARAMETER	SYMBOL	VS-VSKDS403/100	UNITS		
Maximum DC reverse voltage	V_{R}	100	V		
Maximum working peak reverse voltage	V_{RWM}	100	V		



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	I _{F(AV)} 50 % duty cycle at T _C = 111 °C, rectangular waveform		200		
Maximum peak one cycle		5 μs sine or 3 μs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	20 000	Α
non-repetitive surge current	IFSM	10 ms sine or 6 ms rect. pulse		2300	
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 5.5 A, L = 1 mH		15	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical		А	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum famound up be an advan	V _{FM}	200 A	- T _J = 25 °C	0.99	V
		400 A		1.3	
Maximum forward voltage drop		200 A	T _J = 125 °C	0.83	
		400 A		1.09	
Mariana da la	I _{RM}	T _J = 25 °C	V _R = Rated V _R	6	mA
Maximum reverse leakage current		T _J = 125 °C		80	IIIA
Maximum junction capacitance	C _T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		55 000	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T _J , T _{Stg}		-55 to 175	°C
Maximum thermal resistance, junction to case per leg		R _{thJC}	DC operation	0.26	°C/W
Typical thermal resistance, case to heatsink per module		R _{thCS}		0.1	C/VV
Approximate weight				75	g
Approximate weight				2.7	OZ.
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the	4	Nm
	busbar		spread of the compound.	3	INIII
Case style			JEDEC®	TO-240AA co	ompatible

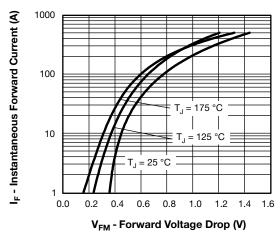


Fig. 1 - Maximum Forward Voltage Drop Characteristics

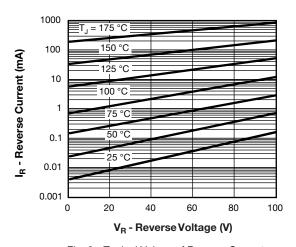


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

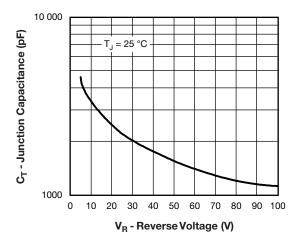


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

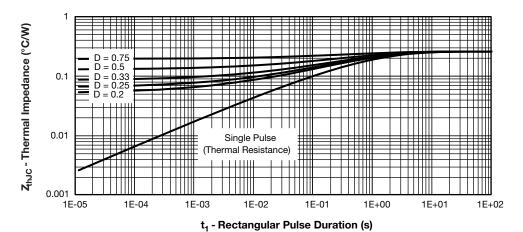


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

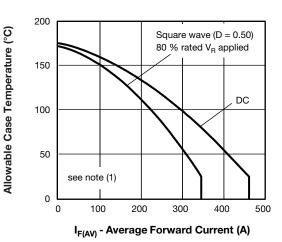


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

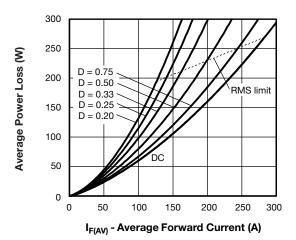


Fig. 6 - Forward Power Loss Characteristics

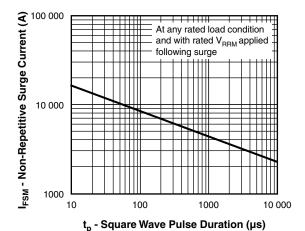


Fig. 7 - Maximum Non-Repetitive Surge Current

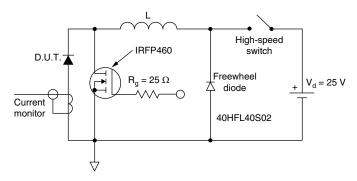


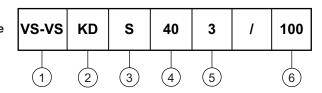
Fig. 8 - Unclamped Inductive Test Circuit

Note

 $^{(1)}$ Formula used: T_C = T_J - (Pd + Pd_{REV}) x R_{th,JC}; Pd = Forward power loss = I_{F(AV)} x V_{FM} at (I_{F(AV)}/D) (see fig. 6); Pd_{REV} = Inverse power loss = V_{R1} x I_R (1 - D); I_R at V_{R1} = 80 % rated V_R

ORDERING INFORMATION TABLE

Device code



VS-VS = Vishay Semiconductors product

2 - Circuit configuration:

KD = ADD-A-PAK - 2 diodes in series

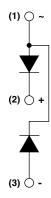
3 - S = Schottky diode

4 - Average rating (x 10)

5 - Product silicon identification

Voltage rating (100 = 100 V)

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS			
Dimensions	www.vishay.com/doc?95369		



ADD-A-PAK Generation VII - Diode

DIMENSIONS in millimeters (inches)





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