

VQ7254 SERIES

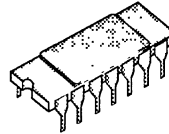


N- and P-Channel Enhancement-Mode MOS Transistor Arrays

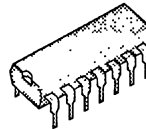
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$	I_D (A)	PACKAGE
VQ7254J	20/-20	3 Ω	2	Plastic
VQ7254P	20/-20	3 Ω	2	Side Braze

14-PIN DIP
SIDE BRAZE

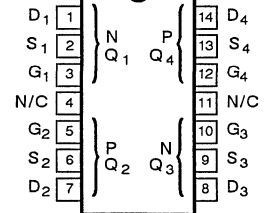


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ7254J		VQ7254P		UNITS
			N-Channel	P-Channel	N-Channel	P-Channel	
Drain-Source Voltage		V _{DS}	20	−20	20	−20	V
Gate-Source Voltage		V _{GS}	± 30	± 30	± 20	± 20	
Continuous Drain Current (T _A = 25°C)		I _D	2	−2	2	−2	A
Pulsed Drain Current ¹		I _{DM}	± 3	± 3	± 3	± 3	
Power Dissipation – Single	T _A = 25°C	P _D	1.75	1.75	1.75	1.75	W
	T _A = 80°C		1.05	1.05	1.05	1.05	
Operating Junction		T _J	−40 to 100				°C
Storage Temperature		T _{stg}	−40 to 150				
Lead Temperature (1/16" from case for 10 seconds)		T _L	300				
Thermal Coupling Factor – Single (K)–Q ₁ –Q ₄ or Q ₂ –Q ₃			60				%
Thermal Coupling Factor – Single (K)–Q ₁ –Q ₂ –Q ₃ –Q ₄ , Q ₁ –Q ₃ or Q ₂ –Q ₄			50				

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ7254J	VQ7254P	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	96.2	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Quad		62.5	62.5	

¹Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS ¹			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS ⁶	VQ7254			UNIT
			TYP ²	MIN	MAX	
STATIC ⁴						
Drain-Source On Voltage	V _{DS(ON)}	V _{GS} = 11.4 V, I _D = 1 A (Q ₁ + Q ₂) or (Q ₃ + Q ₄)	2.5	2	3	V
Drain-Source On-Resistance ³	r _{DS(ON)}		2.5	2	3	Ω

PARAMETER	SYMBOL	TEST CONDITIONS ⁶	N-Channel			P-Channel			UNIT
			TYP ²	MIN	MAX	TYP ²	MIN	MAX	
STATIC									
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 10 μA	-40	20		-55	-20		V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} I _D = 1 mA	1.5	0.8		-3.6	-0.8		
		T _J = 85°C	1.2	0.65		-3.3	-0.65		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	±1		±100	±1		±100	nA
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	0.1		500	-0.1		-500	μA
On-State Drain Current ³	I _{D(ON)}	V _{DS} = 10 V, V _{GS} = 10 V	1.8			-1.6			A
Forward Transconductance ³	g _{FS}	V _{DS} = 10 V, I _D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C _{iss}	V _{DS} = 12 V V _{GS} = 0 V f = 1 MHz	85		175	130		190	pF
Output Capacitance	C _{oss}		80		95	75		100	
Reverse Transfer Capacitance	C _{rss}		18		25	20		60	
SWITCHING ⁵									
Turn-On Time	t _{ON}	V _{DD} = 17 V, R _L = 15 Ω I _D = 1.1 A, V _{GEN} = 10 V R _G = 25 Ω	12		20	20		30	ns
Turn-Off Time	t _{OFF}		14		20	20		30	
DYNAMIC									
Continuous Source Current (Body Diode)	I _S	Modified MOSPOWER symbol showing the integral P-N junction rectifier   N-Channel P-Channel			2			-2	A
Source Current (Body Diode)	I _{SM}				3			-3	
Diode Forward Voltage	V _{SD}	V _{GS} = 0 V T _C = 25°C	I _S = 50 mA I _S = 1 A	0.6 1	0.75 1.2	-0.6 -1		-0.75 -1.2	V

- NOTES: 1. $T_A = 25^\circ\text{C}$ unless otherwise noted.
 2. For design aid only, not subject to production testing.
 3. Pulse test; $PW = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 4. $r_{DS(ON)}$ and $V_{DS(ON)}$ limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
 5. Switching time is essentially independent of operating temperature.
 6. Reverse polarity for p-channel devices.