Siliconix incorporated

VQ7254J

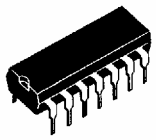
N- and P- Channel Enhancement-Mode MOS Transistor Array

T43-25

PRODUCT SUMMARY

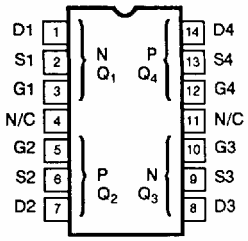
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$ (Ω)	I_D (A)
20/–20	3	2

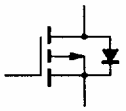
14-PIN PLASTIC



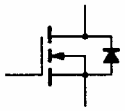
TOP VIEW

Dual-In-Line Package





P-Channel



N-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS N-CHANNEL	LIMITS P-CHANNEL	UNITS
Drain-Source Voltage		V_{DS}	20	–20	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current		I_D	2	–2	A
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation – Single	T_A = 25°C	P_D	1.75	1.75	W
	T_A = 80°C		1.05	1.05	
Operating Junction Temperature Range		T_J	–40 to 100		°C
Storage Temperature Range		T_{stg}	–40 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		
Thermal Coupling Factor – Single (K) – Q_1 – Q_4 or Q_2 – Q_3			60		%
Thermal Coupling Factor – Single (K) – Q_1 – Q_2 –Q_3 – Q_4, Q_1 – Q_3 or Q_2 – Q_4			50		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	K/W
Junction-to-Ambient – Quad		62.5	

[1]Pulse width limited by maximum junction temperature

6

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS[f]	TYP[b]	MIN	MAX	UNIT
STATIC[d]						
Drain-Source On Voltage	$V_{DS(ON)}$	V_{GS} = 11.4 V, I_D = 1 A	2.5	2	3	V
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	(Q_1 + Q_2) or (Q_3 + Q_4)	2.5	2	3	Ω

SPECIFICATIONS[a]			LIMITS						
			N-CHANNEL			P-CHANNEL			
PARAMETER	SYMBOL	TEST CONDITIONS[f]	TYP[b]	MIN	MAX	TYP[b]	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	40	20		−55	−20		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8		−3.6	−0.8		
		T_J = 85°C	1.2	0.65		−3.3	−0.65		
Gate-Body Leakage	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V	±1		±100	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.1		500	−0.1		−500	µA
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8			−1.6			A
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V f = 1 MHz	85		175	130		190	pF
Output Capacitance	C_{oss}		80		95	75		100	
Reverse Transfer Capacitance	C_{rss}		18		25	20		60	
SWITCHING[e]									
Turn-On Time	t_{ON}	V_{DD} = 17 V, R_L = 15 Ω I_D = 1.1 A, V_{GEN} = 10 V	12		20	20		30	ns
Turn-Off Time	t_{OFF}	R_G = 25 Ω	14		20	20		30	

NOTES
a T_A = 25°C unless otherwise noted
b. For design aid only, not subject to production testing.
c Pulse test, PW = ≤ 300 µS, duty cycle ≤ 2%.
d. $r_{DS(ON)}$ and $V_{DS(ON)}$ limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
e Switching time is essentially independent of operating temperature.
f Reverse polarity for p-channel devices.