VQ2001 SERIES

Siliconix incorporated

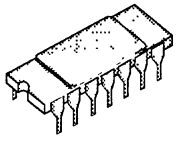
P-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

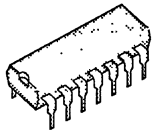
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2001J	-30	2	-0.6	Plastic
VQ2001P	-30	2	-0.6	Side Braze

Performance Curves: **VPMH03** (See Section 7)

14-PIN DIP
SIDE BRAZE

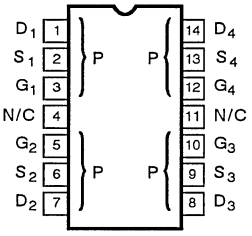


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2001J	VQ2001P	UNITS
Drain-Source Voltage		V_{DS}	-30	-30	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.6	-0.6	A
	T_A = 100°C		-0.12	-0.12	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2001J	VQ2001P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
			VQ2001			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±16 V, T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	-0.0001		-10	µA
		V_{DS} = -30 V, V_{GS} = 0 V, T_J = 125°C	-0.3		-500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-1.6	-1.5		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2	Ω
		V_{GS} = -12 V, I_D = -1 A, T_J = 125°C	3.1		3.6	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290	200		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.05 A	800			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	pF
Reverse Transfer Capacitance	C_{rss}		20		60	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -15 V, R_L = 23 Ω, I_D = -0.6 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	18		30	ns
Turn-Off Time	t_{OFF}		13		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.