MITEL
SEMICONDUCTOR

VP510

Bi Directional Colour Space Converter

Advance Information

DS3507 - 1.6 September 1996

FEATURES

- User definable colour space conversion
- Sampling rates up to 27 MHz
- On chip decimating or interpolating FIR filters
- Conversion from 24 bit inputs to 16 bit outputs or vice versa
- RAM based look up tables for gamma correction
- 100 pin Quad Flat Pack

ASSOCIATED PRODUCTS

- VP2611 Integrated H.261 Video Encoder
- VP2615 H.261 Video Decoder
- VP520S Two dimensional Video Filter

ORDERING INFORMATION

VP510 CG GPFR

(Commercial Temperature - PLCC Package).

DESCRIPTION

The VP510 converts three channels of RGB data into two channels of decimated chrominance and luminance data. Alternatively it converts two channels of luminance and chrominance data into three channels of interpolated RGB data. Each channel has its own RAM based look up table, which can be loaded from a host system and then used for gamma correction and/or ranging.

The direction of the data flow is controlled by a bit in a Control Register, and causes previous outputs to become inputs and vice versa. The filters change from the decimating to the interpolating mode, and correspondingly follow or precede the colour space conversion.

The 3 x 3 conversion matrix is provided with user definable 12 bit coefficients which have a range from -4.0 to +4.0. The luminance channel is provided with a 23 tap low pass filter which can decimate or interpolate by two. The chrominance channels each have two 11 tap filters in series which can decimate or interpolate by four. This arrangement allows the device to accept or produce RGB data which has been 2x oversampled, thus avoiding the need for external analog anti-aliasing filters. If necessary the device will still accept or produce video data which has not been oversampled.

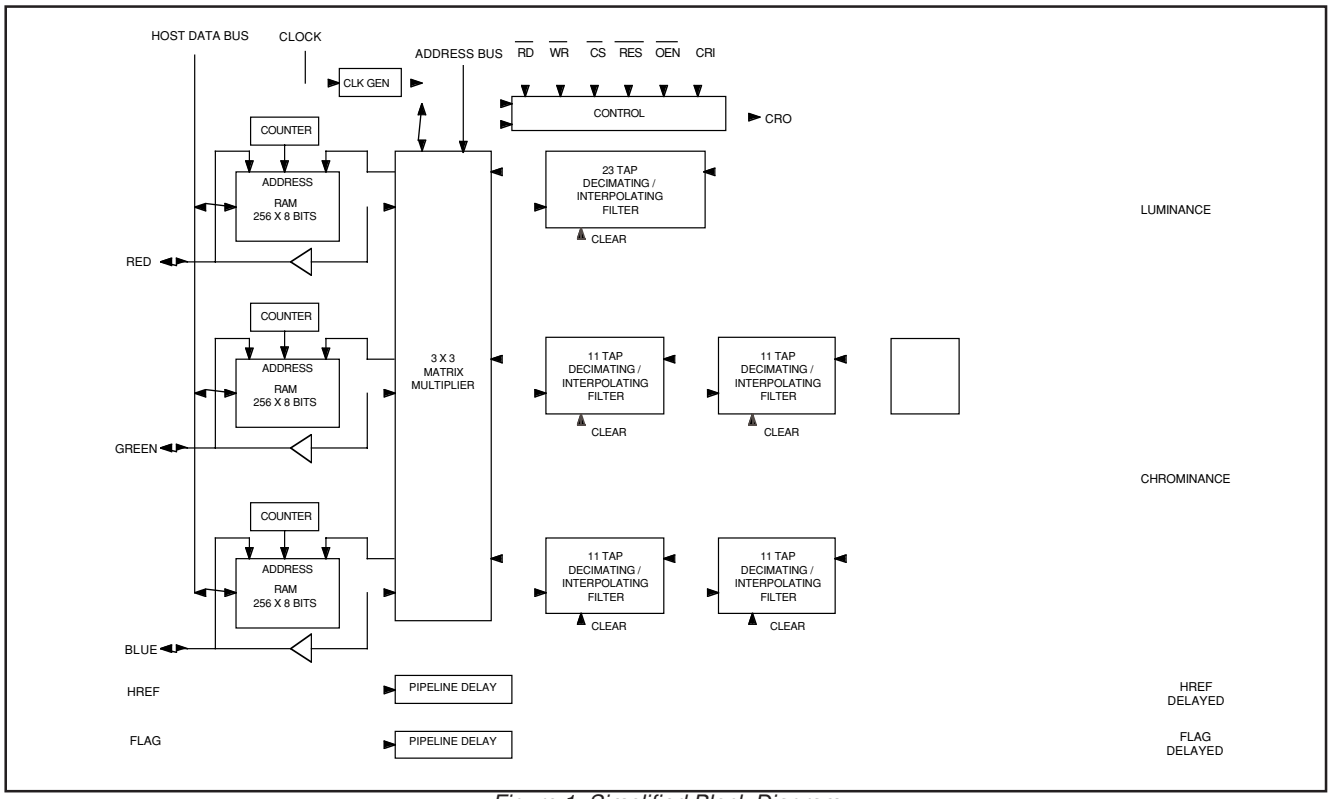


Figure 1. Simplified Block Diagram

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
R7:0	I/O	Unsigned Red data. Range may be changed by the RAM look up table
G7:0	I/O	Unsigned Green data. Range may be changed by the RAM look up table
B7:0	I/O	Unsigned Blue data. Range may be changed by the RAM look up table
Y7:0	I/O	Unsigned Luminance data in or out. Range is user definable
C7:0	I/O	Two's complement or offset binary multiplexed chrominance data. Range is user definable
D7:0	I/O	Host data bus used for reading or writing
A4:0	I	Host Address Bus. Matrix coefficients and the control register are directly addressable
CLK	I	External line locked clock. All inputs and outputs are referenced to the rising edge
HREF	I	Horizontal or Composite reference used as a start of line indicator and to clear the FIR filters
HDLY	O	HREF input delayed by the 39 clock delay to a correctly filtered output
FI	I	Input Flag as defined by the user. No internal operation.
FO	O	FI delayed by the 39 clock delay to a correctly filtered output
CRI	I	An input which indicates that valid luminance and chrominance data is present
CRO	O	An output which indicates that valid luminance and chrominance data is on the output pins
$\overline{OEN}$	I	Active low output enable for the tristate bus. Used in conjunction with a Control Register bit
$\overline{CS}$	I	Active low Chip Select from the host system
$\overline{RD}$	I	Active low request from the host to read the matrix coefficients and RAM contents
$\overline{WR}$	I	Active low request from the host to write to the device
$\overline{RES}$	I	Asynchronous low reset used to initialise the device. Must be present for at least 1024 clock periods

LOOK UP TABLES

When the device is configured to produce chrominance and luminance outputs from RGB inputs, each of the three look up tables is addressed by its appropriate colour bus. Any changes to the data thus occur before the colour space conversion. Typically the look up tables are used to provide gamma correction to linear RGB inputs, and / or to limit the range of the inputs. The coefficients in the conversion matrix are usually defined to expect either a range of 1 - 254 or 16 - 235, when converting to Cr and Cb chrominance values.

When the device is configured to produce RGB outputs, the look up tables are positioned just before the output buses. If linear outputs are required the tables can then be used to remove the gamma correction which is produced by the coefficients in the conversion matrix. They can also be used to expand the range produced by the conversion matrix.

The RAM's are not dual ported and use by the host system takes priority over pixel accessing. The RAM's are not directly addressable from the host since the device only uses a 5 bit address bus. Instead each RAM has an internal address counter which must be cleared by writing to address decimal 27. Data is then sequentially written to the Red RAM by supplying 256 bytes of data and address 28. Similarly using address 29 will cause write operations to the green RAM, and address 30 will cause write operations to the blue RAM. The counters do not wrap around and must be reset by using address 27 before further write or read operations are required. Read operations are mechanized in a similar manner to write operations, except that a read strobe must be supplied instead of a write strobe. Since each RAM has its own address counter the red, green, and blue operations can be intermingled on a byte by byte basis, rather than completing one colour before starting the next.

Although host operations are asynchronous to the device clock, this clock must be present to internally effect a read or write operation. The read and write strobes are internally synchronized to the clock, and the read strobe must be active for at least five clock periods, and the write strobe for two clock periods.

CONVERSION MATRIX

The 3 x 3 matrix multiplier performs the following basic operation on three channels with identical sampling rates;

$$\begin{vmatrix} O/PA \\ O/PB \\ O/PC \end{vmatrix} = \begin{vmatrix} c1 & c2 & c3 \\ c4 & c5 & c6 \\ c7 & c8 & c9 \end{vmatrix} X \begin{vmatrix} I/PA \\ I/PB \\ I/PC \end{vmatrix}$$

When converting from RGB to colour difference information, any decimation of the chrominance channels must be done after the above operation. Conversely when producing RGB data the chrominance channels must be interpolated before the matrix operation. The configuration bit in the Control Register takes care of this reorganization.

The coefficients C9:1 are loaded from the host system, and are directly addressable using the 5 bits provided (see Table 1). Each coefficient must be loaded as two bytes since it uses a total of 12 bits. The upper 4 bits in the most significant byte are don't care values. If the loaded values are read back by the host, these four bits will always be zero's, and are not sign bits.

The 12 coefficient bits are comprised of 3 signed integer and 9 fractional bits. This gives a decimal range of -4.00 to approximately +3.998, with the fractional bits actually giving a decimal resolution of 0.001953.

Pixel data going into the matrix multiplier uses a total of 13 bits; 10 signed integer bits plus 3 fractional bits. This additional pixel accuracy is only obtained from the output of the interpolating filters, where 10 integer bits are necessary to accommodate signed data with undershoot and overshoot beyond the nominal gain.

In the RGB to chrominance and luminance mode, when pre interpolation does not occur, only 8 unsigned integer bits are available from the look up table. Thus, within the 13 bit total, the top 2 bits plus the bottom 3 bits will be made into zero's.

Intermediate precision within the matrix multiplier grows to 15 signed integer bits plus 6 fractional bits. The least significant 9 or 10 of the integer bits are selected at the output, and the fractional bits are rounded to 3 bits. Ten integer bits are used when the matrix is producing RGB from interpolated chrominance and luminance. This allows for undershoot and overshoot beyond the nominal 8 bit unsigned value.

Only 9 integer bits are necessary when the matrix is producing chrominance, and the three fractional bits provide additional precision into the decimating filter. In fact, if the matrix is producing normalized chrominance, the coefficients will have been chosen to produce an output in the range ±127. This range only requires 8 integer bits, and the ninth bit will be a repeated sign bit. Note that ±127 is actually representing ±0.5 in this context. When the NORM bit in the Control Register is reset, the chrominance outputs lie in the range ±1, or ±256 in our internal representation. The full 9 integer bits are then needed.

LUMINANCE FILTER

The luminance channel contains a 23 tap low pass filter with internally defined 10 bit signed coefficients. When the MODE bit in the Control Register is reset the filter will decimate the sampling rate by two. When the MODE bit is set the filter will interpolate the incoming data to produce outputs at twice the incoming sampling rate. The filter coefficients remain the same in both cases, but the gain is adjusted to preserve the energy content..

When the filter is producing decimated luminance it accepts data from the matrix converter with 9 signed integer bits plus 3 fractional bits (9.3). Since luminance is always positive, however, the most significant bit will be zero. Words within the filter calculation are allowed to grow to 15 integer bits plus 6 fractional bits. This is then rounded to 15 bits plus 3 fractional bits, and finally the 10 least significant integer bits are chosen to give a 10.3 result. The 10 bit integer component allows for any undershoot or overshoot in the nominal 0 to 255 luminance range. The three fractional bits are used to round the integer component to a 10 bit value. This is then clipped to a value between 0 and 255. Negative values become zero, and positive values greater then 255 will saturate at 255. Outputs will not saturate under normal operating conditions, and the circuit is only necessary to prevent overflow when the input swings between the maximum and minimum values. Figure 2 illustrates the bit significance at various points in the data path.

When the filter is used to interpolate incoming luminance data, the 8 bit input is padded to the 9.3 format used previously. The 13 bit output from the filter is applied to the matrix converter without further rounding.

The response given by the filter is shown in Figure 3. Stop band attenuation is approximately 45 dB, and the maximum pass band ripple is 0.07 dB. These figures were obtained with 10 bit quantized coefficients and unquantized data. The effects of the various quantization steps within the filter, plus the reduction to 10 bits, is superimposed upon Figure 3. Also shown is the CCIR601 specification for a luminance or RGB

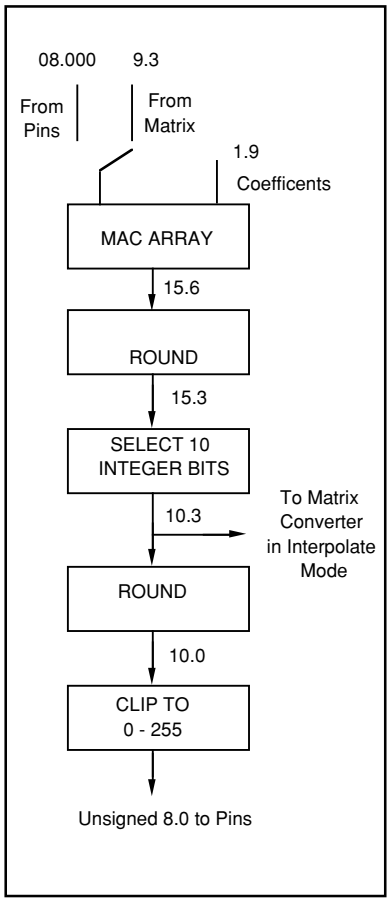


Fig 2. Bit significance in the Y Filter

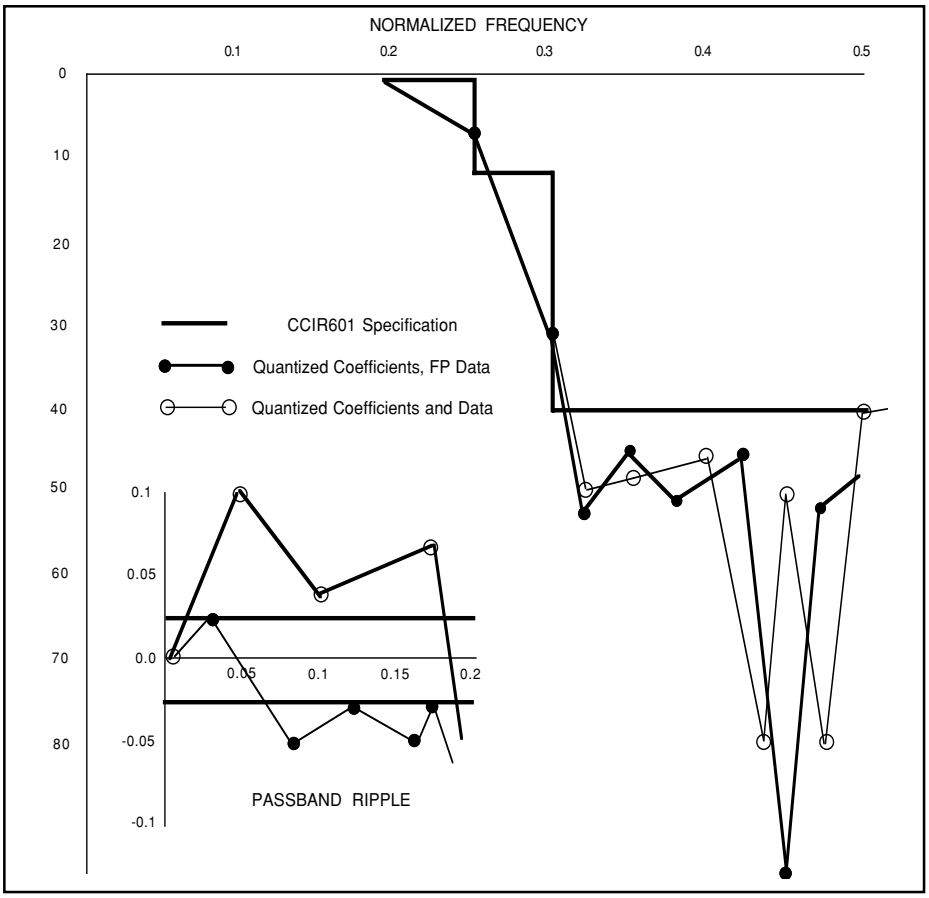


Figure 3. Response of the Luminance Filter

filter with 13.5 MHz output sampling.

CHROMINANCE FILTERS

Each chrominance channel has two 11 tap filters in series and each pair can decimate or interpolate by four. The MODE bit defines whether the filters interpolate or decimate. The coefficients are 10 bit internally defined values, and are the same in both modes. Figure 4 illustrates the bit significance at various points in the calculation.

When the filters are used to decimate chrominance produced by the matrix converter, the inputs are represents by either 8 or 9 signed integer bits plus 3 fractional bits. When the matrix coefficients have been chosen to produce normalized chrominance, the range can be represented by 8 integer bits. Otherwise 9 integer bits are needed. When the inputs are chrominance from the pins, the 3 fractional bits are set to zero, and the ninth bit is sign extended. Words within the filter calculation are allowed to grow to 15 integer bits plus 6 fractional bits. This is then rounded to 15 bits plus 3 fractional bits.

When the filter is used to supply interpolated data to the matrix converter, the least significant 10 integer bits are selected out of the 15 outputs. Only 9 integer bits are actually needed to represent the filtered chrominance with undershoot and overshoot, but the hardware multiplier expects a 10 bit number.

When the filter is producing decimated chrominance, the NORM bit in the Control Register is used to select which 12 integer and fractional bits will be used by the rounding and clipping circuit. For a full description of this operation see the section on Chrominance Outputs.

The response of the filters is given in Figure 5. These results were obtained with 10 bit quantized coefficients and unquantized data. The effects of the various quantization steps within the filter, and then finally rounding down to a 9 bit value are superimposed onto Figure 5. Also shown is the CCIR601 specification for sample rate conversion down to 4:2:2 resolution.

RGB INPUTS

The 24 bit RGB data must meet the set up and hold requirements, with respect to the rising edge of the clock, which are specified in Figure 6. The first edge after HREF has gone inactive (i.e. high) must strobe in the first samples if the delay to the first correctly filtered output is to match the fixed pipline delay of 39 clock to the HDLY and FO outputs. The maximum range is 0 to 255 for each component. If the coefficients in the matrix converter are defined for a restricted input range then this must be guaranteed by the user. Alternatively the look up tables can be used to limit the range. When HREF goes active low the outputs will go low after 39 clocks.

The VP510 has been designed to accept two times oversampled RGB data from an A/D converter. This avoids the need for analog anti aliasing filters before the A/D converters. For this reason the clock used by the VP510 is expected to be twice the sampling clock needed to produce a given number of RGB pixels per line. If the RGB inputs have not been oversampled this double rate clock should still be used. Each incoming sample will then be internally used twice, but the decimating filters will still produce the correct luminance and chrominance values.

Each input directly addresses its own RAM, which has been pre-loaded to meet the system requirements. Linear

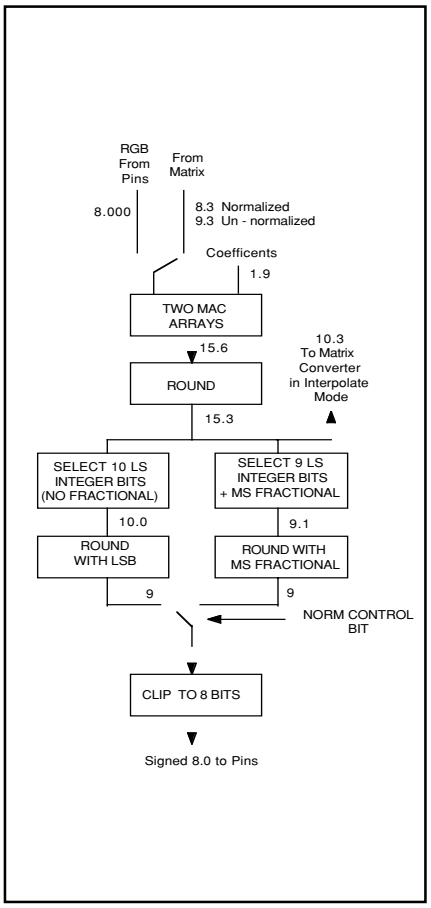


Figure 4. Bit significance

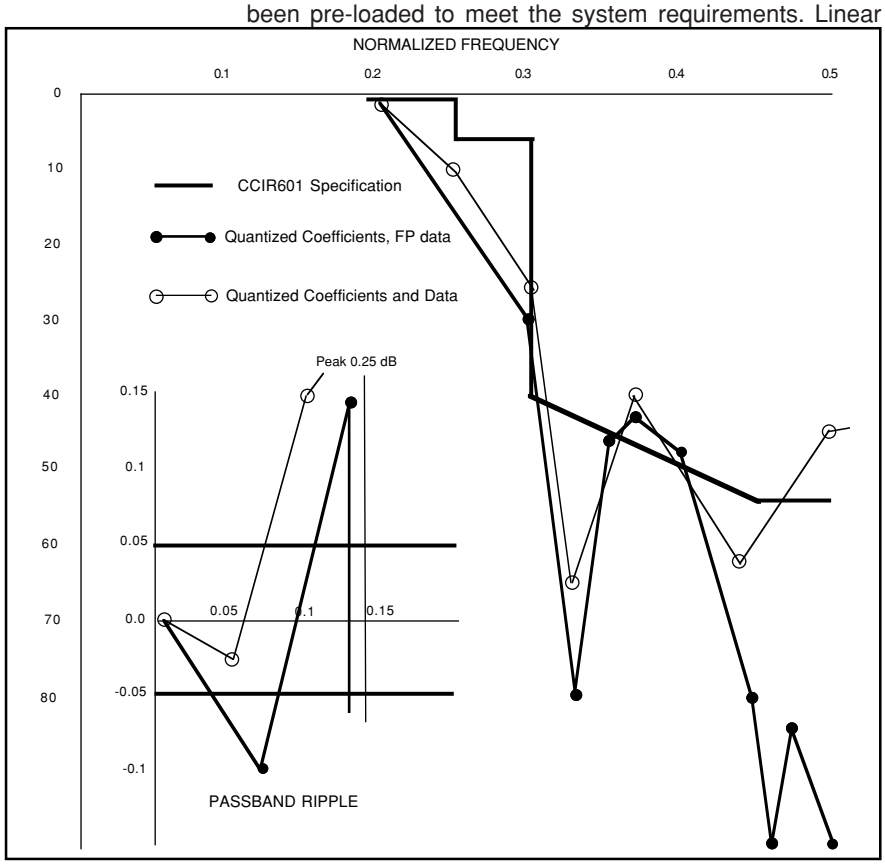
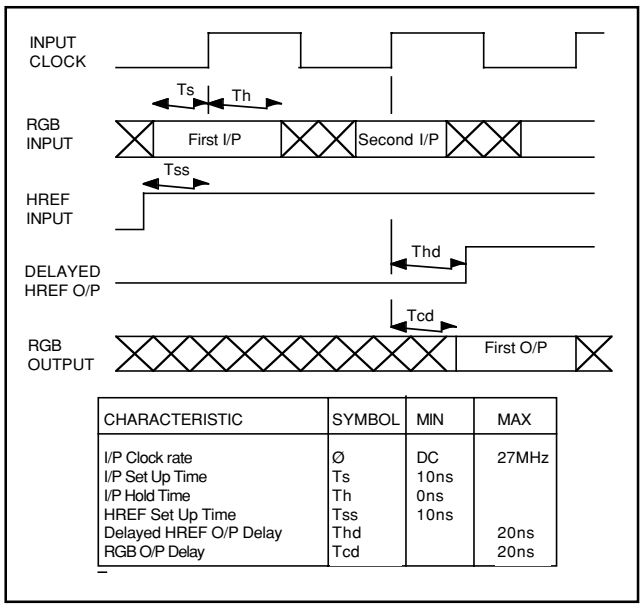


Figure 5. Response of the Chrominance Filters



CHARACTERISTIC	SYMBOL	MIN	MAX
I/P Clock rate	Ø	DC	27MHz
I/P Set Up Time	Ts	10ns	
I/P Hold Time	Th	0ns	
HREF Set Up Time	Tss	10ns	
Delayed HREF O/P Delay	Thd		20ns
RGB O/P Delay	Tcd		20ns

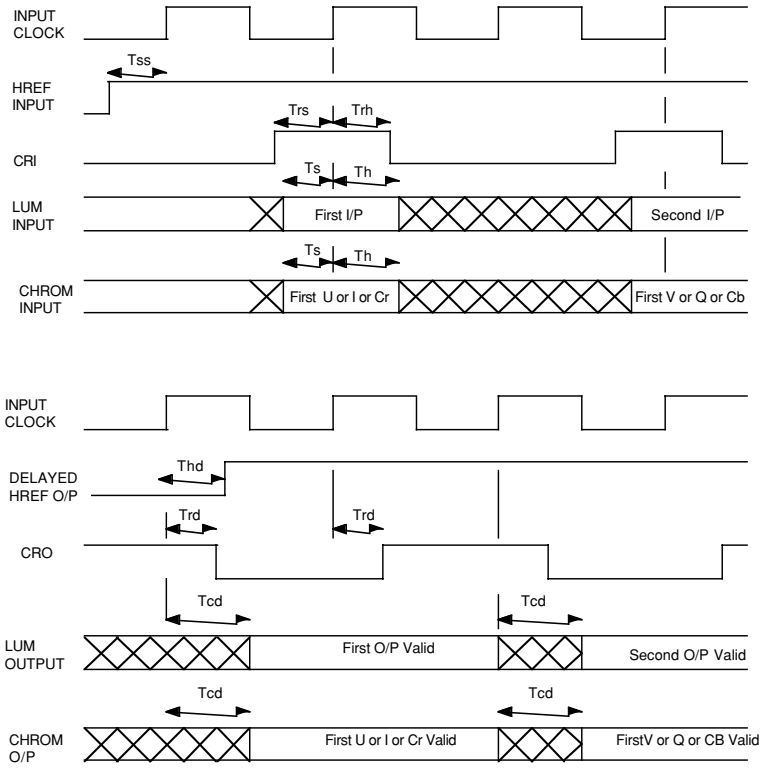
Figure 6. RGB I/O Timing (Advanced Data)

RGB data must normally be gamma corrected by the RAM's before colour space conversion.

LUMINANCE AND CHROMINANCE INPUTS

The 16 bit luminance and chrominance values must meet the set up and hold times, with respect to the rising edge of the clock, which are specified in Figure 7. Since the input rate will be half the clock rate an additional signal is required to indicate alternate clock periods. This signal (CRI) must also meet the set up and hold requirements given in Figure 7. On the first occurrence of CRI after HREF goes inactive (High), the 16 bit input bus must contain the first 8 bit luminance component plus the first 8 bit U,I, or Cr component, if the delay to the first correctly filtered output is to match the fixed pipeline delay to the HDLY and FO outputs. On the second occurrence it must contain the second luminance component plus the first V, Q, or Cb component. When HREF goes low the outputs will be forced low after the 39 clock pipeline delay.

YUV or YIQ data is directly applied to the interpolating filters by setting the BYPASS Bit in the Control Register. When Y Cr Cb data is to be used this bit should be reset, and the inputs will then be applied to the ranging and offset circuitry. The SEL bit in the Control Register is used to determine the ranging options. If this bit is reset then the Y input will be



CHARACTERISTIC	SYMBOL	MIN	MAX
I/P Clock Rate	Ø	DC	27 MHz
I/P Set Up Time	Ts	10ns	
I/P Hold Time	Th	0ns	
HREF Set Up Time	Tss	10ns	
CREF Set Up Time	Trs	10ns	
CREF Hold Time	Trh	0ns	
Delayed HREF O/P Delay	Thd		20ns
CREF O/P Delay	Trd		20ns
Data O/P Delay	Tcd		20ns

Figure 7. Chrominance I/O Timing (Advanced Data)

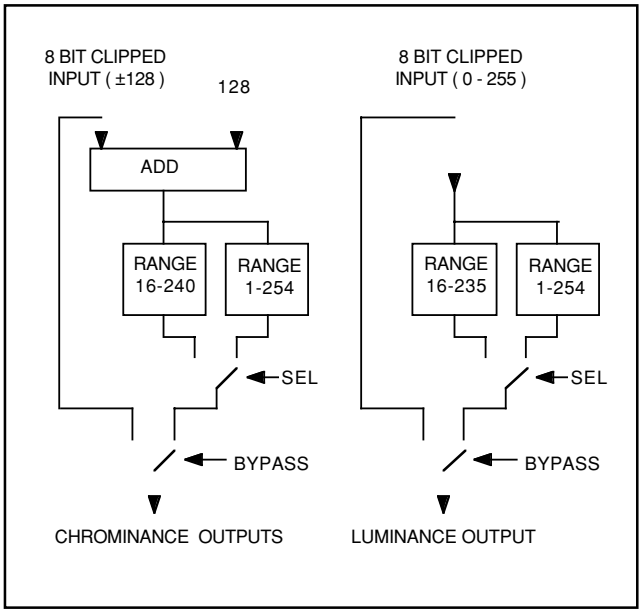


Figure 8. Chrominance and Luminance Output Options

adjusted to have a range of 16 - 235, and the Cr and Cb inputs will be adjusted to 16 - 240. If the SEL bit is set the range will be 1 - 254 for all three inputs. After either ranging option 128 is subtracted from the Cr and Cb channels before they are applied to the matrix converter. Note that if the incoming Y Cr Cb data is already correctly ranged then the range circuit will have no further action. The BYPASS pin must, however, still be reset or the offset of 128 will not be subtracted from the chrominance channels.

RGB OUTPUTS

RGB outputs will be valid after the delay from the rising edge of the clock given in Figure 6. A version of the HREF input is provided (HDLY), which has been delayed by the same number of clock periods as the data. This indicates when the first converted samples are available from each line.

In normal operation of the VP510 the clock input will be two times the sampling clock required to produce a given number of pixels per line. The device then produces RGB outputs at this double rate, and thus avoids the needed for analog anti aliasing filters after the D/A converters. Incoming luminance data is interpolated by two, and chrominance data by four, to achieve these output rates.

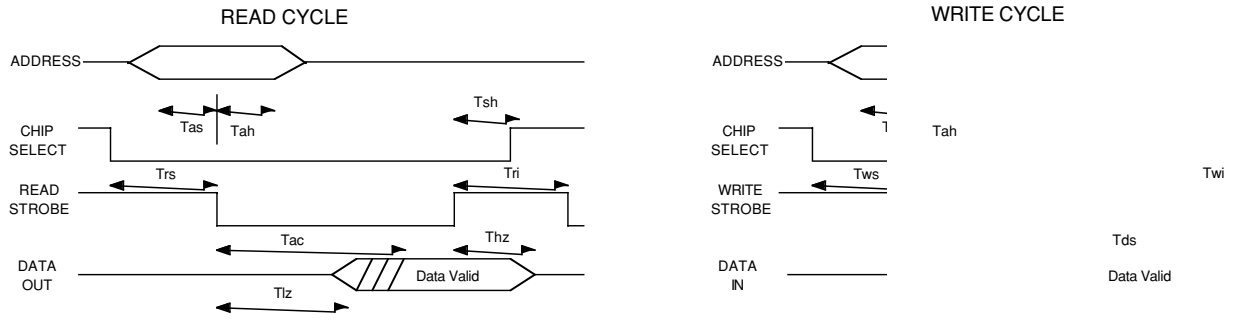
For standard CCIR601 video with 720 RGB pixels per line the clock needed would thus be 27 MHz. For square pixel NTSC a clock of 24.54 is needed, and square pixel PAL needs a clock of 29.5 MHz.

If the RGB outputs are connected to a frame store rather than driving a D/A converter, then these oversampled outputs are probably not needed. Since the RGB data will not contain any frequencies above one quarter the clock rate used by the VP510, then the user can simply just use every other output sample without causing aliasing effects.

Each 8 bit output value is obtained from the output of the matrix converter, which is internally represented by 13 bits. This comprises 10 signed integer bits plus three fractional bits. At this point the RGB values have a range of -512 to +511, which is sufficient to accommodate any overshoot or undershoot produced by the filters. If the most significant fractional bit is set, then the integer bits are incremented by one, and the result is then clipped. Negative values will be forced to zero, and values greater than +255 will be forced to saturate at +255. The resulting unsigned 8 bit number is made available on the output pins, as shown in Figure 2.

LUMINANCE AND CHROMINANCE OUTPUTS

The 16 bit output bus changes on alternate rising edges of the clock, with the delay specified in Figure 7. Each output remains valid for two clock periods and is either comprised of a luminance byte plus a U, I, or Cr component, or another luminance byte plus a V, Q, or Cb component. The sequence of events following the HREF delayed output is shown in Figure 7. The CRO signal can be used as a clock enable or a half rate clock for the next component in the system.



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Trs	0ns	
Chip Select Hold Time	Tsh	0ns	
Strobe In active Time	Tri	Øns	
Data Access Time	Tac		10 +5Øns
Delay to O/P's low Z	Tlz	4Øns	
Delay to O/P's high Z	Thz		25ns

NOTE

Ø is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN
Addresss Set Up Time	Tas	10ns
Address Hold Time	Tah	10ns
Chip Select Set Up Time	Tws	0ns
Chip Select Hold Time	Tsh	0ns
Strobe In active Time	Twi	3Øns
Strobe Active Time	Twa	2Øns
Data Set Up Time	Tds	10ns
Data Hold Time	Tdh	10ns

Figure 9. Host Interface Timing (Advanced Data)

ADDR	FUNCTION	ADDR	FUNCTION
0	C1 L Byte	1	C1 H Byte
2	C2 L Byte	3	C2 H Byte
4	C3 L Byte	5	C3 H Byte
6	C4 L Byte	7	C4 H Byte
8	C5 L Byte	9	C5 H Byte
10	C6 L Byte	11	C6 H Byte
12	C7 L Byte	13	C7 H Byte
14	C8 L Byte	15	C8 H Byte
16	C9 L Byte	17	C9 H Byte
27	RAM Address Reset		
28	R/W Red RAM		
29	R/W Green RAM		
30	R/W Blue RAM		
31	Control Register		
18 - 26	Not Used		

Table 1. Internal Address Map

Internally the luminance component obtained from the decimating filter is represented by the 10 least significant integer bits plus 3 fractional bits. The 10 integer bits accommodate any undershoot or overshoot caused by the filter. If the most significant fractional bit is set, then the integer bits are incremented by one. The resulting 10 bit signed integer value ,representing ± 512, is then clipped to provide an 8 bit, positive only, number. Negative values become zero, and values greater than 255 will saturate at 255.

The NORM bit in the Control Register determines which bits out of the 15.3 available are selected from the outputs of the chrominance filters. The choice is illustrated in Figure 4. If the user is working with normalized chrominance, then the matrix coefficients will have been chosen to produce outputs in the range of ±128 (representing ±0.5). This range only requires 8 signed integer bits, and the ninth bit going into the filter will be a repeated sign bit. The 9 least significant integer bits are then selected out of the 15 available from the output of the filter. These are then sufficient to accommodate any undershoot and overshoot beyond the 8 bit input, and are rounded with the most significant fractional bit. The resulting 9 bit signed value is clipped to an 8 bit signed number with a range of ±128, representing ±0.5. Values outside the range are clipped to the maximum values allowed.

When chrominance is not normalized the range becomes ±1, or ±256 in our internal notation. This range needs all 9 bits of the integer component going into the filter, and requires 10 integer bits coming out of the filter to allow for undershoot and overshoot. The 9 bit value expected by the clipping circuit is now produced by using the least significant integer bit to round the next 9 integer bits. This word is then clipped to an 8 bit signed value with a range of ±128, but now representing ±1 since higher order bits were selected at the output of the filter.

If the BYPASS bit is set in the Control Register, these values are passed directly to the output pins. If this bit is reset they are further modified in a manner determined by the SEL bit in the Control Register. This is illustrated in Figure 8.

If the SEL bit is set, then zero luminance values become 1 and value 255 is clipped at 254. If the SEL bit is reset, then values below 16 will be forced to decimal 16 and values greater than 235 will be forced to 235.

When the BYPASS bit is reset decimal 128 will be added to each chrominance channel, to provide a positive only number. The SEL bit then either limits the range to 1 to 254 or to 16 to 240. Values outside those ranges are respectively forced to the minimum or maximum values. Note that if the BYPASS pin is reset then the NORM bit must be set.

HOST INTERFACING

The VP510 utilizes a conventional microprocessor interface except that the RAM based look up tables are not directly addressable. The address inputs must meet set up and hold times with respect to the front edge of the read and write strobes. These are given in Figure 9. Note that the address inputs are internally latched, and need not stay valid for the whole of the strobe times. Chip select, however, must stay active for the whole of the strobe times.

Data, which is to be written to the RAM or Control Register, must meet set up and hold times with respect to the back edge of the write strobe. These are also given in Figure 9. The device clock must be present for the write operation to occur, and internal synchronization takes place. For this reason the write strobe must be active for at least 2 clock periods.

Reading data from the VP510 also requires the presence of the device clock. Data from the RAM is internally pipelined and the read strobe must be active for at least 5 clock periods (4 pipeline delays plus synchronization). The output bus will not go low impedance before this pipeline delay.

The matrix coefficients and the Control Register are directly addressable, and use the locations given in Table 1. Four addresses are used to access the three RAM's, and the scheme used is descibed in the section on the look up tables.

DEVICE CONFIGURATION

The device is configured by means of bits in a Control Register. A reset pulse must be applied, whilst the device clock is active, before loading the Control Register. The reset pulse will actually clear all the control bits to zero, and ensure that neither output bus is low impedance, even if OEN is low.

The significance of the bits is given below. For a fuller description of individual bits see the releant sections.

BIT	NAME	FUNCTION
0	OEI	This bit must be set and the OEN pin must be low for either the 24 or 16 bit output bus to be low impedance. The status of the MODE bit determines which bus is actually enabled as an output. With this arrangement either bus can be controlled by software or by driving a pin.
1	SEL	This bit controls the range of the luminance and chrominance data. When high the I/O range is 1-254. When low the luminance is 16-235 and the chrominance is 16-240.
2	MODE	This bit selects the direction of operation. When low the 24 bit bus represents RGB inputs and the 16 bit bus represents luminance and chrominance outputs. The filters then deci mate. When high the data flow reverses and the filters interpolate.

3 BYPASS This bit should be reset when Cr Cb data is to being processed. NORM must then be set.It should be set when the ranging and offset circuit is to be bypassed.

4 NORM When this bit is reset the chrominance outputs are not normalized, and the 8 bit outputs rep resent a range of ±1. When NORM is set the outputs will represents a range of ±0.5, still using 8 bits.

7:5 Reserved. Must all be reset.

CONVERSION BETWEEN RGB AND YUV

If incoming, gamma corrected, analog RGB is normalized to a range of 0 to 1, then the following coefficients will produce YUV outputs. Y will have a range of 0 to 1, U will have a range of ±0.436, and V will have a range of ±0.615. The NORM bit must be reset, and the BYPASS bit set. The 8 bit chrominance outputs then represent a possible range of ±1.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.147 & -0.289 & 0.436 \\ 0.615 & -0.51 & -0.100 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The coefficients given below will produce gamma corrected RGB normalized to a range of ±1, when YUV have the ranges given above.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.140 \\ 1 & -0.395 & -0.581 \\ 1 & 2.032 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

These coefficients translate to the following HEX values, which define the 12 bit number to be loaded. Note that these are given as simple three digit HEX values, without a separate 3 bit integer and 9 bit fractional part.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ F64 & F6C & 0DF \\ 13A & EF8 & FCC \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 000 & 247 \\ 200 & F35 & ED6 \\ 200 & 410 & 000 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

If normalized digital UV components are required, the coefficients must be modified as given below. The NORM and BYPASS bits should then be set. The U I/O range is expanded to ±0.5, and the V I/O range is compressed to the same values. Y has an I/O range of 0 to 255. The 8 bit chrominance outputs now represent a range of ±0.5.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.169 & -0.331 & 0.500 \\ 0.5 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.42 \\ 1 & -0.344 & -0.714 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

The equivalent HEX values which be loaded into the device are given below;

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ FA9 & F56 & 100 \\ 100 & F29 & FD6 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 000 & 2CD \\ 200 & F4F & E92 \\ 200 & 38B & 000 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

CONVERSION BETWEEN RGB AND YIQ

The coefficients for converting analog RGB to YIQ are given below. The gamma corrected RGB inputs have a range of 0 to 1. Analog I and Q have ranges of ±0.596 and ±0.525 respectively, and the NORM bit must be reset to produce 8 bit outputs representing a range of ±1. The BYPASS bit must be set.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.596 & -0.275 & -0.321 \\ 0.212 & -0.523 & 0.311 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

In the opposite direction the following coefficients produce gamma corrected RGB, when the YIQ inputs have the ranges given above.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0.956 & 0.620 \\ 1 & -0.272 & -0.647 \\ 1 & -1.108 & 1.705 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

In HEX these values become;

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ 131 & F73 & F5B \\ 06C & EF4 & 09F \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 200 & 1E9 & 139 \\ 200 & F74 & EB4 \\ 200 & SDC8 & 368 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

The conversion between digital RGB and normalized digital YIQ requires the following coefficients. I and Q are then compressed to fall in the range of ±0.5, and the NORM bit must be set since the 8 bit chrominance outputs now represent ±0.5. The BYPASS bit must also be set.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.231 & -0.269 \\ 0.203 & -0.500 & 0.297 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.139 & 0.648 \\ 1 & -0.324 & -0.677 \\ 1 & -1.321 & 1.783 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

These correspond to the HEX coefficients gven below;

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 099 & 12C & 03A \\ 100 & F89 & F76 \\ 068 & F00 & 098 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

R		200	247	146		Y
G	=	200	F5A	EA5		I
B		200	D5B	391		Q

CONVERSION FROM Y Cr Cb TO RGB

The analog conversion matrix is given below;

R = Y + 1.402(Cr - 128)
G = Y - 0.714(Cr - 128) - 0.344(Cb - 128)
B = Y +1.772(Cb - 128)

If the Y Cr Cb ranges are all 1 to 254, then the RGB range produced will be 1 to 254. If the Y range is 16 to 235 and the Cr Cb ranges are 16 to 240, then the expected RGB range is 16 to 235. Incoming Y CR Cb data can be adjusted to either of these ranges by using the SEL bit in the Control Register. The input circuit also does the necessary subtraction of 128 from the Cr and Cb values (the BYPASS bit must be reset). The resulting HEX values which must be loaded into the coefficient store are given below;

C1	C2	C3		200	2CE	0
C4	C5	C6	=	200	E92	F50
C7	C8	C9		200	0	38B

The digital conversion matrix is given below;

R = Y + 1.37(Cr - 128)
G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)
B Y + 1.73(Cb - 128)

The corresponding HEX values are given below;

C1	C2	C3		200	2BD	0
C4	C5	C6	=	200	E9B	F54
C7	C8	C9		200	0	376

The digital matrix only functions correctly when the Y range is 16 to 235 and the Cr Cb ranges are 16 to 240. The RGB range produced should then be 16 to 235. Both the SEL and BYPASS bits should thus be reset.

CONVERSION FROM RGB TO Y Cr Cb

The analog matrix is given below;

Y = 0.299R + 0.587G + 0.114B
Cr = 0.5R - 0.419G - 0.081B + 128
Cb = -0.169R - 0.331G + 0.5B + 128

This can handle RGB ranges of either 1 to 254 or 16 to 235. If necessary the RAM based look up tables can be used to limit the range of the incoming RGB. The BYPASS bit must always be reset, and the NORM bit set, when producing Cr and Cb data.

The SEL bit is used to limit the range of the YCr Cb values which are outputed. When SEL is set all three output ranges are 1 to 254. When it is reset the Y range is 16 to 235, and the Cr Cb ranges are 16 to 240. Values ouside the range limits will be forced to the correct maximum or minimum value. The offset of 128 is added to the Cr Cb values before the ranging is done.

The HEX values which correspond to the analog matrix are given below;

C1	C2	C3		99	12D	3A
C4	C5	C6	=	100	F29	FD7
C7	C8	C9		FA9	F57	100

In the CCIR601 specification the digital matrix is expressed as fractions of 256, and is given below;

Y = 77/256R + 150/256G + 29/256B
Cr = 131/256R - 110/256G - 21/256B + 128
Cb = -44/256R - 87/256G + 131/256B + 128

The HEX values which correspond to this digital matrix are given below;

C1	C2	C3		9A	12C	3A
C4	C5	C6	=	106	F24	FD6
C7	C8	C9		FA8	F52	106

This matrix expects the RGB inputs to be in the range of 16 to 235, and also the SEL bit to detemine the output range.

CONVERSION BETWEEN RGB AND Y,R-Y,AND B-Y

The analog matrices used to convert between RGB and Y Cr Cb can also be used with normalized colour difference information. The BYPASS bit must, however, be reset to avoid the 128 offset circuitry. RGB and Y inputs and outputs will have a range of 0 to 255. Colour difference inputs and outputs will have a range of -128 to +127 (±0.5). The NORM bit should always be set.

When working with analog colour difference values the following coefficients should be used, with the NORM bit reset. R - Y will have a range of ±0.701, and B - Y a range of ±0.886.

Y		0.299	0.587	0.114		R
R-Y	=	0.701	-0.587	-0.114		G
B-Y		-0.299	-0.587	0.886		B

R		1	1	0		Y
G	=	1	-0.509	-0.194		R-Y
B		1	0	1		B-Y

The corresponding HEX values are given below;

Y		099	12C	03A		R
R-Y	=	167	ED3	FC6		G
B-Y		F67	ED3	1C6		B

R		200	200	0		Y
G	=	200	EFB	F9D		R-Y
B		200	0	200		B-Y

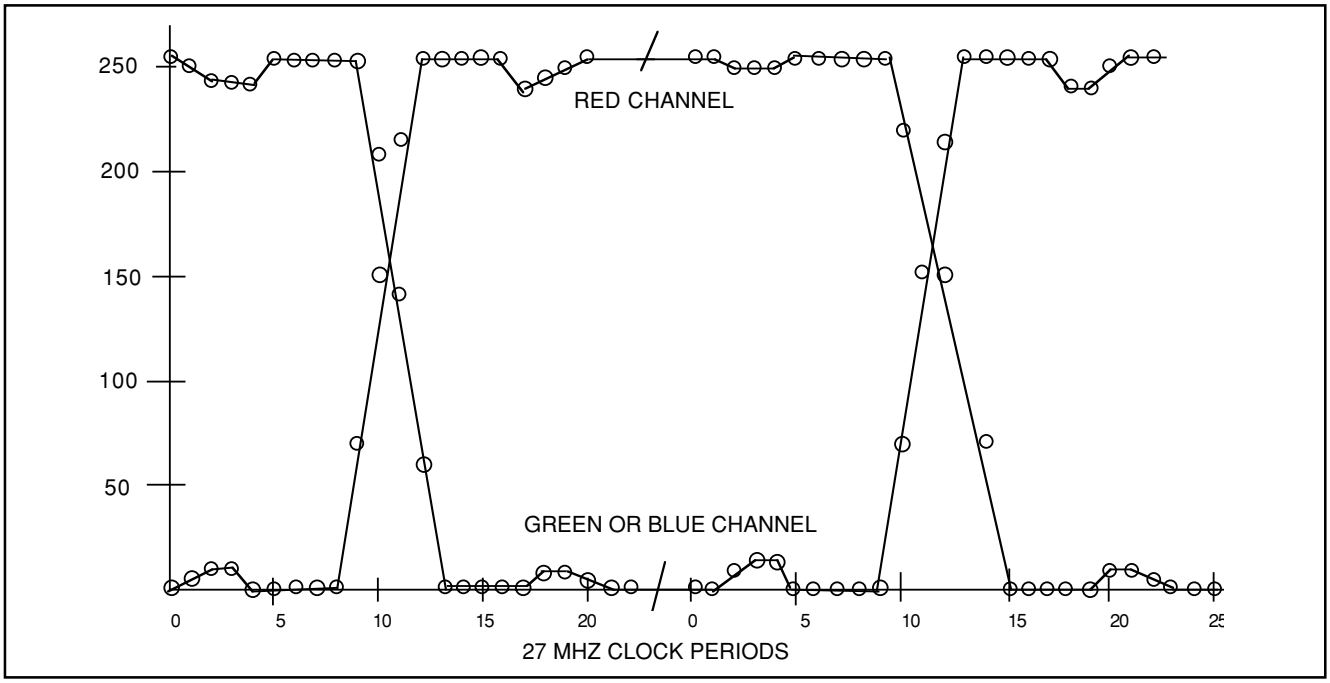


Figure 10. RGB Response to step changes in Y Cr Cb

RESPONSE TO INPUT STEP CHANGES

Figure 10 shows the actual response given by the RGB outputs to step changes in the Y Cr Cb inputs. Note that both negative undershoot and overshoot above 255 are prevented by the clipping circuit. The response of the Blue and Green filters will always be identical since they use identical circuits. The Red channel uses a different interpolating filter.

The Y Cr Cb changes were calculated to theoretically cause the RGB outputs to swing from maximum to minimum values, using the analog coefficients. Initial Y Cr Cb values were 151/20/43 with a step to 105/236/213. These should cause RGB to change from 0/255/0 to 255/0/255. The second transition was caused by changing the Y CR Cb values from 228/148/0 to 179/0/171. This should cause RGB to change from 255/255/0 to 0/255/255.

Figure 11 show the response of the Y Cr Cb outputs to maximum range step changes in RGB. The sequence used to cause the four transitions, and the theoretical results are given below.

	R	G	B	Y	Cr	Cb
Start	255	255	255	235	128	128
T1	255	255	0	226	149	16
T2	0	255	255	178	16	172
T3	0	255	0	148	21	44
T4	255	0	255	106	237	212

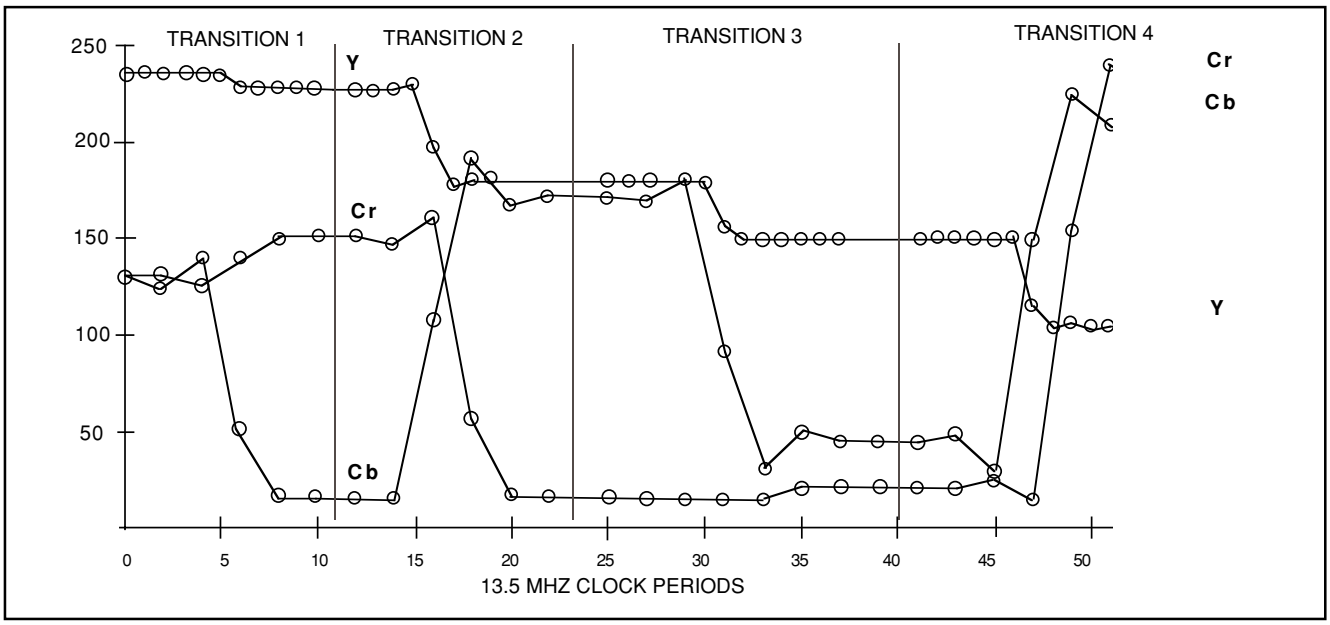


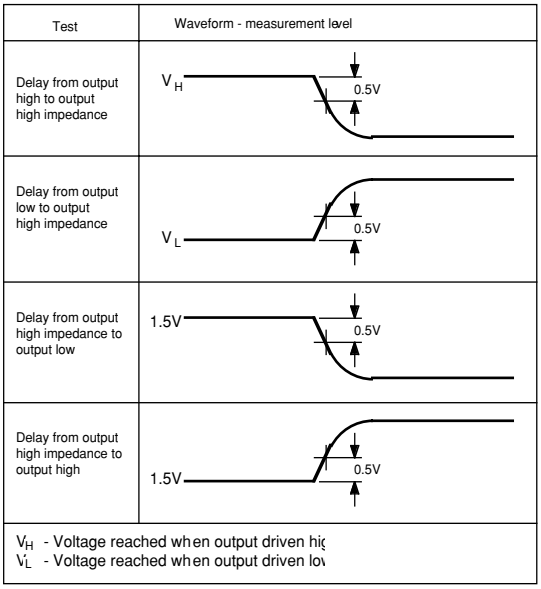
Figure 11. Y Cr Cb response to step changes in RGB

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	100°C
Package power dissipation	1000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.



STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C Vcc = 5.0v ± 10%

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Output high voltage	V_{OH}	3.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	3V for CLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
NC	1	R0	26	NC	51	C0	76
NC	2	GND	27	NC	52	NC	77
NC	3	NC	28	NC	53	GND	78
VDD	4	NC	29	VDD	54	NC	79
CLK	5	NC	30	Y7	55	NC	80
RES	6	VDD	31	Y6	56	VDD	81
GND	7	G7	32	NC	57	D7	82
OEN	8	G6	33	Y5	58	D6	83
GND	9	G5	34	NC	59	D5	84
FI	10	G4	35	Y4	60	D4	85
NC	11	G3	36	Y3	61	D3	86
HREF	12	G2	37	Y2	62	D2	87
FO	13	G1	38	Y1	63	D1	88
HDLY	14	G0	39	Y0	64	D0	89
CRI	15	GND	40	GND	65	GND	90
CRO	16	VDD	41	VDD	66	VDD	91
GND	17	B7	42	C7	67	A4	92
VDD	18	B6	43	C6	68	A3	93
R7	19	B5	44	C5	69	A2	94
R6	20	B4	45	C4	70	A1	95
R5	21	B3	46	C3	71	A0	96
R4	22	B2	47	C2	72	CS	97
R3	23	B1	48	NC	73	RD	98
R2	24	B0	49	C1	74	WR	99
R1	25	GND	50	NC	75	GND	100

Pin Out Diagram

ORDERING INFORMATION

VP510 CG GPFR (Commercial Temperature - PLCC Package).

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