VP2611

H.261 Encoder

Supersedes June 1996 edition, DS3487 - 4.0

DS3487 - 4.1 December 1998

FEATURES

- Fully integrated H261 video encoder
- Up to full CIF resolution and 30 Hz frame rates
- Inputs YUV data in 8 x 8 sub block format
- Outputs run length coded coefficients
- On chip motion vector estimator with +/-7 pixel search window
- Addresses and control generated internally for DRAM frame store
- QFP package

ASSOCIATED PRODUCTS

- VP510 Colour Space Converter
- VP520S CIF/QCIF Converter
- VP2612 Video Multiplexer
- VP2614 Video Demultiplexer
- VP2615 H.261 Decoder

DESCRIPTION

The VP2611 Video Compression Source Coder forms part of a chip set used in video conferencing, video telephony and multimedia applications. It produces data which conforms to the H261 standard for video compression with rates between 64K and 2M bits per second. With a 27 MHz clock the device will accept data produced to full CIF resolution at 30 Hz frame rates. The pipeline latency through the device is only 3 macro block periods.

The VP2611 contains all the elements necessary for the compression algorithm. It incorporates a Motion Vector Estimator which performs a +/- 7 pixel search. The decision to use inter or intra frame compression is made by the device, and the selected data blocks are read from the frame store. New or difference data is then passed through a Discrete Cosine Transformer and quantized. Data from the quantizer is also inverse quantized and passed through an Inverse Discrete Cosine Transformer. This re-constructed data is then written to the frame store for use in the next frame period.This frame store is managed by an internal DRAM controller, and no external logic is needed.

The input data must be in YUV space, and must also conform to the six sub blocks per macro block format defined by H261. Any conversion from RGB format is performed by the VP510 Colour Space Converter. Any reduction in spatial resolution, down to CIF or QCIF requirements, is done by the VP520 Three Channel Video Filter.

The quantized data is zig-zag scanned and run length coded before being output, together with block information and motion vectors.

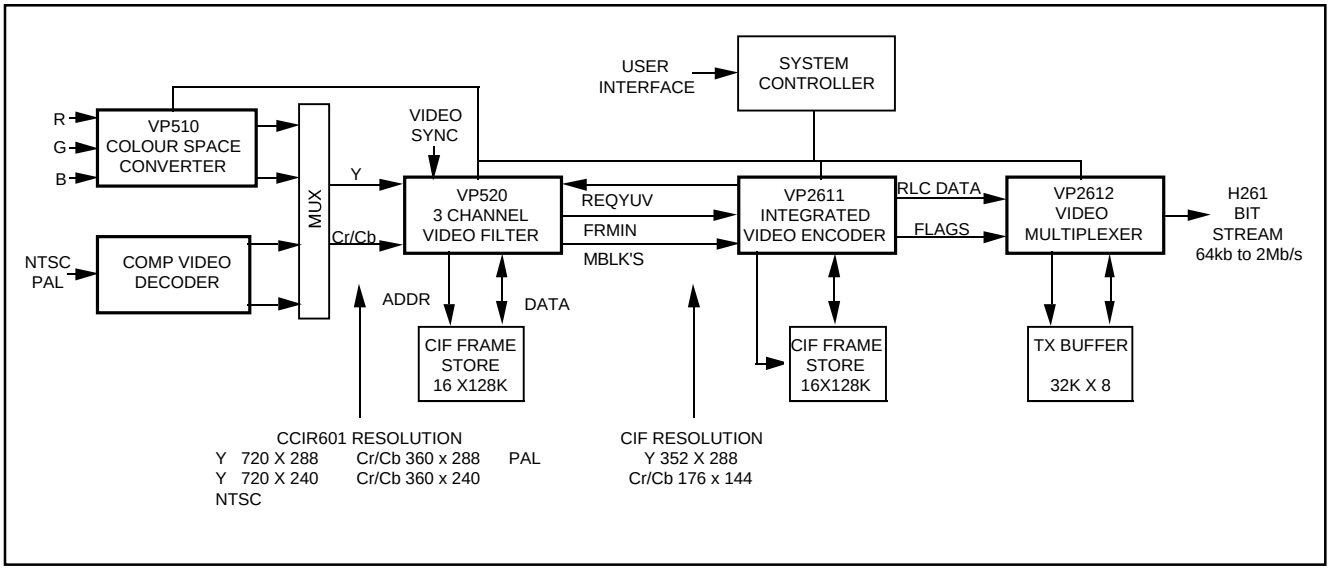


Fig 1 : Typical Video Conferencing Transmission System

PIN DESCRIPTIONS

YUV7:0	This input bus accepts YUV data one pixel at a time from the preprocessor, clocked in on the rising edge of PCLK.
PCLK	This signal is used to strobe in data at the YUV port and must be derived by dividing SYSCLK with an integer greater than one.
FRMIN	This input should be pulled high to prepare the VP2611 to code a new frame. It must be held high for at least one SYSCLK cycle and then must be pulled low again before the next frame begins. The VP2611 will respond to the rising edge of FRMIN by asserting REQYUV appproximately 184 SYSCLK cycles later.
REQYUV	This output is pulled high to request that YUV data be input for a new MacroBlock. It is pulled low again 1871 SYSCLK cycles later. It remains low during Dummy MacroBlocks and during the lay period between frames.
DBUS7:0	This output bus serves several functions as defined by DMODE3:0. In addition to providing the quantized coefficients and motion vectors, it is used to output control information.
DMODE3:0	Output flag port for DBUS7:0 bus. The value at this port identifies the data type appearing on DBUS7:0 during the same period.
DCLK	This output pulses high for a minimum of 37ns each time new data is output on DBUS or DMODE. It can be used as an edge sensitive strobe signal or a level sensitive "valid" signal.
SW15:0	This bidirectional port is connected to the frame store.
$\overline{RAS}$	Row Address Strobe output for the external DRAMs.
$\overline{CAS}$	Column Address Strobe output for the external DRAMs.
R/$\overline{W}$1	Read/Write control for external DRAM 1.
R/$\overline{W}$2	Read/Write control for external DRAM 2. N/C if 256k DRAMs.
$\overline{OE1}$	Output Enable control for external DRAM 1 or ADR8.
$\overline{OE2}$	Output Enable control for external DRAM 2. N/C if 256k DRAMs.
ADR7:0	Address output for the external DRAMs.
CBUS7:0	Bi-directional data bus for use by a Microprocessor. Data and insructions are clocked on and off the chip on the rising edge of CSTR.
$\overline{CSTR}$	Data strobe for the CBUS port.
$\overline{CEN}$	An enabling signal for the CBUS port.
CADR	When high, this signal defines CBUS as a data bus, and when low as an instruction input.
SYSCLK	System clock, run at 27MHz maximum. The clock must be high for between 35% and 65% of each clock cycle. This clock is used for all internal operations.
$\overline{RESET}$	Active low power on reset which must be held low for at least 2064 cycles.
TCK	Test clock for JTAG.
TMS	Test Mode Select for JTAG.
TDI	Input JTAG test data.
TDO	Output JTAG test data.
$\overline{TRST}$	Reset JTAG controller (active low).

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

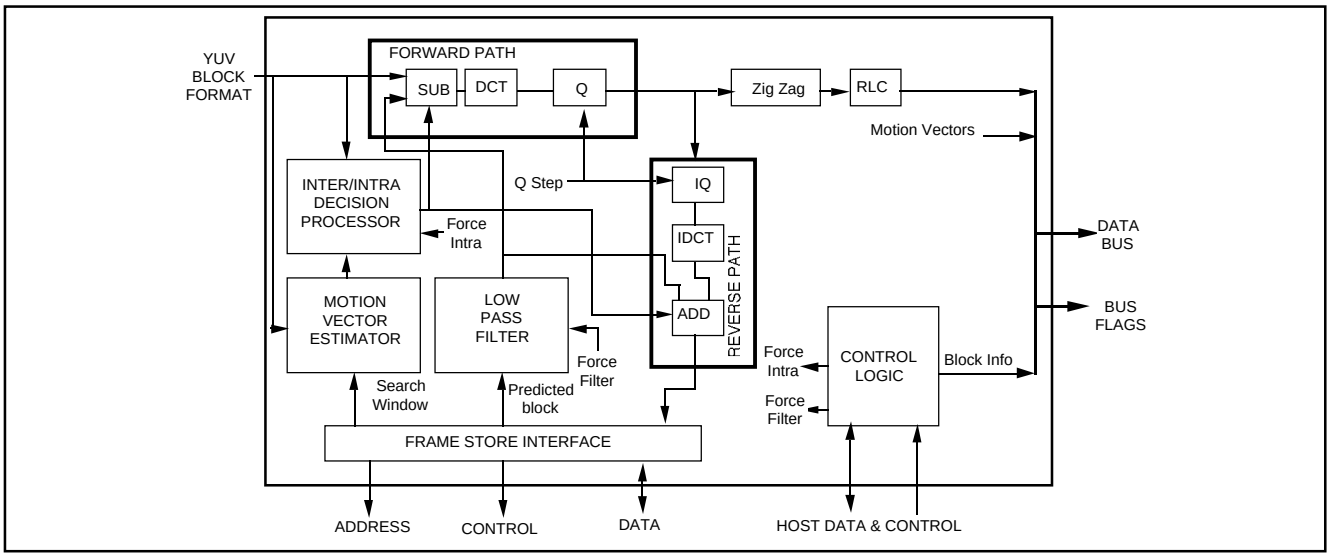


Fig 2 : Simplified Block Diagram

OPERATION OF MAJOR BLOCKS

Motion Vector Estimator

The motion estimator calculates the mean absolute error (MAE) for each possible position of the combined luminance block in a search window from the previous frame. The combined luminance block consists of 16 x 16 pixels, and in the search window this is displaced between -7 to +7 vertically, and -8 to +7 horizontally. The two lsb's of each pixel are discarded and the MAE value is contained within 14 bits.

The minimum MAE value, representing the best match between the previous and current block, is passed to the motion compensation decision block, together with the position of this best fit in the search window. The zero displacement MAE value is also passed to this block, which then decides whether the best fit is sufficiently better than the zero displacement fit. It uses the characteristic shown in Figure 3, where the 14 bit MAE is a Hex value. In the area to the right of the line all points defined by the two MAE values will cause motion compensation to be applied. In this case the best fit MAE value is used by the inter/intra decision processor, otherwise the zero displacement value is used.

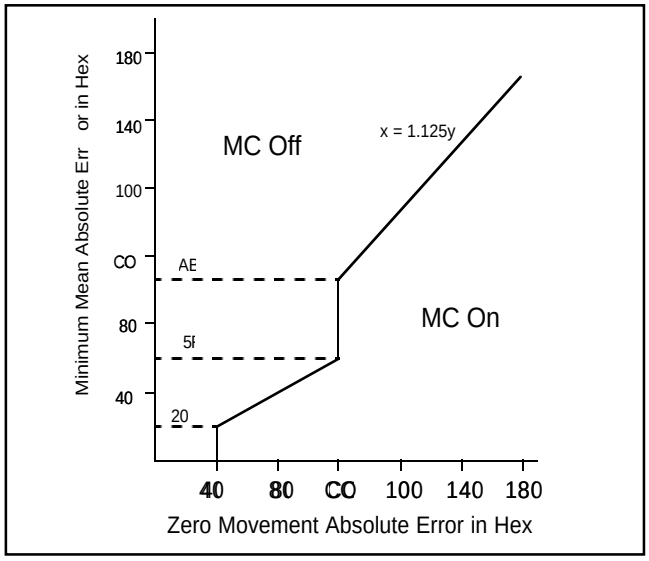


Fig 3 : MC Decision Slope

Inter/Intra Decision Processor

The MAE value passed by the motion compensation decision block is compared to the simplified variance of the current block. This simplified variance is calculated by summing the moduli of the differences between each luminance pixel and the mean luminance value over the whole macroblock. Eight bit pixels are used, and the variance value is expressed in 14 bits by discarding the two lsb's from the actual 16 bit result. It can then be directly compared to the 14 bit MAE value.

If the MAE value is below a user defined threshold inter mode coding is always selected. The default threshold is 3, on a scale from 0 to 255 using the 8 msb's from the 14 bit value. Above this threshold inter mode is only selected if the variance of the current block is greater than or equal to the MAE value in use.

In order to avoid gradual picture degredation, every 61st Macroblock input to the VP2611 is coded in intra mode regardless of the above decision. As 61 is a prime number, this will ensure that each macroblock will be transmitted in intra mode at least once in every 61 transmissions. If FIX MACROBLOCK or SKIP PICTURE is invoked this `Force Intra' counter will be disabled.

The user may overide the internal Inter/Intra decision at any time using the CBUS control port. A user generated forced inter mode will overide an internally generated `Force Intra'.

Low Pass Filter

The macroblock selected from the previous frame in motion compensated inter mode coding, will be filtered before it is subtracted from the current block. This decision can be overidden externally by the system controller. The Filter uses a simple [1 2 1] characteristic in both vertical and horizontal dimensions as specified in H.261 on the macroblock boundaries [010] is used.

SYMBOL	PARAMETER	MINIMUM	MAXIMUM
t RAC	Access time from RAS	-	105ns or under
t CAC	Access time from CAS	-	25ns or under
t RP	RAS precharge time	50ns or under	-
t CP	CAS precharge time	15ns or under	-
t RAS	RAS pulse width	90ns or under	-
t CAS	CAS pulse width	50ns or under	-
t REF	Time to refresh 256 rows	-	0.25ms or over

N.B. All times are quoted assuming 27MHz operation. For lower clock frequencies increase the above values proportionately.

Table 1 : External DRAM timing requirements

Frame Store Manager

The previous picture is stored in an external CIF DRAM frame store, which is connected by a glueless interface. The internal Frame Store Manager controls all read, write, and refresh operations to these DRAMs. No provision is made to allow the use of smaller DRAM's, if only QCIF operation is required.

During the coding of each macroblock columns of the search window are read from these DRAMs, and finally the "best fit" macroBlock is obtained. At the completion of coding the fully processed new macroblock is written to the DRAM's, after it has been decoded again. In this way the frame store maintains a bit-accurate duplicate of the image seen by the Decoder (excepting transmission errors).

Several configurations are possible to make the required 128Kx16 store. Two 64K x 16 DRAMs could be employed; in this case use the default 1M DRAM mode when setting up the chip. Otherwise, a single 256K x 16 DRAM or four 256K x 4 DRAMs could be used. In these last two cases use OE1 as ADR8, RW1 as R/W, and do not connect RW2 and OE2. Also, use the Setup instruction at the CPORT to put the device into 4M DRAM mode.

Table 1 details the critical timing parameters which the external DRAM must meet with SYSCLK running at 27MHz. Note that, if used at slower speeds, the requirements on the DRAM timing are relaxed with the exception of refresh. The number of refresh cycles the VP2611 produces is directly proportional to the SYSCLK frequency.

Discrete Cosine Transform

This circuit performs a Discrete Cosine Transform on each 8x8 sub block, whether in inter or intra mode. In intra mode, eight bit pixel data is used, with a ninth implied sign bit (all pixel data is positive). In inter mode the difference between the current and best fit previous block is used. This will be a two's complement number. Twelve bit coefficients are produced by the DCT, and passed on to the quantizer.

Quantize

This section quantizes the results of the DCT by dividing the 12 bit output from the DCT with a host supplied value. The 5 bit quantization value supplied corresponds to division of the 12 bit coefficients (range $\pm$ 2048) by values from 2 to 62, but in steps of 2. This variable quantization strategy allows the volume of data generated by the encoder to be adjusted dynamically, depending on the fullness of the transmission buffer. For H.261 applications it uses the quantisation value provided at the control port during the previous Macroblock period (or at some earlier time). An option is provided which allows two quantisation values to be used, one for use with inter coded macroblocks, and the other for use with intra coded macroblocks.

As specified in H.261, the DC coefficient of an Intra coded Block is treated differently and the 12 bit value is always divided by 8.

When the quantization value is small, and the DCT coefficient is large, there is a danger of overflow in the eight bit output. To avoid this a clipping circuit is included at the output of the quantizer, which saturates at the maximum values.

Zig Zag Scan

This is essentially an address generator which reorders the DCT coefficients according to the standard zig-zag scan pattern. This has the effect of concentrating the significant coefficients at the beginning of the sub-block, improving the efficiency of the Run Length Coder.

Run Length Coder

Each coefficient output from the zig zag scan is examined. If it is non-zero, then the Run Length Coding circuit will pass the coefficient magnitude to the output port along with its zero count i.e. the number of zero magnitude coefficients preceding it within the same 8x8 sub-block.

Inverse Quantize

This circuit replicates the operation of the inverse quantizer in the decoder. It reconstructs the 12 bit DCT coefficients from the 8 bit quantized inputs, using the 5 bit quantization value. This is achieved using the following formulae.

If QUANT is odd :
REC = QUANT*(2*LEVEL+1) : LEVEL > 0
REC = QUANT*(2*LEVEL-1) : LEVEL < 0

If QUANT is even :
REC = QUANT*(2*LEVEL+1)-1 : LEVEL > 0
REC = QUANT*(2*LEVEL-1)+1 : LEVEL < 0

For Intra Coded DC Coefficients :
REC = 8*LEVEL
except if LEVEL=255 when REC=1024

If LEVEL=0 then REC=0 in all cases.

The reconstructed values (REC) are passed through a Clipping Circuit in case of arithmetic overflow.

Thus, the Inverse Quantizer restores the DCT coefficients to their original value but with quantisation error.

Inverse DCT

This circuit replicates the operation of the Inverse Cosine Transform in the Decoder, and outputs 9 bit signed pixel data (intra mode) or pixel difference data (inter mode). The IDCT fully meets the CCITT specification.

Reconstruction Adder

In Inter Mode, the IDCT data is added to the best fit block from the previous frame store. In Intra mode, the IDCT data is simply added to zero. After the adder, the sign bit is removed from the result to give 8 bit pixels. Clipping circuits ensure that any pixels with values exceeding 255 are clipped to 255, and any with negative values are clipped to zero (such values are possible due to quantization noise).

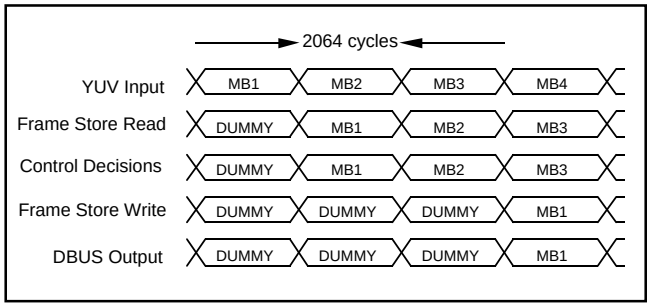


Fig 4: MacroBlock Pipelining

OPERATION OF INTERFACES

Macroblock Delays

The VP2611 has a three macroblock pipeline delay between pixel inputs and run length coded outputs. This is illustrated in Figure 4. Whilst the second macroblock is being input, the best fit macroblock from the previous frame is being identified and then read from the frame store. At this time any Control Decisions which are to effect the first macroblock must be supplied by the host controller. The run length coded outputs for the first macroblock are not available until the fourth macroblock is supplied at the input pins.

YUV Input Port

The YUV port accepts pixel data from the preprocessor in block format as illustrated in Figure 5. Within a complete system the VP2611 is always the master device, and must be supplied with macroblock data when it makes a demand. The order in which pixels are supplied is pre-determined, and must be strictly maintained. There are 64 pixels per sub-block and 4 luminance and 2 chrominance sub-blocks per macroblock. The macroblocks themselves are divided into groups of blocks (GOB's), and the sequence specified in H.261 must also be maintained. Note that, since the chrominance resolution is half the luminance resolution both vertically and horizontally, then the two chrominance blocks cover the same picture area as the four luminance blocks.

The pre-processor producing macroblock data must produce a frame start signal (FRMIN) when it has a complete frame of data available. This resets the input controller within the VP2611, which will then generate sequential GOB and macroblock numbers for the coded outputs referenced to this input.

FRMIN must go high for at least one system clock period, and must go low before the next frame is available. The VP2611 responds to FRMIN with a request for macroblock data (REQYUV), which occurs approximately 184 SYSCLK periods after FRMIN. It must then receive a complete macroblock within 1871 SYSCLK periods, and at the end of this time REQYUV will go inactive. The VP2611 must be provided with a PCLK signal to strobe in the data. This must be derived from SYSCLK, and must only be present when there is valid data at the input. Data must meet the set up and hold times with respect to PCLK as specified in Figure 6.

The maximum peak rate for PCLK is the SYSCLK rate divided by two, but since there are 384 bytes per macroblock

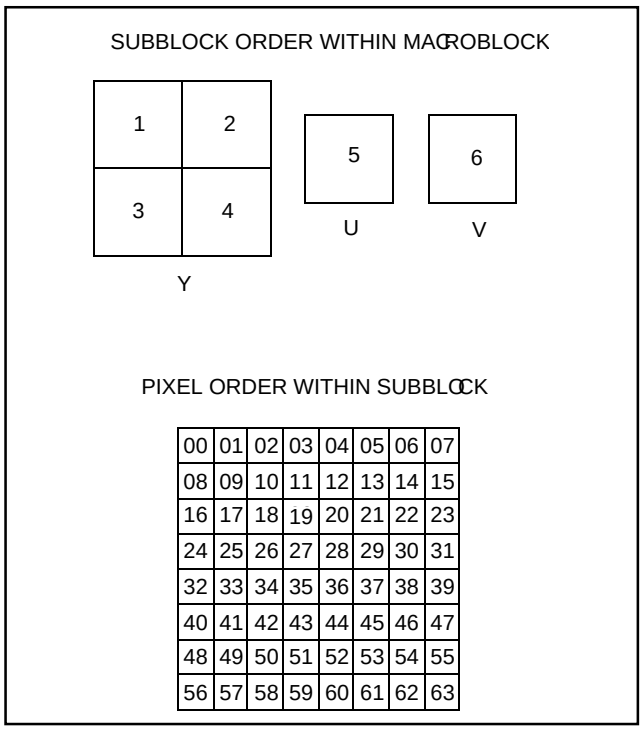


Fig 5 : Ordering of Pixels

then theoretically the average rate need only be 384/1871 times the SYSCLK rate. Note that PCLK must always be obtained by dividing SYSCLK by an integer greater than one. When the VP520 CIF/QCIF Converter is supplying the VP2611 with data, it provides a peak PCLK rate equivalent to SYSCLK divided by two, and an average rate of SYSCLK divided by four.

The mimimum gap between REQYUV going active is 2064 SYSCLK periods. In full CIF mode "dummy" macroblocks are internally inserted between rows, in order to give the chip sufficient time to load a new search window. No new YUV data must be loaded during these dummy macroblocks, and REQYUV will remain inactive. No dummy macroblocks are required in QCIF mode. With a 27MHz SYSCLK all macroblocks will be coded in less than a 30Hz frame rate period, and there will be a period of inactivity before FRMIN goes active again. During this period the output bus will remain static at all ones, and no output strobe (DCLK) will be produced.

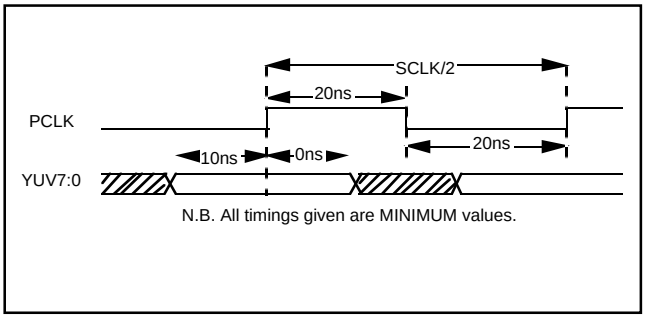


Fig 6 : Timing at YUV Port

DBUS Output Port

The DBUS port is used to pass data and control information directly to the VP2612 Video Multiplexer. The type of data on the output pins is identified by the DMODE 3:0 outputs, using the codes shown in Table 2. An output strobe is also produced (DCLK) which always goes high one system clock period after the data defined by DMODE 3:0 becomes valid. This edge is used to strobe the data into the Video Multiplexer, and thus the data set up time is always one SYSCLK period minus differential output delays.

The number of SYSCLK periods during which data remains valid is dependent on the type of data, and DCLK remains high for this same period. It goes low as the result of the same SYSCLK rising edge which produces a change in DMODE 3:0. The output delays with respect to SYSCLK are illustrated in Figure 8, and Figure 9 shows a typical output sequence during which DCLK remains high for several cycles as the sub-block number (code 7) is produced. During a Wait State
(code 15) no DCLK transitions are produced. The actual sequence of output events which occur for each macroblock, and the duration of each event, are illustrated in Figure 7.

The output events are defined in more detail below;

Control Decisions : This byte shows which control decisions have been taken for the forthcoming macroblock. DBUS0 will be high if a Fixed Macroblock (FIX MB) was enforced i.e. no new data will be transmitted this macroblock. DBUS1 indicates whether Inter (high) or Intra (low) coding was used for the macroblock. DBUS2 will be high if the macroblock was filtered, and DBUS3 will be high if motion compensation was used. DBUS5 will be high if the current frame is being coded in FAST UPDATE mode. In this mode the complete frame will be intra coded. DBUS6 will be high if the current frame is a SKIP FRAME i.e. not being coded - so no coefficients will be transmitted. DBUS4 and DBUS7 are not used.

DMODE3:0	FUNCTION
0000	GOB Number
0001	MB Number
0010	Control Decisions
0011	Quant Value
0100	Horizontal MV
0101	Vertical MV
0110	Coded Blk Pattern
0111	Sub-Block No
1000	Zero Run Count
1001	RLC Coefficient
1010	Not used
1011	Not used
1100	Not used
1101	Not used
1110	Not used
1111	Wait State

Table 2 : DBUS Functions

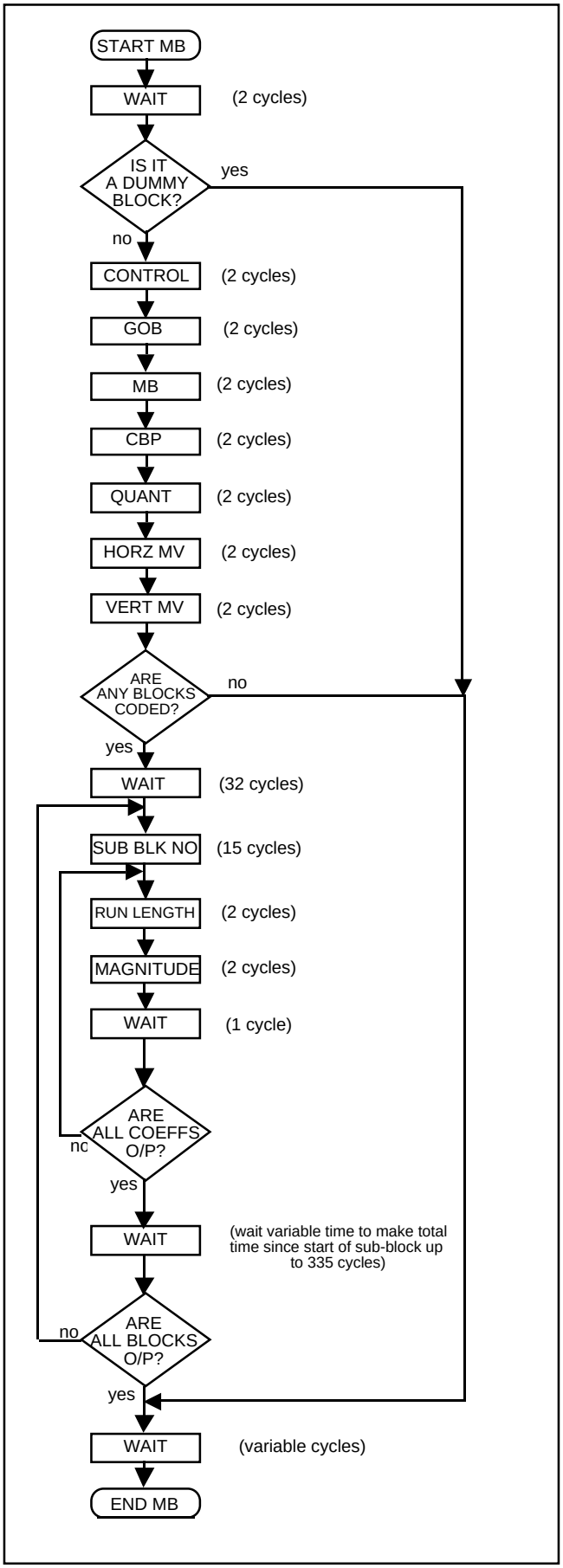


Fig 7 : DBUS Port Flow Chart

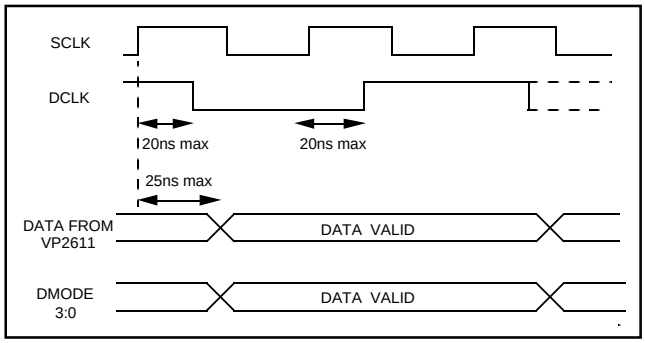


Fig 8: Timing diagram

GOB Number : At the start of each new macroblock, the current GOB Number is output on DBUS3:0. (DBUS3 is MSB).

MB Number : After the GOB Number, the macroblock Number is output on DBUS5:0 (DBUS5 is MSB).

Coded Block Pattern : This byte contains a 6 bit linear code that indicates which of the sub-blocks actually contain coded data. DBUS6 will be high if sub-block 1 contains coded data, through to DBUS 1 being high if sub-block 6 contains coded data. DBUS7 and DBUS0 are not used. Note that if the macro block is not motion compensated and the coded block pattern is all zero's, the fixed macro block bit will be set in the control decisions byte.

Quant Value : The quantisation value used in processing the current macroblock is output on DBUS4:0 (DBUS4 is MSB). This represents an actual quantisation level between 2 and 62, in steps of 2 and as defined in H.261.

Horizontal MV : If motion compensation is used, the horizontal component of the motion vector will be output on DBUS4:0 (DBUS4 is MSB). This 5 bit value represents a two's complement number in the range +/-15 (although only vectors in the range -8 to +7 are currently possible with the VP2611).

Vertical MV : If motion compensation is used, the vertical component of the motion vector will be output on DBUS4:0 (DBUS4 is MSB). This 5 bit value represents a two's complement number in the range ±15 (although only vectors in the range ±7 are currently possible with the VP2611).

CBUS3:0	INSTRUCTION
0000	Input VAR Threshold
0001	Reserved
0010	Input Inter Quantiser
0011	Input Intra Quantiser
0100	Input Setup Data
0101	Input Control Functions
0110	Reserved
0111	Reserved
1000	Output GOB Number
1001	Output MB Number
1010	Reserved
1011	Output Control Decisions
1100	Output Setup Data
1101	Reserved
1110	Reserved
1111	Overide internal clock doubler

Table 3 : CBUS Instruction Codes

Sub-block Number : An identifier for the run length coded coefficients which are about to be made available. DBUS 2:0 contain the coded sub-block number from 1 to 6. All zero sub-blocks will not be produced at the outputs, and their corresponding numbers will not appear.

Zero Run Count : The number of zero valued coefficents preceding the next non zero coefficient is available on DBUS5:0 (DBUS5 is MSB). Normally, DBUS7:6 are low, except to signify the end of a Sub-block, when they will both be high. Zero Run Count is always followed by a coefficient, even at the end of a sub-block.

RLC Coefficient : This byte contains the 8 bit coefficient value. It will always be a non-zero value, except when the previous Zero Run Count signalled the end of sub-Block. A zero value is then possible since, as stated above, the run count is always followed by a coefficient byte, which may be zero if the last coefficient is zero.

Wait State : This indicates that no valid data is being output from the DBUS port during this cycle. No DCLK is produced for this state.

Pins which are "not used" for certain functions will be forced low.

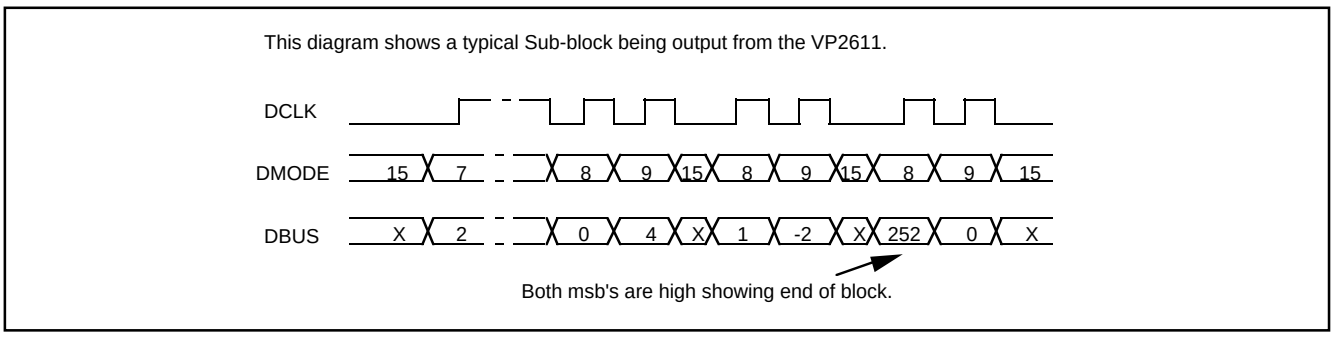


Fig 9: DBUS Timing

CBUS Control Port

The CBUS control port is used to input control and setup information and also to output status information. In order to save on pin count, a microprocessor driving this port is required to execute two I/O instructions in order to transfer a single byte of information to or from the device. The first transfer is always a write operation, with a low level on the single address line which is used by the interface. Data on the bus then defines the instructions listed in Table 3. The second transfer can be a read or write operation as necessary, but the address line must then be high with the set up time given in Figure 10.

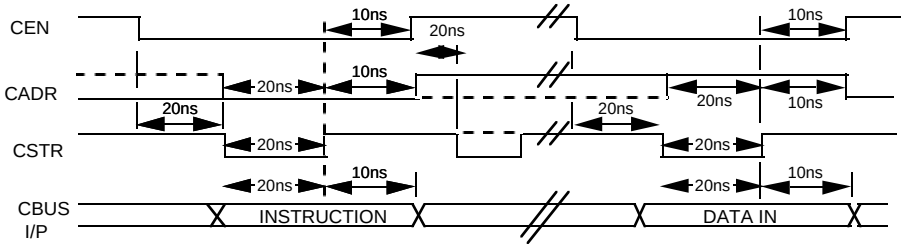
In addition to the single addresss line (CADR), data transfers use a control strobe (CSTR) which is only effective when a chip enable is present (CEN). Detailed timing information is given in Figure 10, and when writing data or instructions to the VP2615 the set up and hold times which are referenced to the rising edge of CSTR must be maintained.

When a write instruction has been defined CADR should be pulled high, valid data presented to CBUS7:0 and then strobed in using CSTR. Other system I/O transfers can occur between defining a write operation and supplying the data to be written, assuming CEN is not active during those other transfers. If CSTR does not go active because of I/O transfers to other devices, then CEN can remain active low between the instruction and data.

When a read instruction has been specified the requested data will then be output on CBUS7:0 after the access time specified from CEN going low, assuming that CADR was already high. Otherwise the data will become valid after the access time specified from CADR going high after CEN was

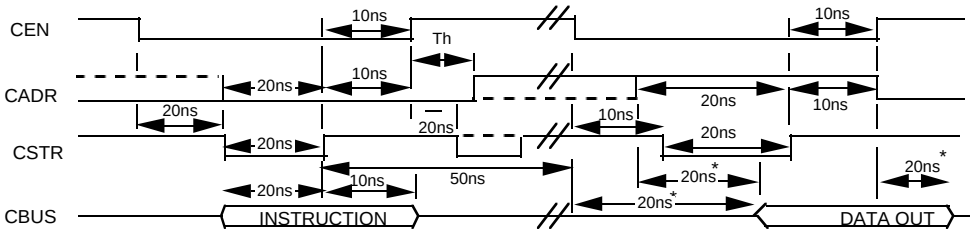
WRITING DATA FROM THE CBUS:

This diagram shows a typical instruction and associated data field being written to the device.



READING INFORMATION ON CBUS :

This diagram shows a typical instruction and associated data field being read from the device.



If Th is less than 5 ns then CBUS may be driven by the VP2615until CEN going high eventually turns off the drivers. It will not prevent correct data being read when CEN again goes active

N.B. All timings shown are minimum values except those marked * which are maximums.

Fig 10 : Use of the Control Port

low. Note that in the data read phase CADR must always go high before CSTR goes high, with the set up time specified. When CEN goes high, or CADR goes low, the CBUS will go high impedance after the delay specified.

Note that the access times under the conditions given above are only true when the gap between CSTR going high in the instruction phase, and CEN going low in the data phase, is greater than the minimum specified in figure 10.

Only the four LSBs, CBUS3:0, are used when writing instructions to the VP2611. The remaining bits, CBUS7:4, should be pulled low while the instruction is strobed into the VP2611.

The instructions listed in Table 3 are described below in greater detail;

Input VAR Threshold: VAR is the difference between the best fit MAE value and the variance of the current macroblock. The VAR Threshold is the best fit MAE value below which Inter Frame Prediction is always used, no matter what the variance of the current block. Above this threshold inter mode coding is only used if the best fit value is less than the current block variance. The default value is 3, within a range of 0 - 255 using the eight most significant bits of the 14 bit value. In normal operation values below 15 should be used.

Input Inter Quantiser: Coefficents of inter coded macroblocks will be quantized using the value on CBUS4:0 following this instruction. Internally this represents a 6 bit number with the lsb always zero, giving a value between 0 and 62 in steps of two. Where only one quantization value is to be used for both inter and intra cases, this instruction should be used. On reset the value will default to the maximum allowed. See note below.

Input Intra Quantiser: This instruction is similar to the above, except that it defines the quantization level for intra mode coding when it is to be different to that of inter mode coding. See note below.

Input Setup Data: This instruction allows several user defined options to be specified, using individual bits in the following data word. If CBUS0 is LOW the device will work in full CIF mode , if HIGH it uses the QCIF mode. If CBUS3 is HIGH both inter and intra quantization values will be used, otherwise a common value will be used. If CBUS5 is high then the motion compensation circuits will be disabled. If CBUS6 is high, then the device will be configured to use 256K x 16 or 256K x 4 DRAM's, otherwise it will assume the use of two 64K x 16 DRAM's. The default conditions after RESET are those selected by the Low level. CBUS1, CBUS2, CBUS4 and CBUS7 are not used but must be low during the definition phase. This instruction may be used any time after RESET has gone high, but the video input bus must not be active. If a subsequent mode change between CIF and QCIF is made then a further RESET is needed.

Input Control Functions: This instruction specifies several control options using individual bits in the following data word. If CBUS0 is HIGH then the on board Inter/Intra Decision circuitry will be overidden according to CBUS1; if CBUS1 is HIGH then all subsequent macroblocks will be intra coded, if it is LOW they will be inter coded. When CBUS2 is HIGH the on-board Filter Decision circuitry is overidden according to CBUS3; if CBUS3 is HIGH then the filter will be forced on, if it is LOW the filter will be forced off. If CBUS4 is HIGH then FIX MB will be implemented, and no new data from the current macroblock will be coded. A two macroblock delay exists between defining the Force Inter/Intra, Force Filter or FIX MB decisions through the control bus and data being affected at the outputs. These decisions will stand for all subsequent macroblocks until they are again changed. If CBUS5 is HIGH a FAST UPDATE will be performed on the next frame and all blocks will be coded in intra mode. If CBUS6 is HIGH then the next frame will not be transmitted (SKIP FRAME). Note that these two global frame bits do not take effect until the start of the next frame, and stay in effect for all frames until they are removed. If CBUS7 is HIGH, then the on-board Force Update Controller will be overidden, and the user will have to enforce their own Force Update policy using the Force Intra command. RESET will cause the options to default to those defined by the LOW state. Note that SKIP FRAME has priority over any other bits and that FIXMB has priority over all bits bar SKIP FRAME. See note below.

Output GOB Number: This instruction will output the GOB Number on CBUS3:0, for the data currently being output on DBUS. CBUS7:4 are not used (always low).

Output MB Number: This instruction will output the macroblock number on CBUS5:0, for the data currently being output on DBUS. If CBUS6 is low it indicates that the macroblock number has just changed, or is about to change. New Quantization Value or Control Function words should not be written at this time since it is uncertain which macroblock they will effect. CBUS7 is not used (always low).

Output Control Decisions: This instruction will output the details of several control decisions on the CBUS. CBUS0 shows whether the MacroBlock currently being output on DBUS was inter or intra coded (0=Intra). CBUS1 shows whether motion compensation was used (1=MC used). CBUS3 shows whether the macroblock was passed through the loop filter or not (1=Filtered). CBUS4 will be high if the FIX MB instruction was enforced. CBUS5 will be high if FAST UPDATE is currently being undertaken. CBUS6 will be high if SKIP FRAME is in force. CBUS2 and CBUS7 are not used.

Output Setup Data: This instruction allows the user to verify the internal setup previously selected. The bits have the same significance as in the Input Setup Data Instruction.

Note

For definitive operation the output MB number should be read first, and these bytes only changed if CBUS b is high.

Initialising the VP2611

On power-up, RESET should be low and must remain low for at least 2064 cycles of SYSCLK. After RESET is pulled high, FRMIN may be activated to start the first frame. Before activating FRMIN for the first time, it is advisable to use the CBUS to implement a FAST UPDATE for the first frame (i.e. all blocks Intra coded).

JTAG Test Interface

The VP2611 includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

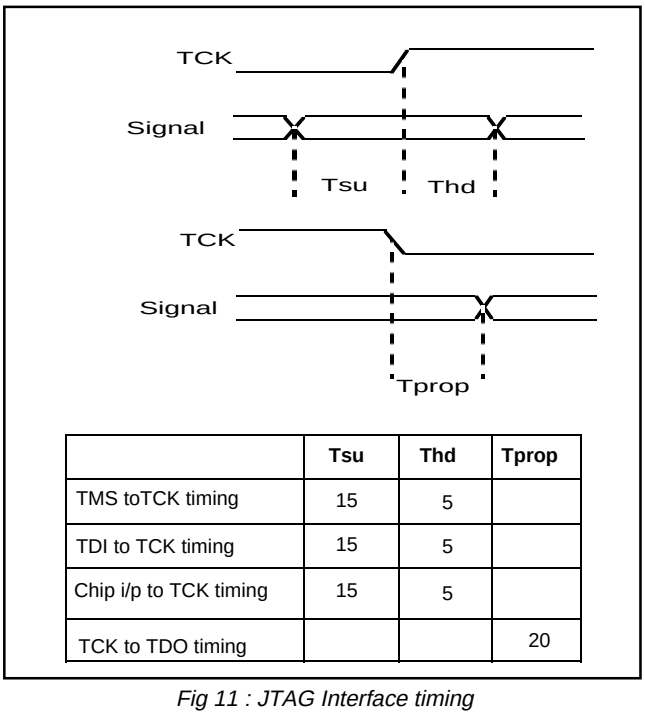
TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 8 bit instruction register (no parity bit) and the following are available.

Instruction Register (MSB first)	Name
11111111	BYPASS
00000000	EXTEST (No inversion)
01000000	INTEST
XX001011	SAMPLE/PRELOAD

Timing details for the JTAG control signals are shown in fig 11.The maximum TCK frequency is 5 MHz.

The test registers, their positions in the boundary loop and the corresponding i/o pad are detailed in Table 4. Note that the three state control signals also have test registers associated with them which are labelled as TRI in Table 4. DHz is an output enable for all signals to the DRAM. The order given in Table 4 determines the serial data stream needed for JTAG testing.



	Tsu	Thd	Tprop
TMS toTCK timing	15	5	
TDI to TCK timing	15	5	
Chip i/p to TCK timing	15	5	
TCK to TDO timing			20

Fig 11 : JTAG Interface timing

Pad	Type	Reg No	Pad	Type	Reg No	Pad	Type	Reg No
RESET	IN	93	DBUS5	OP	62		IN	31
CADR	IN	92	DBUS6	OP	61	SW1	OP	30
CSTR	IN	91	DBUS7	OP	60		IN	29
CEN	IN	90	SW15	OP	59	SW0	OP	28
CBUS0	OP	89		TRI	58		IN	27
	TRI	88		IN	57	DHZ	TRI	26
	IN	87	SW14	OP	56	RAS	OP	25
CBUS1	OP	86		IN	55	CAS	OP	24
	IN	85	SW13	OP	54	RW1	OP	23
CBUS2	OP	84		IN	53	RW2	OP	22
	IN	83	SW12	OP	52	OE1	OP	21
CBUS3	OP	82		IN	51	OE2	OP	20
	IN	81	SW11	OP	50	ADR0	OP	19
CBUS4	OP	80		IN	49	ADR1	OP	18
	IN	79	SW10	OP	48	ADR2	OP	17
CBUS5	OP	78		IN	47	ADR3	OP	16
	IN	77	SW9	OP	46	ADR4	OP	15
CBUS6	OP	76		IN	45	ADR5	OP	14
	IN	75	SW8	OP	44	ADR6	OP	13
CBUS7	OP	74		IN	43	ADR7	OP	12
	IN	73	SW7	OP	42	PCLK	IN	11
DCLK	OP	72		IN	41	YUV7	IN	10
DMODE0	OP	71	SW6	OP	40	YUV6	IN	9
DMODE1	OP	70		IN	39	YUV5	IN	8
DMODE2	OP	69	SW5	OP	38	YUV4	IN	7
DMODE3	OP	68		IN	37	YUV3	IN	6
DBUS0	OP	67	SW4	OP	36	YUV2	IN	5
DBUS1	OP	66		IN	35	YUV1	IN	4
DBUS2	OP	65	SW3	OP	34	YUV0	IN	3
DBUS3	OP	64		IN	33	SYSCLK	IN	2
DBUS4	OP	63	SW2	OP	32	FRMIN	IN	1
						REQYUV	OP	0

Table 4 Pin and JTAG test registers

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage VDD	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to VDD+ 0.5V
Output voltage V_{OUT}	-0.5V to VDD + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-55°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	125°C
Package power dissipation	3000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation for 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C VDD = 5.0v ± 5%

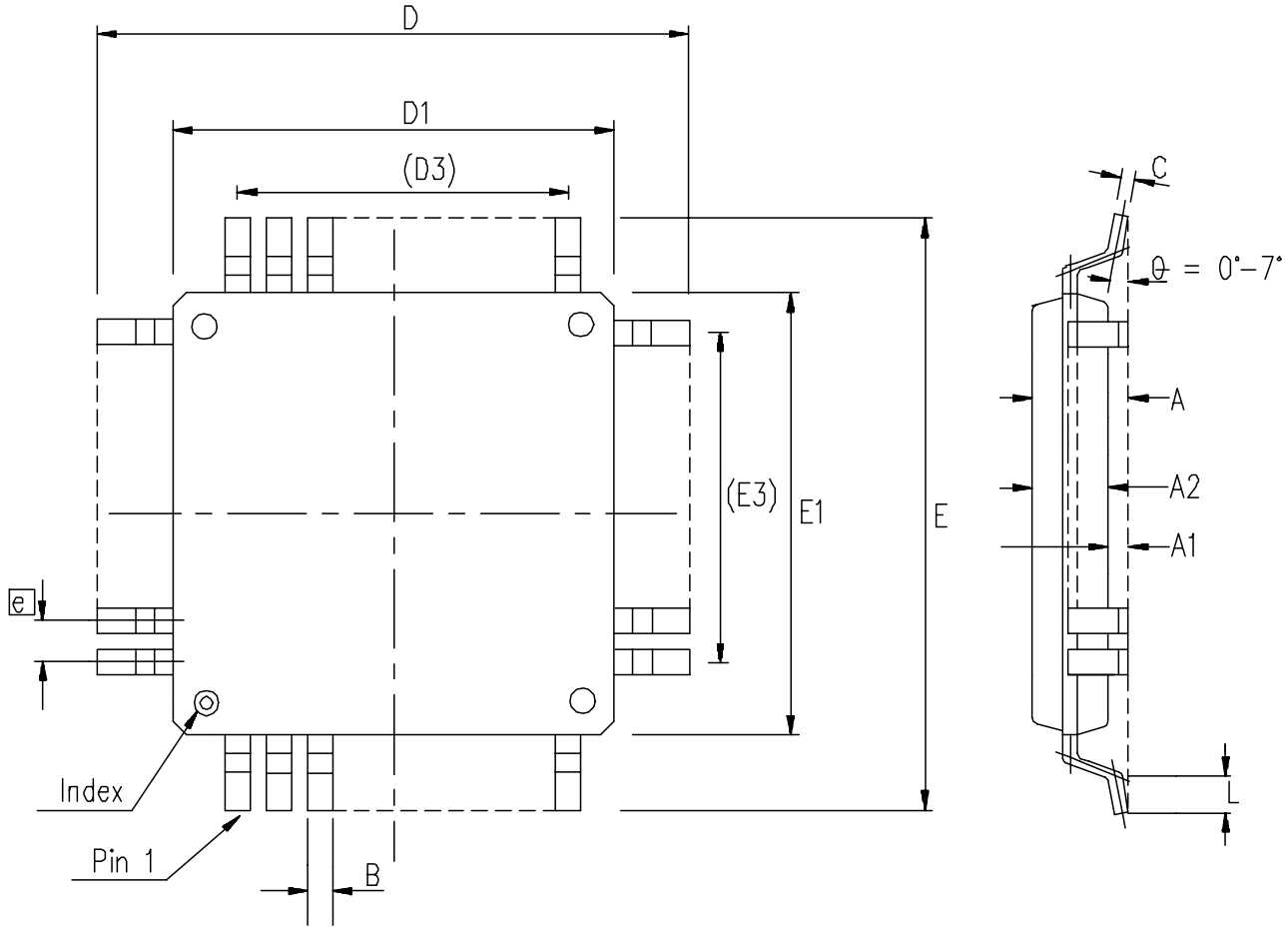
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	V_{DD} -1V for SYSCLK and PCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	V_{DD} = Max

ORDERING INFORMATION

VP2611 CG GH1R (Commercial - Plastic QFP power package)

Pin	Function	Pin	Function	Pin	Function
1	SW3	44	DCLK	87	YUV3
2	NC	45	NC	88	NC
3	SW4	46	CBUS7	89	YUV4
4	SW5	47	VDD	90	YUV5
5	GND	48	CBUS6	91	VDD
6	VDD	49	GND	92	GND
7	SW6	50	VDD	93	YUV6
8	SW7	51	CBUS5	94	YUV7
9	NC	52	GND	95	NC
10	SW8	53	CBUS4	96	PCLK
11	SW9	54	CBUS3	97	NC
12	SW10	55	CBUS2	98	NC
13	SW11	56	CBUS1	99	ADR7
14	NC	57	NC	100	ADR6
15	GND	58	GND	101	ADR5
16	SW12	59	VDD	102	VDD
17	NC	60	CBUS0	103	GND
18	VDD	61	TRST	104	NC
19	SW13	62	CEN	105	ADR4
20	SW14	63	NC	106	ADR3
21	NC	64	NC	107	ADR2
22	SW15	65	CSTR	108	ADR1
23	DBUS7	66	NC	109	GND
24	DBUS6	67	CADR	110	ADR0
25	NC	68	RESET	111	VDD
26	DBUS5	69	VDD	112	GND
27	GND	70	GND	113	NC
28	VDD	71	TCK	114	OE2
29	DBUS4	72	TMS	115	OE1
30	DBUS3	73	TDI	116	VDD
31	NC	74	NC	117	RW2
32	DBUS2	75	TDO	118	RW1
33	NC	76	(CLK54)	119	CAS
34	NC	77	REQYUV	120	RAS
35	DBUS1	78	FRMIN	121	VDD
36	DBUS0	79	VDD	122	GND
37	DMODE3	80	NC	123	NC
38	NC	81	SYSCLK	124	SW0
39	GND	82	GND	125	SW1
40	VDD	83	NC	126	SW2
41	DMODE2	84	YUV0	127	NC
42	DMODE1	85	YUV1	128	NC
43	DMODE0	86	YUV2		

Pin out table for GH128 PQFP package



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	3.91		---	0.154
A1	0.25	---		0.010	---
A2	3.17	3.67		0.125	0.144
D	31.65	32.15		1.246	1.266
D1	27.90	28.10		1.098	1.106
D3	24.80 REF			0.976 REF	
E	31.65	32.15		1.246	1.266
E1	27.90	28.10		1.098	1.106
E3	24.80 REF			0.976 REF	
L	0.65	0.95		0.026	0.037
e	0.80 BSC			0.0315 BSC	
B	0.30	0.45		0.011	0.018
C	0.13	0.23		0.005	0.009
	Pin features				
N	128				
ND	32				
NE	32				
NOTE	SQUARE				

NOTES:–
1. CONTROLLING DIMENSIONS ARE IN MM.
2. This document supersedes 418/ED/51699/004 issue 1

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