

# VP2410 SERIES

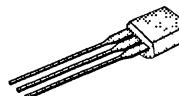
**Siliconix**  
incorporated

P-Channel Enhancement-Mode MOS Transistors

## PRODUCT SUMMARY

PART NUMBER	V <sub>(BR)DSS</sub> (V)	r <sub>DSON</sub> (Ω)	I <sub>D</sub> (A)	PACKAGE
VP2410L	-240	10	-0.18	TO-92
VP2410B	-240	10	-0.17	TO-205AF

TO-92

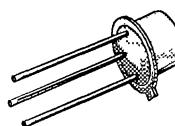


BOTTOM VIEW

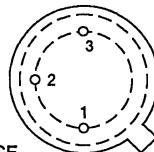


1 SOURCE  
2 GATE  
3 DRAIN

TO-205AF



BOTTOM VIEW



1 SOURCE  
2 GATE  
3 DRAIN & CASE

Performance Curves: VPDV24 (See Section 7)

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	VP2410L	VP2410B	UNITS
Drain-Source Voltage	V <sub>DS</sub>	-240	-240	V
Gate-Source Voltage	V <sub>GS</sub>	±30	±20	
Continuous Drain Current	I <sub>D</sub>	-0.18	-0.17	A
T <sub>A</sub> = 100°C		-0.11	-0.10	
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	-0.72	-0.70	W
Power Dissipation	P <sub>D</sub>	0.80	0.73	
T <sub>A</sub> = 100°C		0.32	0.22	
Operating Junction and Storage Temperature	T <sub>j</sub> , T <sub>stg</sub>	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)	T <sub>L</sub>	300		

## THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP2410L	VP2410B	UNITS
Junction-to-Ambient	R <sub>thJA</sub>	156	170	°C/W

<sup>1</sup>Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS <sup>1</sup>			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	VP2410		UNIT
				MIN	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -5 μA	-255	-240		V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -2.5 mA	-2.25	-0.8	-2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V V <sub>GS</sub> = ±20 V	±1		±10	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -180 V V <sub>GS</sub> = 0 V	±5		±50	
On-State Drain Current <sup>3</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V	-0.001		-1.0	μA
Drain-Source On-Resistance <sup>3</sup>	r <sub>DS(ON)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -100 mA	-0.40		-100	
Forward Transconductance <sup>3</sup>	g <sub>FS</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V	-300	-150		mA
Common Source Output Conductance <sup>3</sup>	g <sub>OS</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -50 mA	7			
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -25 V V <sub>GS</sub> = 0 V f = 1 MHz	65		95	pF
Output Capacitance	C <sub>oss</sub>		20		30	
Reverse Transfer Capacitance	C <sub>rss</sub>		8		15	
<b>SWITCHING</b>						
Turn-On Time	t <sub>d(ON)</sub>	V <sub>DD</sub> = -25 V, R <sub>L</sub> = 250 Ω I <sub>D</sub> = -100 mA, V <sub>GEN</sub> = -10 V R <sub>G</sub> = 25 Ω (Switching time is essentially independent of operating temperature)	7		15	ns
	t <sub>r</sub>		18		30	
Turn-Off Time	t <sub>d(OFF)</sub>		45		70	
	t <sub>f</sub>		45		60	

NOTES: 1. T<sub>A</sub> = 25 °C unless otherwise noted.

2. For design aid only, not subject to production testing.

3. Pulse test; PW = 300 μs, duty cycle ≤ 2%.